DESCRIPTION

The TSEV8388BFS Evaluation Board (EB) is a prototype board which has been designed in order to facilitate the evaluation and the characterization of the TS8388BF device (in CQFP68) up to its 1.5 GHz full power bandwidth at up to 1 Gsps in the military temperature range.

The high speed of the TS8388BF requires careful attention to circuit design and layout to achieve optimal performance. This four metal layer board with internal ground plane has the adequate functions in order to allow a quick and simple evaluation of the TS8388BF ADC performances over the temperature range.

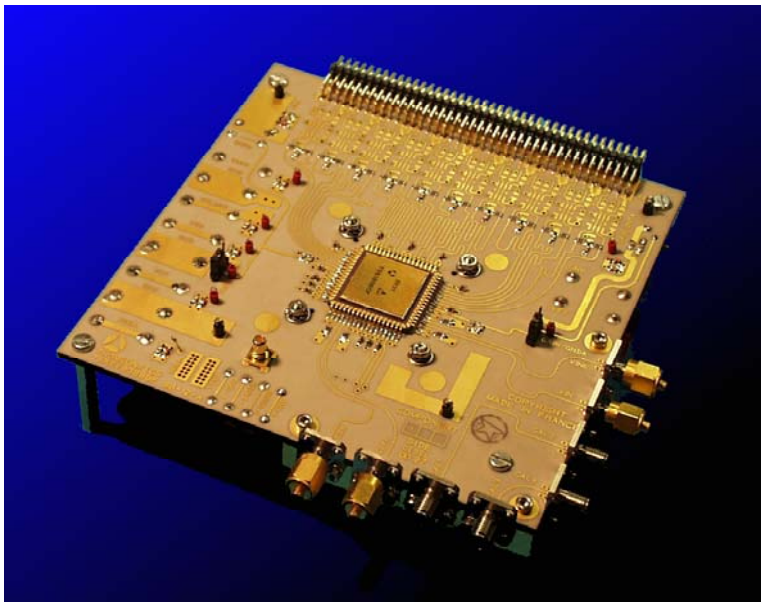
The TS8388BF Evaluation Board (EB) is very straightforward as it only implements the TS8388BF ADC device, SMA connectors for input / output accesses and a 2.54 mm pitch connector compatible with HP16500C high frequency probes.

The board also implements a de-embedding fixture in order to facilitate the evaluation of the high frequency insertion loss of the inputs microstrip lines, and a die junction temperature measurement setting.

The board is constituted by a sandwich of two dielectric layers, featuring low insertion loss and enhanced thermal characteristics for operation in the high frequency domain and extended temperature range.

The board dimensions are 130 mm x 130 mm.

The board set comes fully assembled and tested, with the TSX8388BF installed.



ADC 8-bit 1 Gsps Converter Evaluation Board

TSEV8388BFS

January 2002

TABLE OF CONTENTS

LIST OF FIGURES

1. TSEV8388BFS BLOCK DIAGRAM

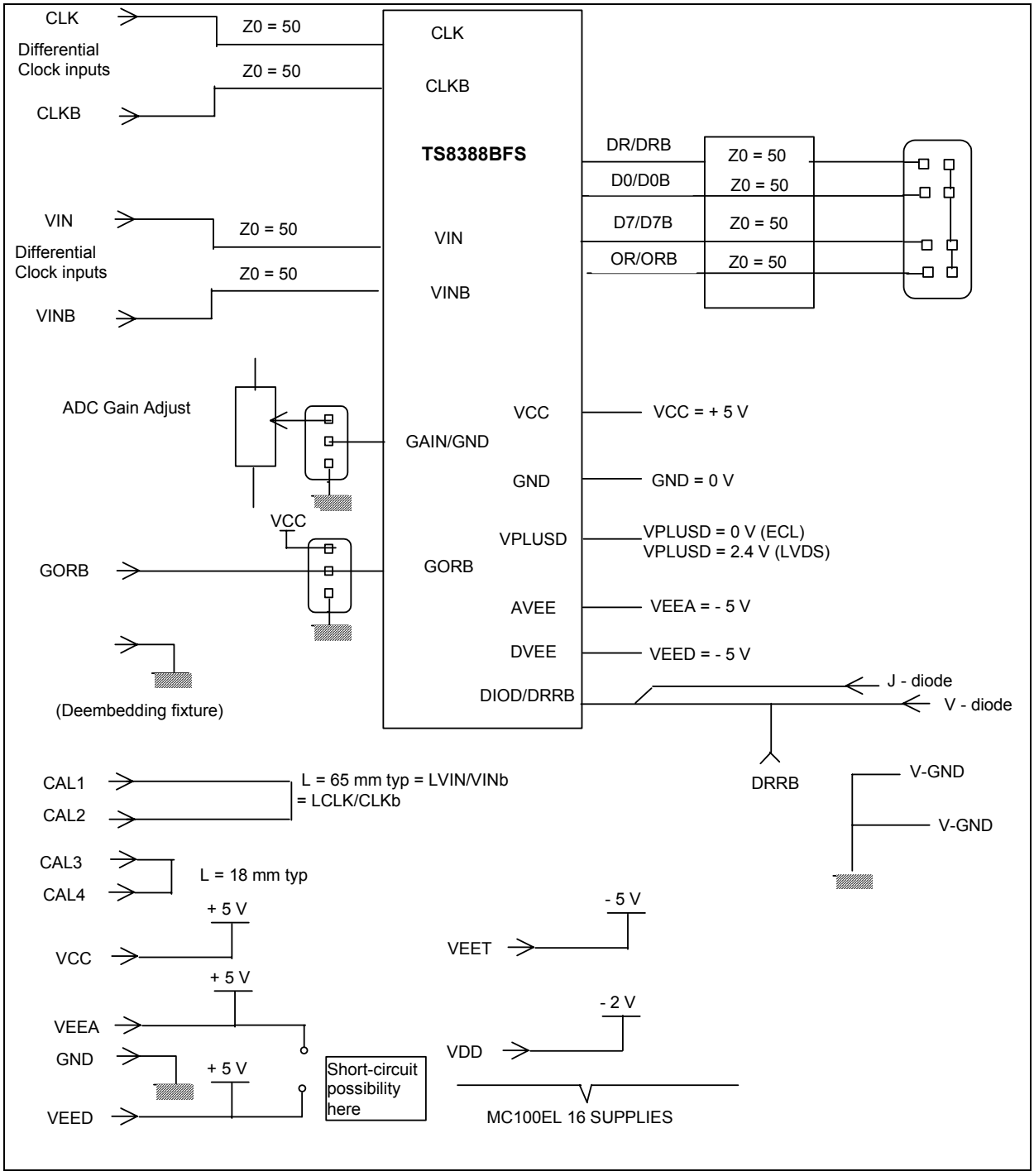


Figure 1 : TSEV8388BFS BLOCK DIAGRAM

2. DETAILED DESCRIPTION

2.1. BOARD MECHANICAL CHARACTERISTICS

2.1.1. BOARD LAYERS THICKNESS PROFILE :

The board layers number, thickness, and functions are given below, from top to bottom :

Layer 1 : Copper layer	Copper thickness = 35 µm AC signals traces = 50 ohms microstrip lines DC signals traces (GORB, GAIN, DIODE)
Layer 2 : RO4003 dielectric layer (Hydrocarbon / wovenglass) :	Layer thickness = 200 µm dielectric constant = 3.4 @ 10 GHz – 0.044 dB / inch insertion loss @ 2.5 GHz – 0.318 dB / inch insertion loss @ 18 GHz
Layer 3 : Copper layer	Copper thickness = 35 µm upper ground plane = reference plane 50 ohms microstrip return
Layer 4 : BT / Epoxy dielectric layer	Layer thickness = 1.2 mm
Layer 5 : Copper layer	Copper thickness = 35 µm lower ground plane (board mechanical rigidity)
Layer 6 : BT / Epoxy dielectric layer	Layer thickness = 1.2 mm
Layer 7 : Copper layer	Copper thickness = 35 µm Power planes = VEEA, VEED, VEET, VDD, VCC, VPLUSD ground plane

The TSEV8388BFS is a seven layer PCB constituted by four copper layers and three dielectric layers.

The four metal layers correspond respectively from top to bottom to the AC and DC signals layer (layer 1) (Fig.9), two ground layers (layers 3 and 5) (Fig.10), and one supply layer (layer 7) (Fig.11).

The upper inner ground plane (layer 3) constitutes the reference plane for the 50 ohms impedance signal traces. The lower inner ground plane (layer 5) is used for dielectric substrate rigidity and is a replica of the upper ground plane.

The backside metal layer is dedicated to the power supplies planes, surrounded by a ground plane.

The three dielectric layers are respectively (from top to bottom) constituted by a low insertion loss dielectric layer (RO4003) (layer 2) and two parallel BT/Epoxy dielectric layers (layers 4 and 6).

Considering the severe mechanical constraints due to the wide temperature range and the high frequency domain in which the board is to operate, it was necessary to use a sandwich of two different dielectric materials, with specific characteristics :

A low insertion loss RO4003 Hydrocarbon / wovenglass dielectric layer of 200 µm thickness, chosen for its low loss (- 0.318 dB / inch) and enhanced dielectric consistency in the high frequency domain. The RO4003 dielectric layer is dedicated to the routing of the 50 ohms impedance signal traces. (The RO4003 typical dielectric constant is 3.4 @ 10 GHz). The RO4003 dielectric layer characteristics are very close to PTFE in terms of insertion loss characteristics.

A BT / Epoxy dielectric layer of 2 mm total thickness which is sandwiched between the upper ground plane and the back-side supply layer.

The BT / Epoxy layer has been chosen because of its enhanced mechanical characteristics for elevated temperature operation. The typical dielectric constant is 4.5 @ 1 MHz.

More precisely, the BT / Epoxy dielectric layer offers enhanced characteristics compared to FR4 Epoxy, namely :
- higher operating temperature value : 170° C (125° C for FR4),
- better with standing of thermal shocks (- 65° C up to 170° C).

The total board thickness is 2.6 mm.

The previously described mechanical and frequency characteristics makes the board particularly suitable for the device evaluation and characterization in the high frequency domain and in the military temperature range.

2.1.2. ANALOG INPUT, CLOCK INPUT, DE-EMBEDDING FIXTURE ACCESSES :

The differential active inputs (Analog, Clock, De-embedding fixture) are provided by SMA connectors.
Reference : RADIALL R 125620001.

Connector mounting plates have been used for fastening the SMA connectors.

2.1.3. DIGITAL OUTPUTS ACCESSES :

Access to the differential output data port is provided by a 2.54 mm pitch connector, compatible with HP16500 Digital Acquisition System. It enables access to the converter output data, as well as proper 50 ohms differential termination.

2.1.4. POWER SUPPLIES AND GROUND ACCESSES :

The power supplies accesses are provided by five 4 mm section banana jacks respectively for VEEA, VEED, VEET, VDD, VPLUSD and VCC.

The Ground accesses are provided by 4 mm and two 2 mm banana jacks.

2.1.5. ADC FUNCTIONS SETTINGS ACCESSES :

For ADC functions settings accesses (GORB, Die junction temp., ADC Gain adjust), smaller 2 mm section banana jacks are provided. A potentiometer is provided for ADC gain adjust.

2.2. LAYOUT INFORMATION

2.2.1. BOARD :

The TS8388BFS requires proper board layout for optimum full speed operation.

The following explains the board layout recommendations and demonstrate how the Evaluation Board fulfills these implementation constraints.

A single low impedance ground plane is recommended, since it allows to lay out signal traces and power planes without interrupting the ground plane.

Therefore a multi-layer board structure has been retained for the TSEV8388BFS.
Four copper metal layers are used, dedicated respectively (from top to bottom) to the signal traces, ground planes and power supplies.

The input / output signals traces occupy the top metal layer.
The ground planes occupy the second and third copper metal layers.
The bottom metal layer is dedicated to the power supplies.

2.2.2. AC INPUTS / DIGITAL OUTPUTS :

The board uses 50 ohms impedance microstrip lines for the differential analog inputs, clock inputs, and differential digital outputs, (including the Out of Range Bit and the data ready output signal).

The input signals and clock signals must be routed on one layer only, without using any through-hole vias. The line lengths are matched to within 2 mm.

The analog and clock input lines are properly reverse terminated by 50 ohms surface mount chip resistors placed very close to the ADC device (See Fig. 7 page17).

The digital output lines are 50 ohms differentially terminated.

The output data traces lengths are matched to within 0.25 inch (6 mm) to minimize the data output delay skew.
For the TSEV8388BFS the propagation delay is approximately 6.1 ps / mm (155 ps /inch).
(The RO4003 typical dielectric constant is 3.4 @ 10 GHz).
For more information about different output termination options refer to the specification application notes.

2.2.3. DC FUNCTIONS SETTINGS (GORB, GAIN, DIE JUNCTION TEMP. MEASUREMENT) :

The DC signals traces are low impedance. They have been routed with 50 ohms impedance near the device because of room restriction.

2.2.4. POWER SUPPLIES :

The bottom metal layer 7 is dedicated to the power supplies traces (VEEA, VEED, VEET, VCC, VDD, VPLUSD). (See Fig. 11).

The supply traces are approximately 6 mm wide in order to present low impedance, and are surrounded by a ground plane connected to the two inner ground planes.

The Analog and Digital negative power supply traces are independent, but the possibility exists to short-circuit both supplies on the top metal layer (see Fig.9).

No difference in ADC high speed performance is observed when connecting both negative supply planes together. Obviously one single negative supply plane could be used for the circuit.

Each power supply incoming is bypassed by a 1 µF Tantalum capacitor in parallel with 1 nF chip capacitor.
Each power supply access is decoupled very close to the device by a 10 nF and 100 pf surface mount chip capacitors in parallel.

Note : the decoupling capacitors are superposed. In this configuration, the 100 pf capacitors must be mounted first.

2.2.5. TS8388BF ON BOARD IMPLEMENTATION :

Surface-mount resistors and chip capacitors allow the closest possible connections to the device pins, for microstrip line back termination and bypassing.

- Connecting the positive supply pads :

The positive supply pads denoted VCC.
The corresponding VCC pad numbers are (19, 21, 23, 30, 39, 40).
Each VCC power supply pad is decoupled as closely to the device as possible by a 1 nF chip capacitor.
The VCC supply pads are connected to the back side VCC plane of the CEB.

The positive digital supply pads are denoted VPLUSD (0 V or 2.4 V).
The corresponding VPLUSD pad numbers are (1, 11).
Each VPLUSD power supply pad is decoupled very close to the device by a 1 nF chip capacitor.
The VPLUSD supply pads are connected to the back side VPLUSD plane of the evaluation board.

- Connecting the negative supply pads :

The TS8388BF has separate analog and digital – 5 Volts supplies :
The negative analog supply pads are denoted VEE.
The VEE corresponding pad numbers are (22, 29, 31).
The negative digital supply pad is denoted DVEE.
The DVEE corresponding pad number is pad 6.
The DVEE supply pad is dedicated to the digital output buffers only.
Each VEE and DVEE power supply pad is decoupled as closely as possible near the device by a 1 nF chip capacitor.

The VEE and DVEE supply pads are respectively connected to the backside layer 7 VEE and VEED supply planes.

- Ground pads connections :

The analog ground pads are denoted GND. The corresponding GND pad numbers are (20, 26, 28, 33, 35, 37).

3. PACKAGE DESCRIPTION.

3.1. TS8388BFS PIN DESCRIPTION

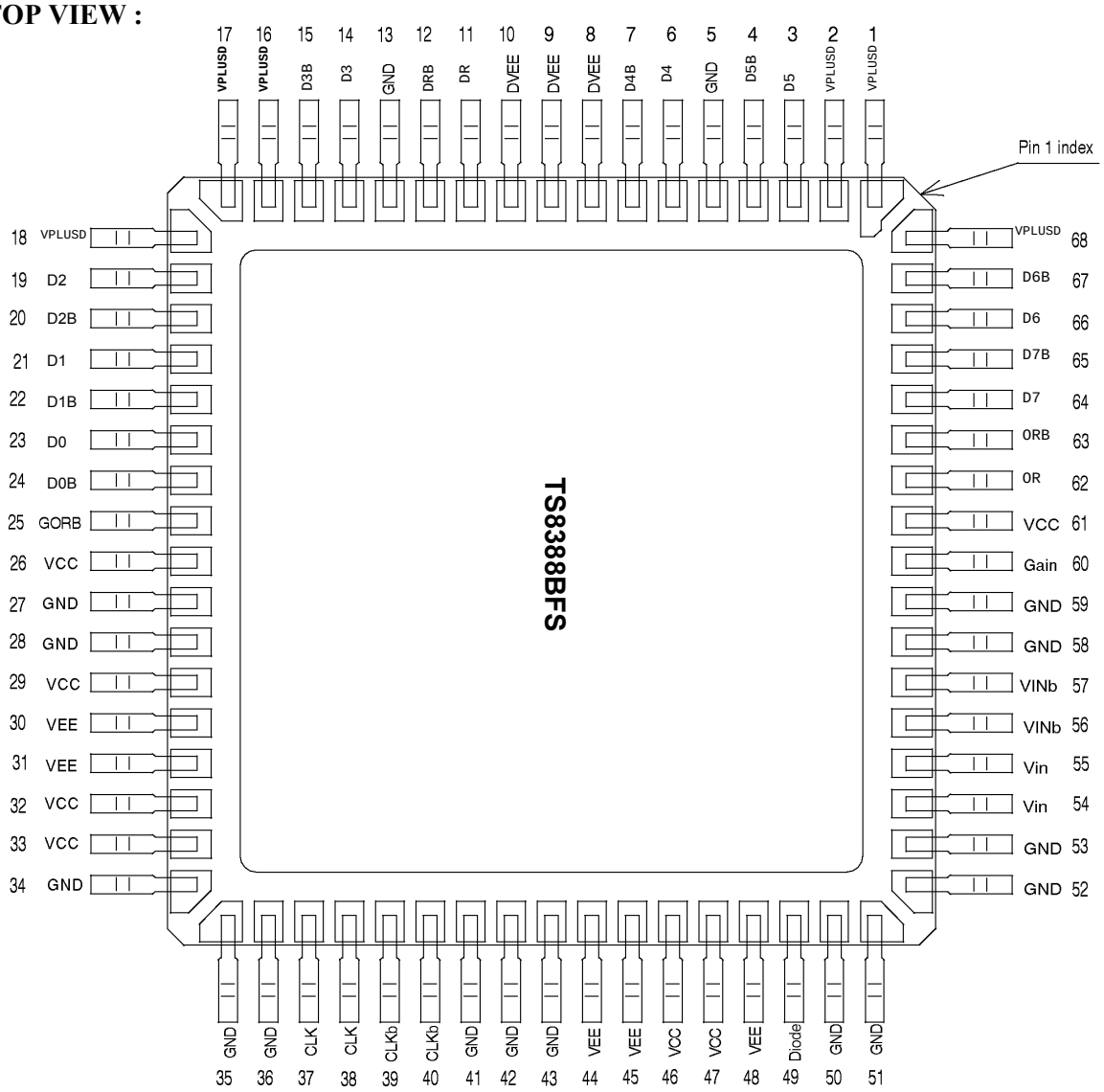
Symbol	Pin number	Function
GND	5, 13, 27, 28, 34, 35, 36, 41, 42, 43, 50, 51, 52, 53, 58, 59	Ground pins. To be connected to external ground plane.
V_{PLUSD}	1, 2, 16, 17, 18, 68	Digital positive supply. (0V for ECL compatibility, +2.4V for LVDS compatibility). *(note 2)*
V_{CC}	26, 29, 32, 33, 46, 47, 61	+5 V positive supply.
V_{EE}	30, 31, 44, 45, 48	-5 V analog negative supply.
DV_{EE}	8, 9, 10	-5 V digital negative supply.
V_{IN}	54(1), 55	In phase (+) analog input signal of the Sample and Hold differential preamplifier.
V_{INB}	56, 57(1)	Inverted phase (-) of analog input signal (V_{IN}).
CLK	37(1), 38	In phase (+) ECL clock input signal. The analog input is sampled and held on the rising edge of the CLK signal.
CLKB	39, 40(1)	Inverted phase (-) of ECL clock input signal (CLK).
D0, D1, D2, D3, D4, D5, D6, D7	23, 21, 19, 14, 6, 3, 66, 64	In phase (+) digital outputs. B0 is the LSB. B7 is the MSB.
D0B, D1B, D2B, D3B, D4B, D5B, D6B, D7B	24, 22, 20, 15, 7, 4, 67, 65	Inverted phase (-) Digital outputs. B0B is the inverted LSB. B7B is the inverted MSB.
OR	62	In phase (+) Out of Range Bit. Out of Range is high on the leading edge of code 0 and code 256.
ORB	63	Inverted phase (+) of Out of Range Bit (OR).
DR	11	In phase (+) output of Data Ready Signal.
DRB	12	Inverted phase (-) output of Data Ready Signal (DR).
GORB	25	Gray or Binary select output format control pin. – Binary output format if GORB is floating or V_{CC}. – Gray output format if GORB is connected at ground (0 V).
GAIN	60	ADC gain adjust pin.
DIOD/DRRB	49	This pin has a double function (can be left open or grounded if not used) : DIOD : die junction temperature monitoring pin. DRRB : asynchronous data ready reset function

Note 1 : Following pin numbers 37 (CLK), 40 (CLKB), 54 (V_{IN}) and 57 (V_{INB}) have to be connected to GND through a 50 Ω resistor as close as possible to the package.(50 Ω termination preferred option).

Note 2 : The common mode level of the output buffers is 1.2V below the positive digital supply.
For ECL compatibility the positive digital supply must be set at 0V (ground).
For LVDS compatibility (output common mode at +1.2V) the positive digital supply must be set at 2.4V.
If the subsequent LVDS circuitry can withstand a lower level for input common mode, it is recommended to lower the positive digital supply level in the same proportion in order to spare power dissipation.

3.2. TS8388BFS PINOUT

TOP VIEW :



3.3. THERMAL CHARACTERISTICS

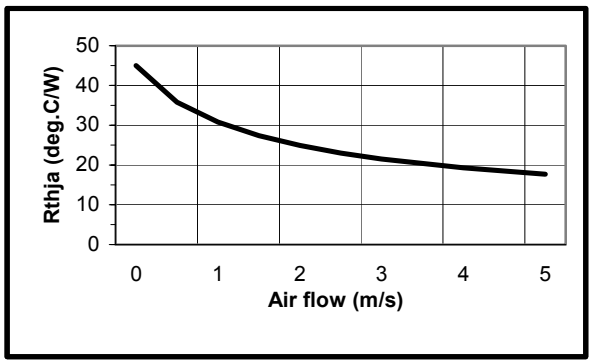
3.3.1. ENHANCED CQFP

The Al_2O_3 CQFP68 has been modified, in order to improve the thermal characteristics :
A CuW heatslug has been added at the bottom of the package.
The die has been electrically isolated with the A_LN substrate.

3.3.2. THERMAL RESISTANCE FROM JUNCTION TO AMBIENT : RTHJA

The following table lists the convector thermal performances parameters of the device itself, with no external heatsink added.

Air flow (m/s)	Estimated ja thermal resistance (°C / W)
0	45
0,5	35,8
1	30,8
1,5	27,4
2	24,9
2,5	23
3	21,5
4	19,3
5	17,7



3.3.3. THERMAL RESISTANCE FROM JUNCTION TO CASE : RTHJC

Typical value for Rthjc is given to 1.56 °C/W.

This value does not include thermal contact resistance between package and external component (heatsink or PCBoard).
As an example, 2.0 °C/W can be taken for 50 µm of thermal grease.

3.3.4. HEATSINK

It is recommended to use an external heatsink or PCBoard special design.

Cooling system efficiency can be monitored using the Temperature Sensing Diode, integrated in the device.

4. APPLICATION INFORMATIONS

For this section, refer also to the product Specification application notes (TS8388Bf Datasheet). More particularly, refer to sections related to single-ended and differential input configurations.

4.1. ANALOG INPUTS

The analog inputs can be entered in differential or Single-ended mode without any high speed performance degradation.

The board digitizes Single-ended signals by choosing either input and leaving the other input open, as the latter is on-board 50 ohms terminated. Nominal In-phase inputs is VIN. (See also Section 6 : Operating Procedure).

4.2. CLOCK INPUTS

The clock inputs can be entered in differential or Single-ended mode without any high speed performance degradation. Moreover, the clock input common mode may be zero volts, or – 1.3 V if ECL input format is used for the clock inputs.

As for the analog input, either clock input can be chosen, leaving the other input open, as both clock inputs are on-board 50 ohms terminated. Nominal in-phase clock input is CLK. (See also section 6 : Operating Procedure).

4.3. SETTING THE DIGITAL OUTPUT DATA FORMAT

For this section, refer to the Evaluation Board Electrical schematic and to components placement document (respectively Fig. 5, 6, 7 and Fig. 12).
Refer also the TS8388BF specification pages about digital output coding.

The TS8388BF delivers data in natural binary code or in Gray code. If the “GORB” input is left floating or tied to Vcc the data format selected will be natural binary, if this input is tied to ground the data will follow Gray code.

Use the jumper denoted ST2 for selecting the output data port format.
- If ST2 is left floating or tied to VCC, the data output format is true Binary,
- If ST2 is tied to GND, the data outputs are Gray formatted.

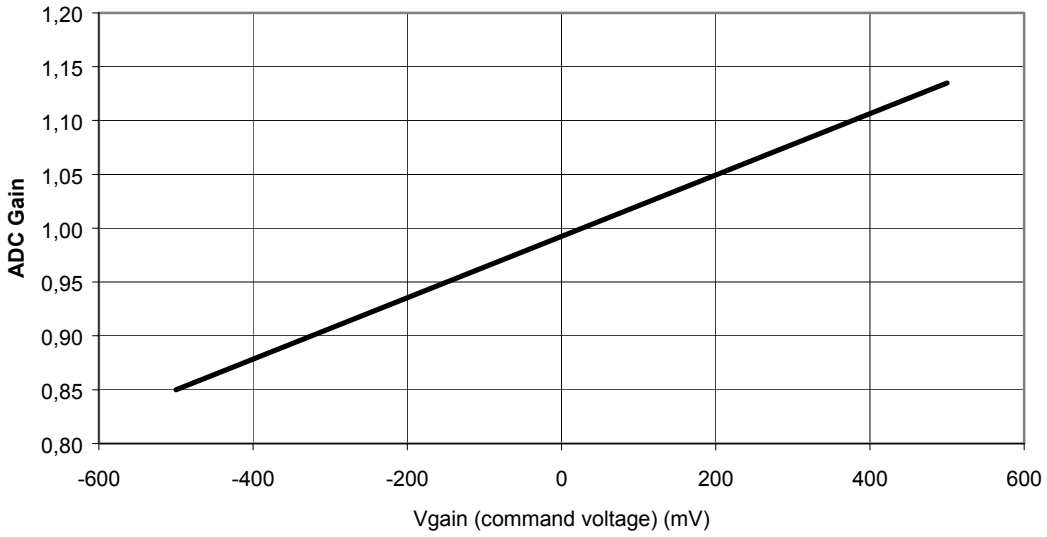
The VPLUSD positive supply voltage allows the adjustment of the output common mode level from – 1.2 V (VPLUSD = 0 V for ECL output compatibility) to + 1.2 V (VPLUSD = 2.4 V for LVDS output compatibility).
Each output voltage varies between – 1.02 V and – 1.35 V (respectively + 1.38 V and + 1.05 V), leading to +/- 0.33 V = 660 mV in differential, around – 1.8 V (respectively + 1.21 V) common mode for VPLUSD = 0 V (respectively 2.4 V).

4.4. ADC GAIN ADJUST

The ADC gain is adjustable by the means of the pin (60) (pad input impedance is 1 MΩ in parallel with 2 pF). A jumper denoted ST1 has been foreseen in order to have access to the ADC gain adjust pin.

The P1 potentiometer is dedicated for adjusting the ADC Gain from approximately 0.85 up to 1.15.

The gain adjust transfer function is given below :



4.5. SMA CONNECTORS AND MICROSTRIP LINES DE-EMBEDDING FIXTURE

Attenuation in microstrip lines can be found by taking the difference in the log magnitudes of the S21 scattering parameters measured on two different lengths of meandering transmission lines.
Such a difference measurement also removes common losses such as those due to transitions and connectors.

The scattering parameter S21 corresponds to the amount of power transmitted through a two-port network.
The characteristic impedance of the microstrip meander lines must be close to 50 ohms to minimize impedance mismatch with the 50 ohms network analyzer test ports.
Impedance mismatch will cause ripple in the S21 parameter as a function of both the degree of mismatch and the length of the line.

4.6. TEMPERATURE MONITORING AND DATA READY RESET FUNCTION

One single pad is used for both DRRB input command and die junction monitoring. The pad denomination is DRRB/DIOD. Temperature monitoring and Data Ready control by DRRB is not possible simultaneously.

4.6.1. TS8388BF ADC DIS JUNCTION TEMPERATURE MEASUREMENT SETUP

For operation in the military temperature range, forced convection is required, to maintain the device junction temperature below the specified maximum value (Tj max = 125° C).

A die junction temperature measurement setting has been included on the board, for junction temperature monitoring.

Four 2 mm section banana jacks (J9, J10, J11, J12) are provided to force current and measure the VBE voltage across the dedicated transistor connected between pads 32 and 33.

The measurement method consists in forcing a 3 mA current flowing into a diode mounted transistor, connected between pad 32 and pad 33 (pad 32 is the emitter and pad 33 is the shorted base-collector).

CAUTION :
Respect the current source polarity.
In any case, make sure the maximum voltage compliance of the current source is limited to maximum 1 Volt or use resistor mounted in serial with the current source to avoid damage occurring to the transistor device (This may occur for instance if current source is reverse connected).

The measurement setup is described in Fig. 2. The diode VBE forward voltage versus junction temperature (in steady state conditions) is given in Fig. 3.

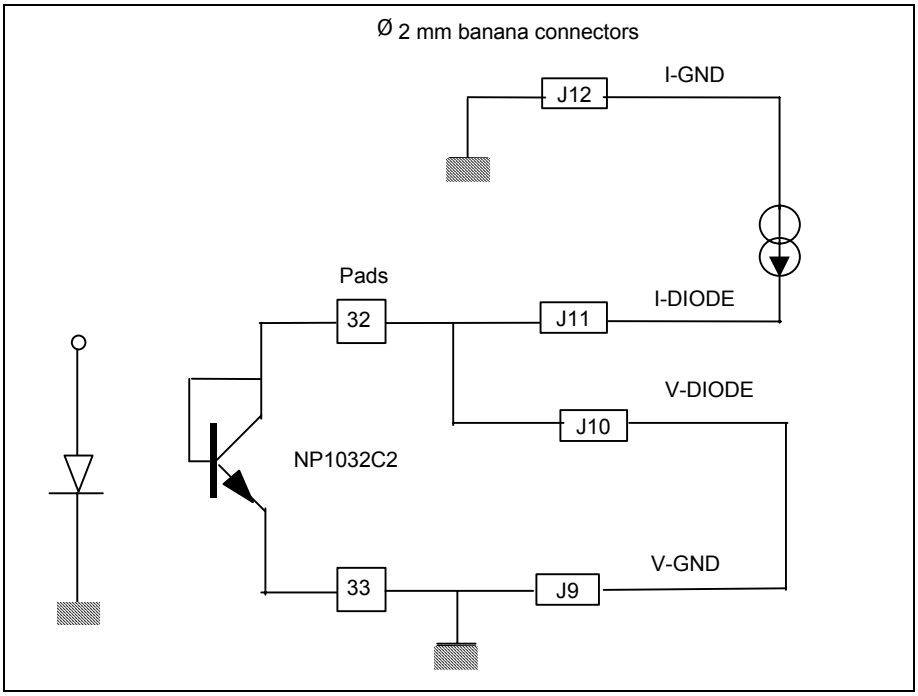


Figure 2 : TS8388BF DIE JUNCTION TEMPERATURE MEASUREMENT SETUP

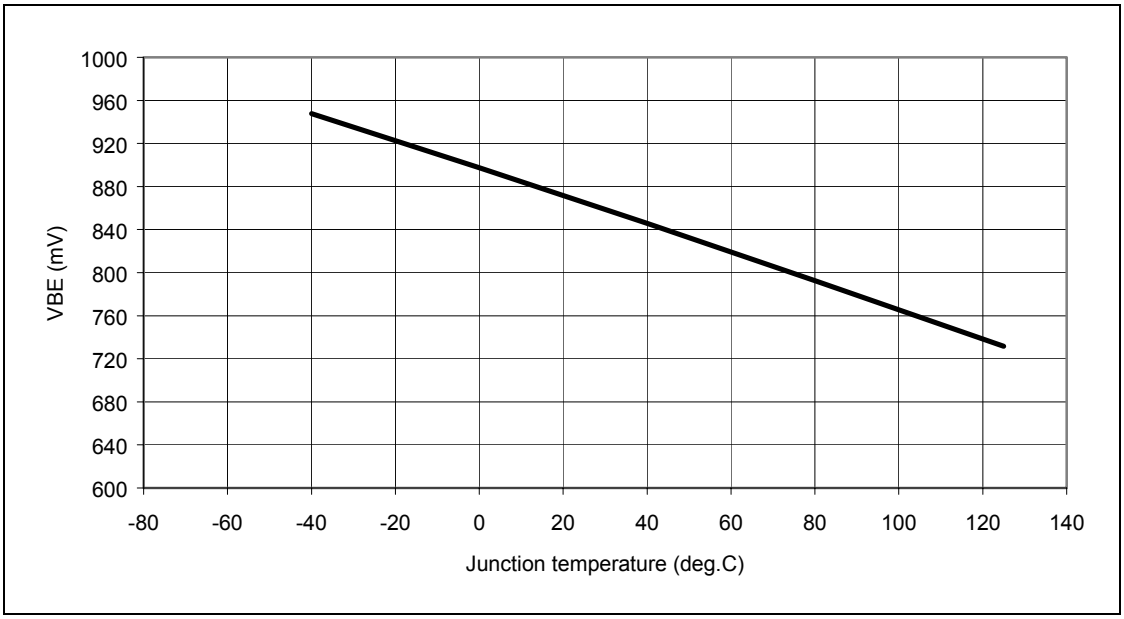


Figure 3 : TRANSISTOR VBE FORWARD VOLTAGE VERSUS JUNCTION TEMPERATURE (I=3mA)

4.6.2. DATA READY OUTPUT SIGNAL RESET :

A subvis connector is provided for DRRB command.

The Data ready signal is reset on falling edge of DRRB input command, on ECL logical low level (- 1.8 V). DRRB may also be tied to VEE = - 5 V for Data Ready output signal master Reset. So long DRRB remains at logical low level, (or tied to VEE = - 5 V), the Data Ready output remains at logical zero and is independent of the external free running encoding clock.

The Data ready output signal (DR, DRB) is reset to logical zero after TRDR = 720 ps typical.
TRDR is measured between the – 1.3 V point of the falling edge of DRRB input command and the zero crossing point of the differential Data Ready output signal (DR, DRB).

The Data ready Reset command may be a pulse of 1 ns minimum time width.

The Data ready output signal restarts on DRRB command rising edge, ECL logical high levels (- 0.8 V).
DRRB may also be grounded, or is allowed to float, for normal free running Data ready output signal.

5. OPERATING CHARACTERISTICS

The power supplies denoted VCC, VEEA, VEED and VPLUSD are dedicated for the TS8388BFS ADC.
The power supplies denoted VEET, VDD are dedicated to the optional MC100EL16 asynchronous differential receivers.

Parameter		Denomination	Min.	Typ.	Max.	Unit
Power supplies (dedicated to TS8388BFS ADC only)	voltage	VCC	+ 4.75	+ 5	+ 5.25	V
	current	ICC		400	425	mA
	voltage	VPLUSD	LVDS : 1.4	ECL : 0 LVDS : 2.4	 LVDS : 2.6	V V
	current	IPLUSD		120	130	mA
	voltage	VEEA	- 5.25	- 5	- 4.75	V
	current	IEEA		170	185	mA
	voltage	VEED	- 5.25	- 5	- 4.75	V
	current	IEED		140	160	mA
Not used by default (dedicated to MC100EL16 differential Receivers) If installed	voltage	VEET	- 5.25	- 5	- 4.75	V
	current	IEET		150		mA
	voltage	VDD	- 2.15	- 2	- 185	V
	current	IDD		390		mA
Nominal Power dissipation (without receivers)		PD		3.6	3.9 (Tj = 125° C)	W
Analog input impedance		ZIN		50		Ω
Full Power Analog Input Bandwidth			1.3	1.5		GHz
Analog input voltage range (differential mode)		VIN	- 125		125	V
Clock input impedance				50		Ω
Clock input voltage compatibility (Single-ended or differential)			ECL levels or 4 dBm (typ) into 50 ohms (see Specification applaication notes)			
Clock input power level (into 50 ohms termination resistor)			- 2	4	10	dBm

6. OPERATING PROCEDURE / QUICK START / RECOMMANDATIONS OF USE

6.1. INTRODUCTION :

This section describes a typical Single-ended configuration for analog inputs and clock inputs.

The single-ended configuration is preferable, as it corresponds to the most straightforward and quickest TSEV8388BFS board setting for evaluating the TS8388BFS at full speed in the military temperature range.

The inverted analog input VINB and clock input CLKB common mode level is Ground (on-board 50 ohms terminated).
In this configuration, no balun transformer is needed to convert properly Single-ended mixer output to balanced differential signals for the analog inputs.

In the same way, no balun is necessary to feed the TS8388BFS clock inputs with balanced signals.

Connect directly the RF sources to the in-phase analog and clock inputs of the converter.

However, dynamic performances can be somewhat improved by entering either analog or clock inputs in differential mode.

6.2. OPERATING PROCEDURE :

A) Connect the power supplies and Ground accesses (VCC = + 5 V, GND = 0 V, VPLUSD = 0 V, VEEA = VEED = - 5 V) through the dedicated banana jacks.

The – 5 Volts power supplies should be turned on first.
Note : one single – 5 V power supply can be used for supplying the digital VEED and analog VEE power planes.

B) The board is set by default for digital outputs in binary format.

C) Connect the CLK clock signal.
The inverted phase clock input CLKB may be left open (as on board 50 ohms terminated).
Use a low phase noise RF source like HP8663 or HP8665.
The clock input level is typically 4 dBm and should not exceed + 10 dBm into the 50 ohms termination resistor (maximum ratings for clock input power level is 15 dBm).
Clock frequency can range between 10 MHz and 1.4 GSPS.

D) Connect the analog signal VIN (the TS8388BF device is not protected against ESD on the analog inputs).
The inverted phase clock input VINB may be left open (as on board 50 ohms terminated).
Use a low phase noise RF source like HP8663 or HP8665.
Full Scale range is 0.5 V peak to peak around 0 Volt, (+/- 250 mV), or – 2 dBm into 50 ohms.
Input frequency can range from DC up to 1.8 GHz.
At 1.7 GHz (TBC), the ADC attenuates by – 3 dB the input signal. The board insertion loss (S21) will be furnished in definitive document release.

E) Connect the high speed data acquisition system probes to the output connector.
The connector pitch (2, 54 mm) is compatible with HP16500 Digital Acquisition System probes.
The digital data are on-board differentially terminated.
However, the output data can be picked up either in single-ended or differentially mode.
For the HP16500, the probes needs to be connected in single-ended.

F) Board functionality verification and proposed product evaluation procedure :

a) A first test can be run at 500 MSPS / 250 MHz Nyquist : about 7.4 Effective Bits (typ) should be obtained.
b) At 1 Gsps / 500 MHz : about 7.0 Effective Bits (typ) should be obtained.
c) At 1 Gsps / 1 GHz and – 1 dB Full Scale analog input, 6.4 bits and – 43 dBc SFDR should be obtained. In the same conditions for – 3 dB Full Scale input, 6.8 bits and – 48 dBc are obtained.

G) The devices operates respectively from 10 MSPS up to 1.4 GSPS in binary output format and 10 MSPS up to 2 GSPS in Gray output format. It is capable of sampling analog input waveforms ranging from DC up to 1.8 GHz;

7. ABSOLUTE MAXIMUM RATINGS

Important : see notes below

Parameter	Symbol	Comments	Value	Unit
Positive supply voltage	V_{CC}		GND to 6	V
Digital negative supply voltage	$DV_{EE\ (*)}$		GND to -5.7	V
Digital positive supply voltage	V_{PLUSD}		GND-0.3 to 2.8	V
Negative supply voltage	$V_{EE\ (*)}$		GND to -6	V
Maximum difference between negative supply voltages	DV_{EE} to V_{EE}		0.3	V
Analog input voltages	V_{IN} or V_{INB}		-1 to +1	V
Maximum difference between V_{IN} and V_{INB}	V_{IN} - V_{INB}		-2 to +2	V
Digital input voltage	V_D	GORB	-0.3 to V_{CC} +0.3	V
Digital input voltage	V_D	DRRB	V_{EE} -0.3 to +0.9	V
Digital output voltage	Vo		V_{PLUSD}-3 to V_{PLUSD} -0.5	V
Clock input voltage	V_{CLK} or V_{CLKB}		-3 to +1.5	V
Maximum difference between V_{CLK} and V_{CLKB}	V_{CLK} - V_{CLKB}		-2 to +2	V
Maximum junction temperature	T_j		+145	°C
Storage temperature	T_{stg}		-65 to +150	°C
Lead temperature (soldering 10s)	T_{leads}		+300	°C

Notes : Absolute maximum ratings are limiting values (referenced to GND=0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability.
The use of a thermal heat sink is mandatory.

(*) : In case only one supply is used for supplying the – 5 V negative power planes, apply the VEED absolute maximum ratings.

8. TSEV8388BFS ELECTRICAL SCHEMATIC

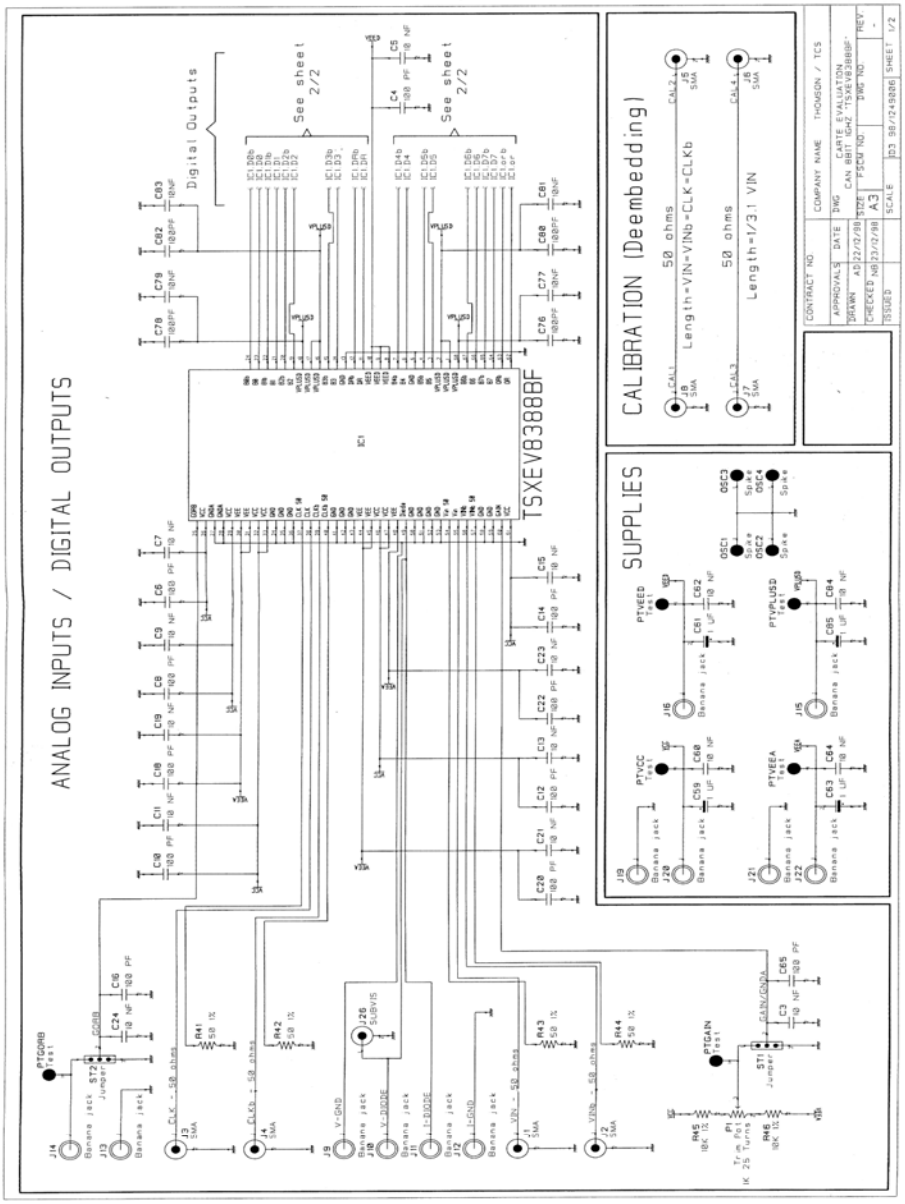


Figure 4 : TSEV8388BFS ELECTRICAL SCHEMATICS

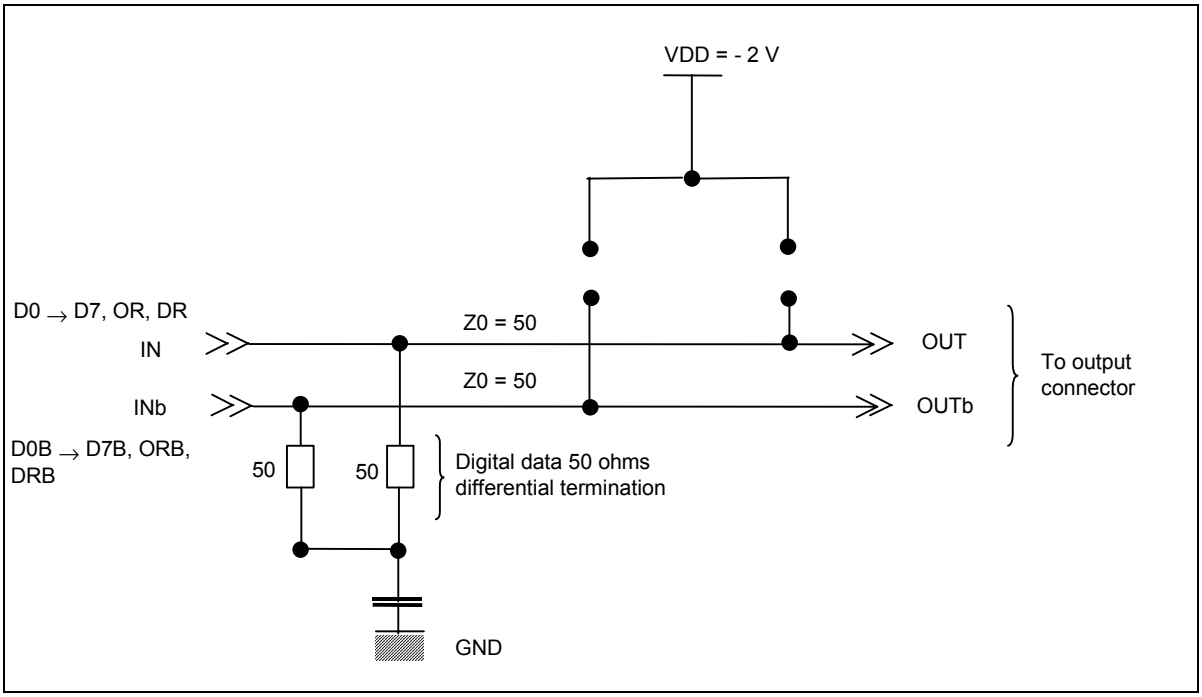


Figure 5 : BOARD DIGITAL OUTPUTS DEFAULT OPTION

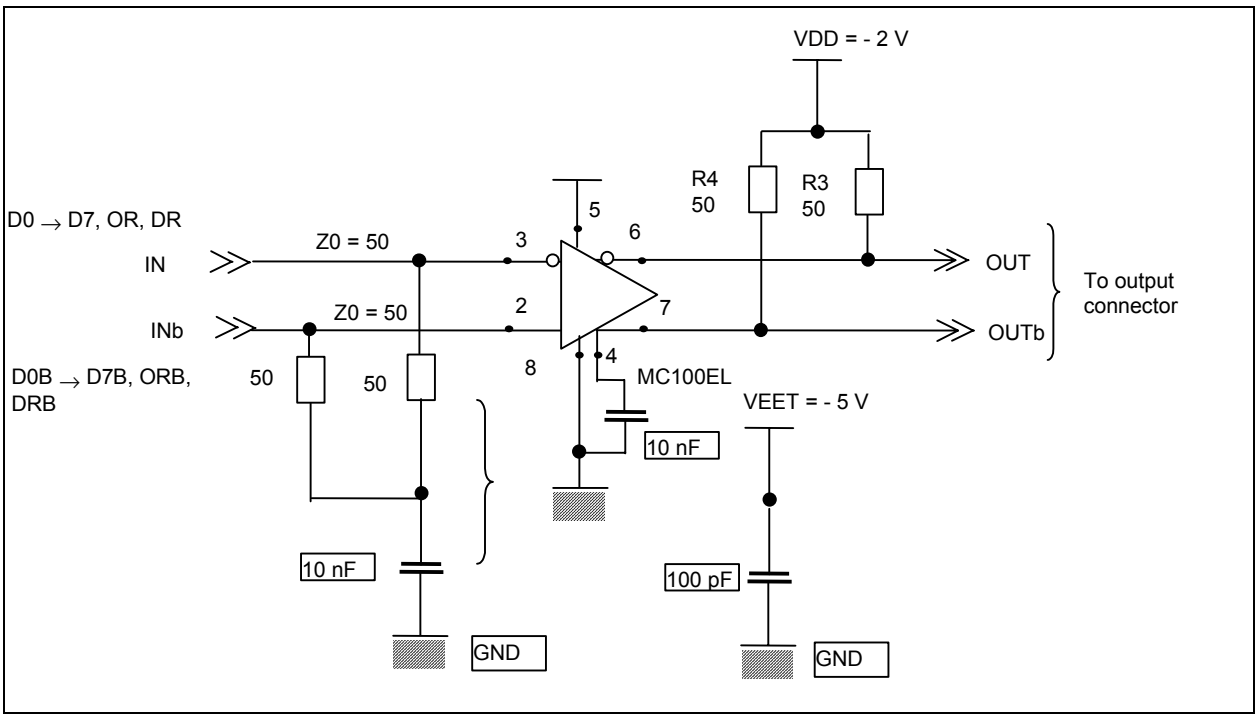


Figure 6 : BOARD DIGITAL OUTPUTS OPTION USING MC100EL16 DIFFERENTIAL RECEIVERS

9. EVALUATION BOARD SCHEMATIC

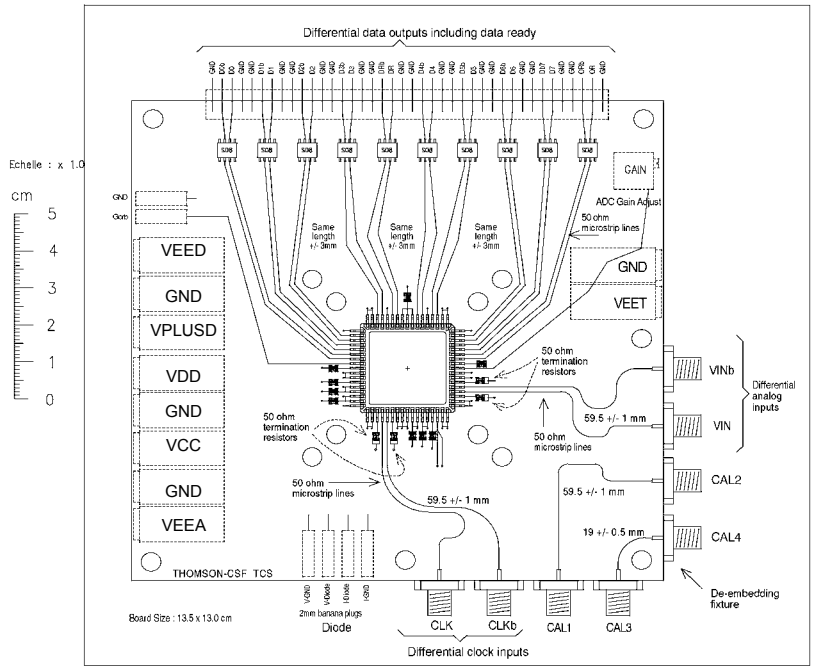


Figure 7 : TSEV8388BFS EVALUATION BOARD SCHEMATIC

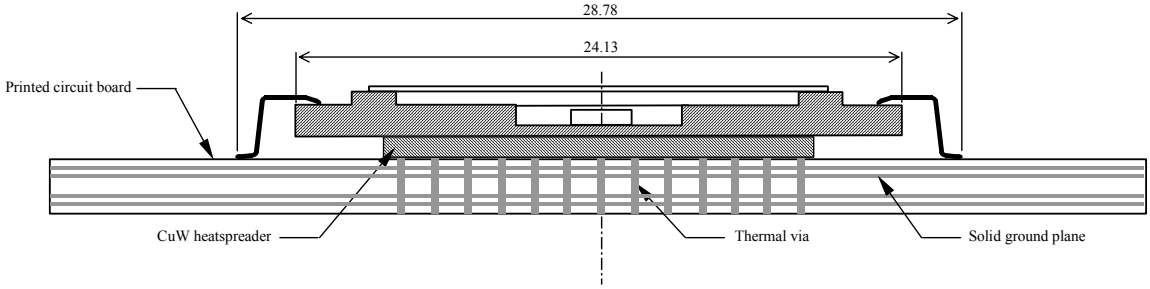


Figure 8 : Rth CQFP868 ASSEMBLY WITH THERMAL HEATSINK

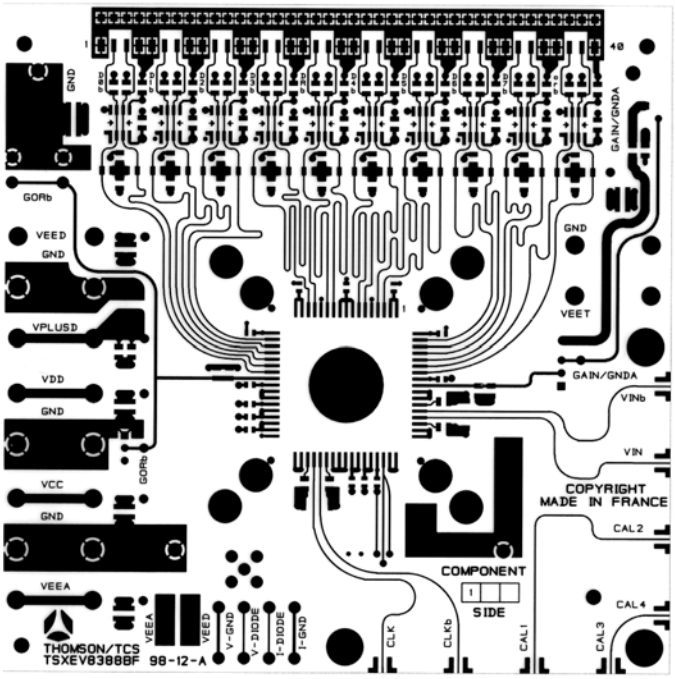


Figure 9 : COMPONENT SIDE DESCRIPTION

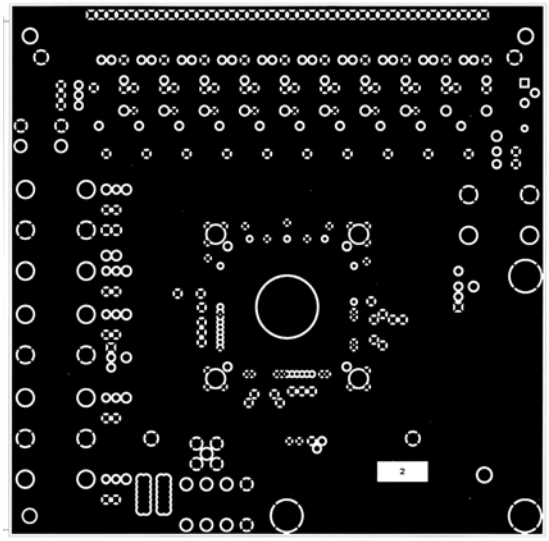


Figure 10 : GROUND PLANE

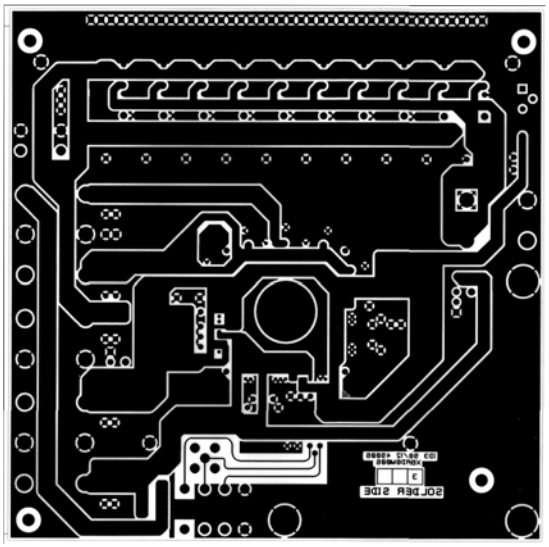


Figure 11 : POWER SUPPLIES PLANES

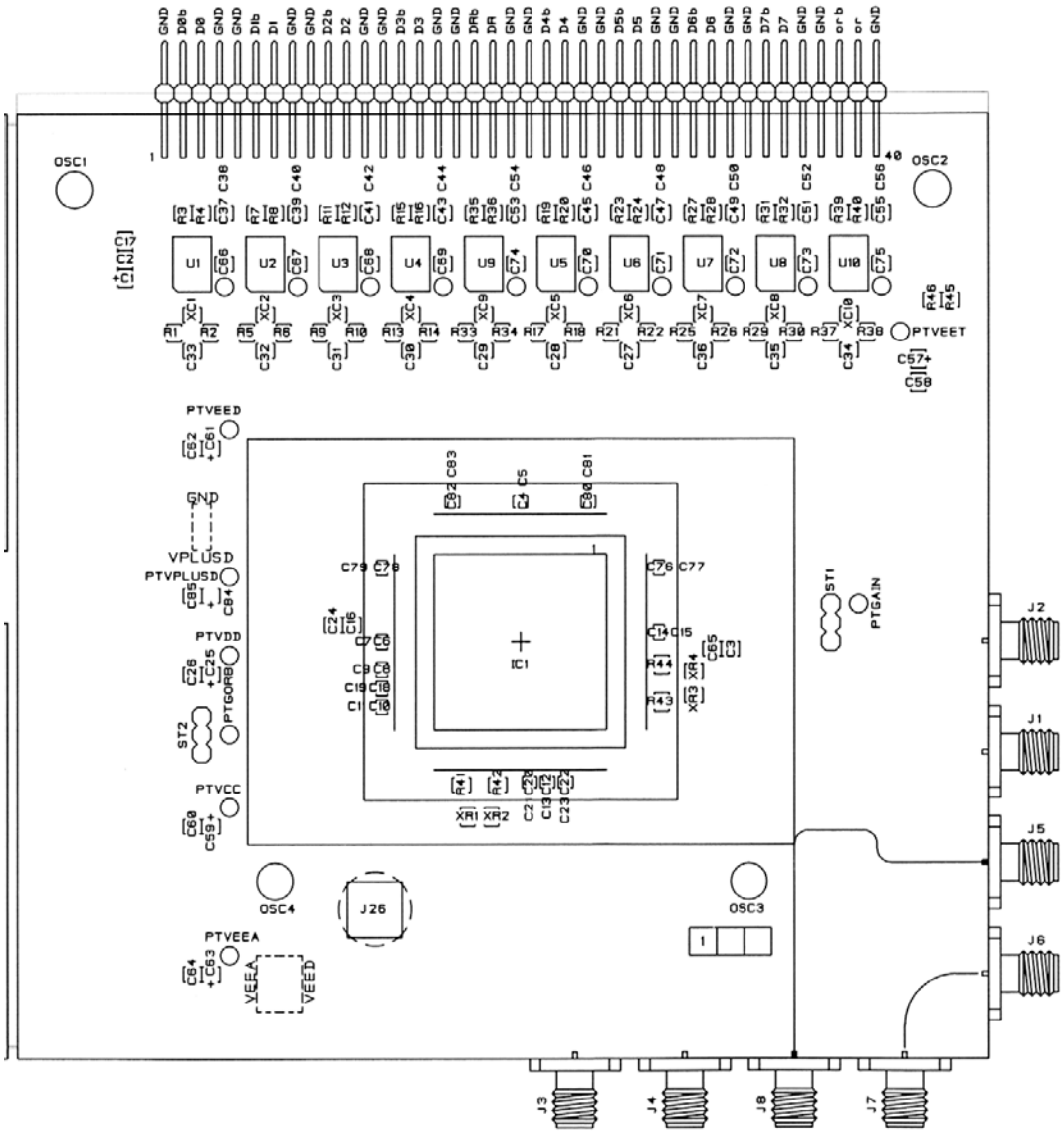


Figure 12 : TSEV8388BFS EVALUATION BOARD : COMPONENTS PLACEMENT

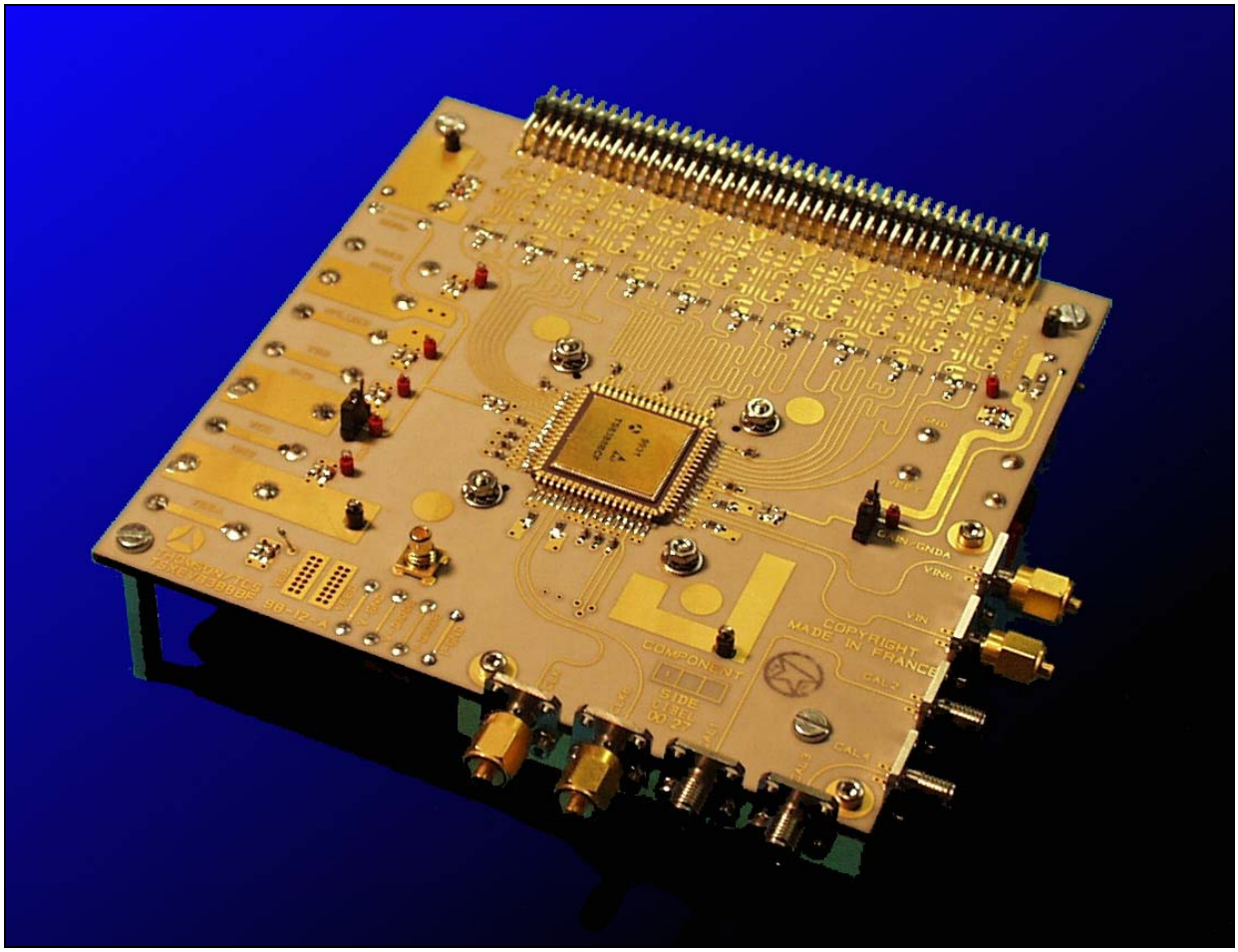


Figure 13 : TSEV8388BFS EVALUATION BOARD : TOP VIEW (SIGNAL SIDE)

10. TEST BENCH DESCRIPTION

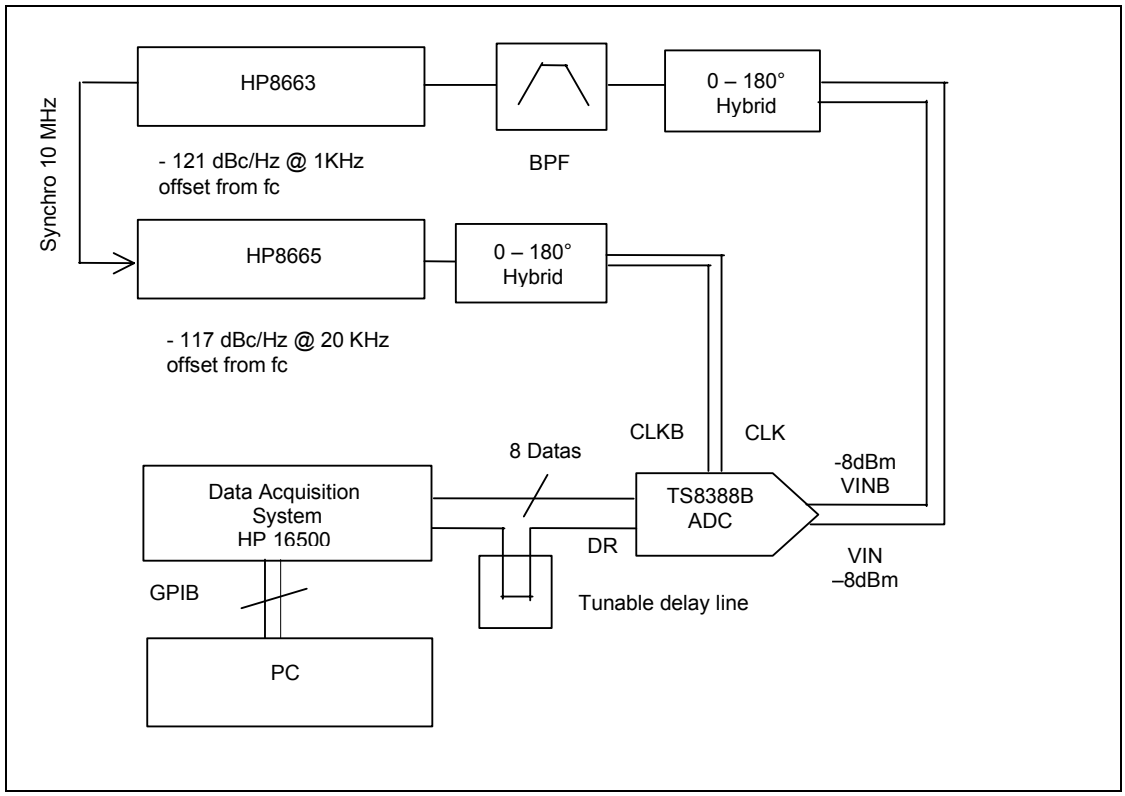


Figure 14 DIFFERENTIAL ANALOG AND CLOCK INPUTS CONFIGURATION

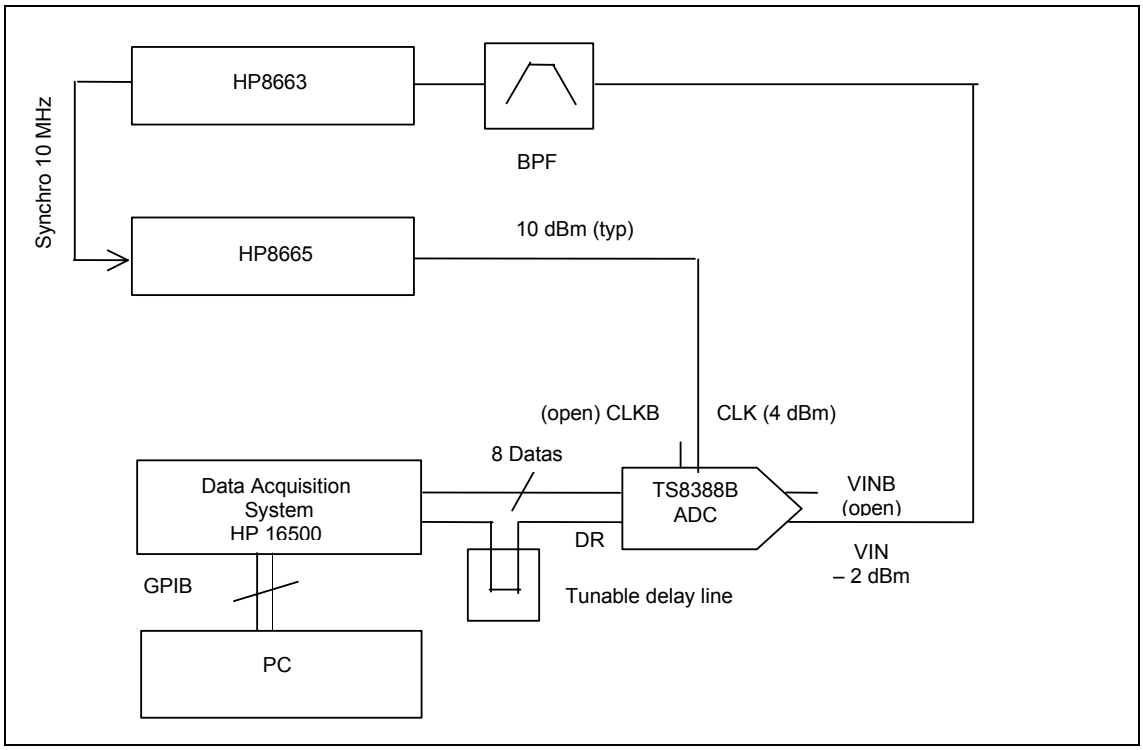
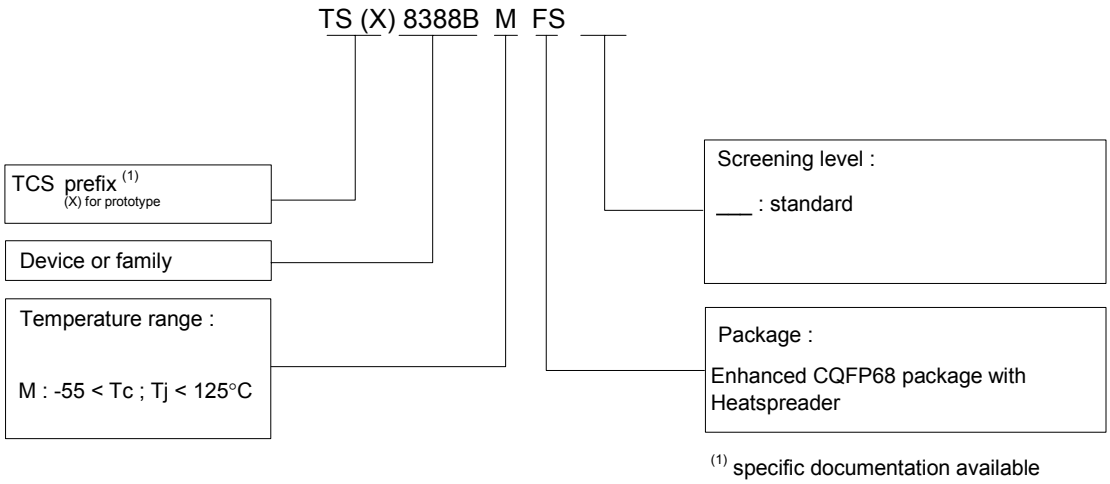


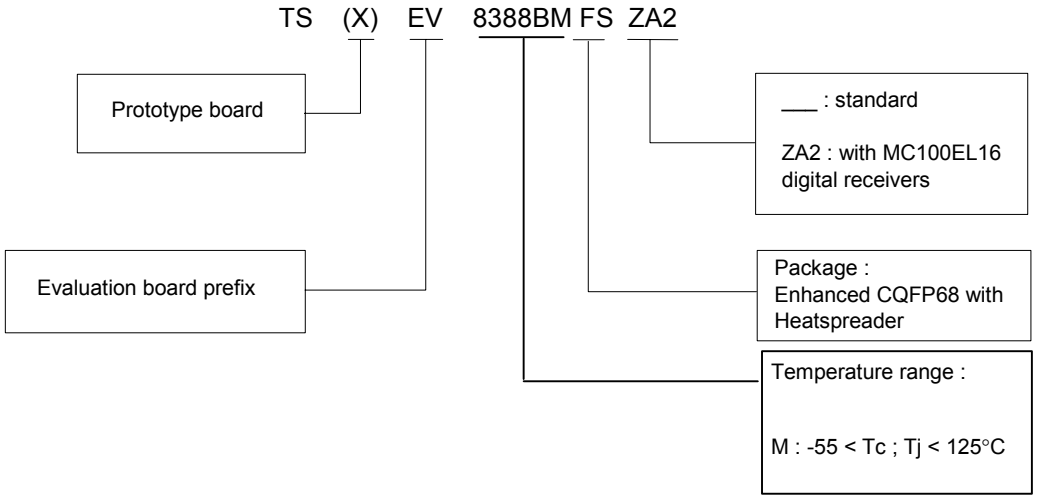
Figure 15 SINGLE6ENDED ANALOG AND CLOCK INPUT CONFIGURATION

11. ORDERING INFORMATION

11.1. PACKAGE DEVICE



11.2. EVALUATION BOARD



The evaluation board is delivered with an ADC and includes the heat sink.

APPENDIX

DATASHEET STATUS		VALIDITY
Objective specification	This datasheet contains target and goal specification for discussion with customer and application validation.	Before design phase.
Target specification	This datasheet contains target and goal specification for product development.	Valid during the design phase.
Preliminary specification Alpha-site	This datasheet contains preliminary data. Additional data may be published later ; could include simulation results.	Valid before the characterization phase.
Preliminary specification Beta-site	This datasheet contains also characterization results.	Valid before the industrialization phase.
Product specification	This datasheet contains final product specifiaction.	Valid for production purpose.
Limiting values		
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.		
Application information		
Where application information is given, it is advisory and does not form part of the specification.		

LIFE SUPPORT APPLICATIONS

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