

## Features

- Integer Unit Based on SPARC V7 High-performance RISC Architecture
- Optimized Integrated 32/64-bit Floating-point Unit
- On-chip Peripherals:
  - EDAC and Parity Generator and Checker
  - Memory Interface:
    - Chip Select Generator
    - Waitstate Generation
    - Memory Protection
  - DMA Arbiter
  - Timers:
    - General Purpose Timer (GPT)
    - Real-time Clock Timer (RTCT)
    - Watchdog Timer (WDT)
  - Interrupt Controller With 5 External Inputs
  - General Purpose Interface (GPI)
  - Dual UART
- Speed Optimized Code RAM Interface
- 8- or 40-bit boot-PROM (Flash) Interface
- IEEE 1149.1 Test Access Port (TAP) for Debugging and Test Purposes
- Fully Static Design
- Performance: 20 MIPs/5 MFlops (double precision) at SYSCLK = 25 MHz
- Core Consumption: 1.0W typ. at 20 MIPs/0.7W typ. at 10 MIPs
- Operating Range: 4.5V to 5.5V (3.3V Capability) -55°C to +125°C
- Total Dose Radiation Capability (Parametric and Functional): 300 KRADs (Si)
- SEU Event Rate Better than  $1E^{-8}$  Error/Component/Day (Worst Case)
- Latch-up Immunity Better than (LET) 100 MeV-cm<sup>2</sup>/mg
- Quality Grades: ESA SCC, QML Q or V
- Package: 256 MQFPF; Bare Die

## Description

The TSC695F (ERC32 Single-Chip) is a highly integrated, high-performance 32-bit RISC embedded processor implementing the SPARC architecture V7 specification. It has been developed with the support of the ESA (European Space Agency), and offers a full development environment for embedded space applications.

The processor is manufactured using the Atmel 0.5  $\mu$ m radiation tolerant ( $\geq 300$  KRADs (Si)) CMOS enhanced process (RTP). It can operate at a low voltage for optimized power consumption. It has been specially designed for space, as it has on-chip concurrent transient and permanent error detection.

The TSC695F includes an on-chip Integer Unit (IU), a Floating Point Unit (FPU), a Memory Controller and a DMA arbiter. For real-time applications, the TSC695F offers a high security watchdog, two timers, an interrupt controller, parallel and serial interfaces. Fault tolerance is supported using parity on internal/external buses and an EDAC on the external data bus. The design is highly testable with the support of an On-Chip Debugger (OCD), and a boundary scan through JTAG interface.



## Rad-Hard 32-bit SPARC Embedded Processor

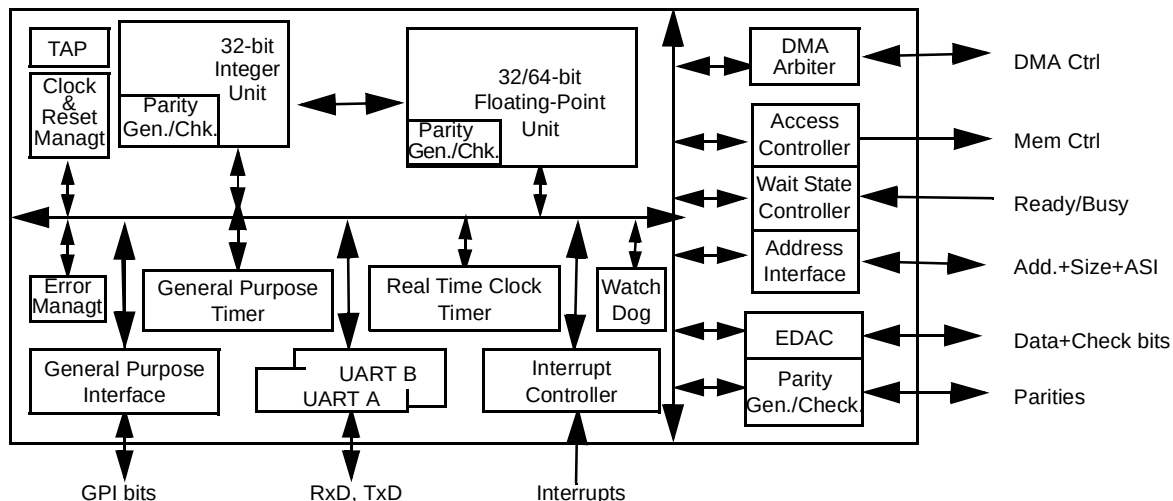
## TSC695F

Rev. 4118F-AERO-04/02



## Block Diagram

Figure 1. TSC695F Block Diagram



## Pin Descriptions

For pin assignment, refer to package section.

Table 1. Pin Descriptions

| Signal     | Type | Active | Description                                   |                            |
|------------|------|--------|-----------------------------------------------|----------------------------|
| RA[31:0]   | I/O  |        | 32-bit registered address bus                 | Output buffer: 400 pF      |
| RAPAR      | I/O  | High   | Registered address bus parity                 | -                          |
| RASI[3:0]  | I/O  |        | 4-bit registered address space identifier     | -                          |
| RSIZE[1:0] | I/O  |        | 2-bit registered bus transaction size         | -                          |
| RASPAR     | I/O  | High   | Registered ASI and SIZE parity                | -                          |
| CPAR       | I/O  | High   | Control bus parity                            | -                          |
| D[31:0]    | I/O  |        | 32-bit data bus                               | -                          |
| CB[6:0]    | I/O  |        | 7-bit check-bit bus                           | -                          |
| DPAR       | I/O  | High   | Data bus parity                               | -                          |
| RLDSTO     | I/O  | High   | Registered atomic load-store                  | -                          |
| ALE        | O    | Low    | Address latch enable                          | -                          |
| DXFER      | I/O  | High   | Data transfer                                 | -                          |
| LOCK       | I/O  | High   | Bus lock                                      | -                          |
| RD         | I/O  | High   | Read access                                   | -                          |
| WE         | I/O  | Low    | Write enable                                  | -                          |
| WRT        | I/O  | High   | Advanced write                                | -                          |
| MHOLD      | O    | Low    | Memory bus hold                               | MHOLD+FHOLD<br>+BHOLD+FCCV |
| MDS        | O    | Low    | Memory data strobe                            | -                          |
| MEXC       | O    | Low    | Memory exception                              | -                          |
| PROM8      | I    | Low    | Select 8-bit wide PROM                        | -                          |
| BA[1:0]    | O    |        | Latched address used for 8-bit wide boot PROM | -                          |
| ROMCS      | O    | Low    | PROM chip select                              | -                          |
| ROMWRT     | I    | Low    | ROM write enable                              | -                          |
| MEMCS[9:0] | O    | Low    | Memory chip select                            | Output buffer: 400 pF      |
| MEMWR      | O    | Low    | Memory write strobe                           | Output buffer: 400 pF      |

Table 1. Pin Descriptions (Continued)

| Signal                         | Type | Active | Description                          |                                                            |
|--------------------------------|------|--------|--------------------------------------|------------------------------------------------------------|
| $\overline{\text{OE}}$         | O    | Low    | Memory output enable                 | Output buffer: 400 pF                                      |
| $\overline{\text{BUFFEN}}$     | O    | Low    | Data buffer enable                   | -                                                          |
| $\overline{\text{DDIR}}$       | O    | High   | Data buffer direction                | -                                                          |
| $\overline{\text{DDIR}}$       | O    | Low    | Data buffer direction                | -                                                          |
| $\overline{\text{IOSEL}}[3:0]$ | O    | Low    | I/O chip select                      | -                                                          |
| $\overline{\text{IOWR}}$       | O    | Low    | I/O and exchange memory write strobe | -                                                          |
| $\overline{\text{EXMCS}}$      | O    | Low    | Exchange memory chip select          | -                                                          |
| $\overline{\text{BUSRDY}}$     | I    | Low    | Bus ready                            | -                                                          |
| $\overline{\text{BUSERR}}$     | I    | Low    | Bus error                            | -                                                          |
| $\overline{\text{DMAREQ}}$     | I    | Low    | DMA request                          | -                                                          |
| $\overline{\text{DMAGNT}}$     | O    | Low    | DMA grant                            | -                                                          |
| $\overline{\text{DMAAS}}$      | I    | High   | DMA address strobe                   | -                                                          |
| $\overline{\text{DRDY}}$       | O    | Low    | Data ready during DMA access         | -                                                          |
| $\overline{\text{IUERR}}$      | O    | Low    | IU error                             | -                                                          |
| $\overline{\text{CPUHALT}}$    | O    | Low    | Processor (IU & FPU) halt and freeze | -                                                          |
| $\overline{\text{SYSERR}}$     | O    | Low    | System error                         | -                                                          |
| $\overline{\text{SYSHALT}}$    | I    | Low    | System halt                          | -                                                          |
| $\overline{\text{SYSAV}}$      | O    | High   | System availability                  | -                                                          |
| $\overline{\text{NOPAR}}$      | I    | Low    | No parity                            | -                                                          |
| $\overline{\text{INULL}}$      | O    | High   | Integer unit nullify cycle           | -                                                          |
| $\overline{\text{INST}}$       | O    | High   | Instruction fetch                    | Used to check the execute stage of IU instruction pipeline |
| $\overline{\text{FLUSH}}$      | O    | High   | FPU instruction flush                |                                                            |
| $\overline{\text{DIA}}$        | O    | High   | Delay instruction annulled           |                                                            |
| $\overline{\text{RTC}}$        | O    | High   | Real Time Clock Counter output       | -                                                          |
| $\text{RxA/RxB}$               | I    |        | Receive data UART "A" and "B"        | Input trigger                                              |
| $\text{TxA/TxB}$               | O    |        | Transmit data UART "A" and "B"       | -                                                          |
| $\text{GPI}[7:0]$              | I/O  |        | GPI input/output                     | Input trigger                                              |
| $\text{GPIINT}$                | O    | High   | GPI interrupt                        | -                                                          |
| $\text{EXTINT}[4:0]$           | I    |        | External interrupt                   | Input trigger                                              |
| $\text{EXTINTACK}$             | O    | High   | External interrupt acknowledge       | -                                                          |
| $\text{IWDE}$                  | I    | High   | Internal watch dog enable            | -                                                          |
| $\text{EWDINT}$                | I    | High   | External watch dog input interrupt   | Input trigger                                              |
| $\text{WDCLK}$                 | I    |        | Watch dog clock                      | -                                                          |
| $\text{CLK2}$                  | I    |        | Double frequency clock               | -                                                          |
| $\text{SYSCLK}$                | O    |        | System clock                         | -                                                          |
| $\overline{\text{RESET}}$      | O    | Low    | Output reset                         | -                                                          |
| $\overline{\text{SYSRESET}}$   | I    | Low    | System input reset                   | Input trigger                                              |
| $\text{TMODE}[1:0]$            | I    |        | Factory test mode                    | Functional mode=00                                         |
| $\text{DEBUG}$                 | I    | High   | Software debug mode                  | -                                                          |
| $\text{TCK}$                   | I    |        | Test (JTAG) clock                    | -                                                          |
| $\overline{\text{TRST}}$       | I    | Low    | Test (JTAG) reset                    | pull-up $\approx 37 \text{ k}\Omega$                       |
| $\text{TMS}$                   | I    |        | Test (JTAG) mode select              | pull-up $\approx 37 \text{ k}\Omega$                       |
| $\text{TDI}$                   | I    |        | Test (JTAG) data input               | pull-up $\approx 37 \text{ k}\Omega$                       |
| $\text{TDO}$                   | O    |        | Test (JTAG) data output              | -                                                          |
| $\text{VCCI/VSSI}$             |      |        | Main internal power                  | -                                                          |
| $\text{VCCO/VSSO}$             |      |        | Output driver power                  | -                                                          |

Note: If not specified, the output buffer type is 150 pF, the input buffer type is TTL



## Product Description

### Integer Unit

The IU is designed for highly dependable space and military applications, and includes support for error detection. The RISC architecture makes the creation of a processor that can execute instructions at a rate approaching one instruction per processor clock possible.

To achieve that rate of execution, the IU employs a four-stage instruction pipeline that permits parallel execution of multiple instructions.

- Fetch - The processor outputs the instruction address to fetch the instruction.
- Decode - The instruction is placed in the instruction register and is decoded. The processor reads the operands from the register file and computes the next instruction address.
- Execute - The processor executes the instruction and saves the results in temporary registers. Pending traps are prioritized and internal traps are taken during this stage.
- Write - If no trap is taken, the processor writes the result to the destination register.

All four stages operate in parallel, working on up to four different instructions at a time. A basic "single-cycle" instruction enters the pipeline and completes in four cycles.

By the time it reaches the write stage, three more instructions have entered and are moving through the pipeline behind it. So, after the first four cycles, a single-cycle instruction exits the pipeline and a single-cycle instruction enters the pipeline on every cycle. Of course, a "single-cycle" instruction actually takes four cycles to complete, but they are called single cycle because with this type of instruction the processor can complete one instruction per cycle after the initial four-cycle delay.

### Floating-point Unit

The FPU is designed to provide execution of single and double-precision floating-point instructions concurrently with execution of integer instructions by the IU. The FPU is compliant to the ANSI/IEEE-754 (1985) floating-point standard.

The FPU is designed for highly dependable space and military applications, and includes support for concurrent error detection and testability.

The FPU uses a four stage instruction pipeline consisting of fetch, decode, execute and write stages (F, D, E and W). The fetch unit captures instructions and their addresses from the data and address busses. The decode unit contains logic to decode the floating-point instruction opcodes. The execution unit handles all instruction execution. The execution unit includes a floating-point queue (FP queue), which contains stored floating-point operate (FPop) instructions under execution and their addresses. The execution unit controls the load unit, the store unit, and the datapath unit. The FPU depends upon the IU to access all addresses and control signals for memory access. Floating-point loads and stores are executed in conjunction with the IU, which provides addresses and control signals while the FPU supplies or stores the data. Instruction fetch for integer and floating-point instructions is provided by the IU.

The FPU provides three types of registers: f registers, FSR, and the FP queue. The FSR is a 32-bit status and control register. It keeps track of rounding modes, floating-point trap types, queue status, condition codes, and various IEEE exception information. The floating-point queue contains the floating-point instruction currently under execution, along with its corresponding address.



## Instruction Set

TSC695F instructions fall into six functional categories: load/store, arithmetic/logical/shift, control transfer, read/write control register, floating-point, and miscellaneous. Please refer to SPARC V7 Instruction-set Manual.

Note: The execution of IFLUSH will cause an illegal instruction trap.

## On-chip Peripherals

### Memory Interface

The TSC695F is designed to allow easy interfacing to internal/external memory resources.

**Table 2.** Memory Mapping

| Memory Contents   | Start Address | Size (bytes)    | Data Size and Parity Options                 |                                          |
|-------------------|---------------|-----------------|----------------------------------------------|------------------------------------------|
| Boot PROM         | 0x00000000    | 128K → 16M      | 8-bit mode                                   | No parity/-No EDAC/-Only byte write      |
|                   |               |                 | 40-bit mode                                  | Parity + EDAC mandatory/-Only word write |
| Extended PROM     | 0x01000000    | Max: 15M        | 8-bit mode                                   | No parity/-No EDAC/-Only byte write      |
|                   |               |                 | 40-bit mode                                  | Parity + EDAC mandatory/-Only word write |
| Exchange Memory   | 0x01F00000    | 4k → 512k       | Parity + EDAC option/-Only word write        |                                          |
| System Registers  | 0x01F80000    | 512K (124 used) | Parity/-Only word read/write access          |                                          |
| RAM (8 blocks)    | 0x02000000    | 8*32K → 8*4M    | Parity + EDAC option/-All data sizes allowed |                                          |
| Extended RAM      | 0x04000000    | Max: 192M       |                                              |                                          |
| I/O Area 0        | 0x10000000    | 0 → 16M         |                                              |                                          |
| I/O Area 1        | 0x11000000    | 0 → 16M         |                                              |                                          |
| I/O Area 2        | 0x12000000    | 0 → 16M         |                                              |                                          |
| I/O Area 3        | 0x13000000    | 0 → 16M         | Parity option/-All data sizes allowed        |                                          |
| Extended I/O Area | 0x14000000    | Max: 1728M      |                                              |                                          |
| Extended General  | 0x80000000    | Max: 2G         | No parity/-All data sizes allowed            |                                          |

### System Registers

The system registers are only writeable by IU in the supervisor mode or by DMA during halt mode.

**Table 3.** System Registers Address Map

| System Register Name          |        | Address      |
|-------------------------------|--------|--------------|
| System Control Register       | SYSCTR | 0x 01F8 0000 |
| Software Reset                | SWRST  | 0x 01F8 0004 |
| Power Down                    | PDOWN  | 0x 01F8 0008 |
| System Fault Status Register  | SYSFSR | 0x 01F8 00A0 |
| Failing Address Register      | FAILAR | 0x 01F8 00A4 |
| Error & Reset Status Register | ERRRSR | 0x 01F8 00B0 |
| Test Control Register         | TESCTR | 0x 01F8 00D0 |

**Table 3. System Registers Address Map (Continued)**

| System Register Name                             |         | Address      |
|--------------------------------------------------|---------|--------------|
| Memory Configuration Register                    | MCNFR   | 0x 01F8 0010 |
| I/O Configuration Register                       | IOCNFR  | 0x 01F8 0014 |
| Waitstate Configuration Register                 | WSCNFR  | 0x 01F8 0018 |
| Access Protection Segment 1 Base Register        | APS1BR  | 0x 01F8 0020 |
| Access Protection Segment 1 End Register         | APS1ER  | 0x 01F8 0024 |
| Access Protection Segment 2 Base Register        | APS2BR  | 0x 01F8 0028 |
| Access Protection Segment 2 End Register         | APS2ER  | 0x 01F8 002C |
| Interrupt Shape Register                         | INTSHR  | 0x 01F8 0044 |
| Interrupt Pending Register                       | INTPDR  | 0x 01F8 0048 |
| Interrupt Mask Register                          | INTMKR  | 0x 01F8 004C |
| Interrupt Clear Register                         | INTCLR  | 0x 01F8 0050 |
| Interrupt Force Register                         | INTFCR  | 0x 01F8 0054 |
| Watchdog Timer Register                          | WDOGTR  | 0x 01F8 0060 |
| Watchdog Timer Trap Door Set                     | WDOGST  | 0x 01F8 0064 |
| Real Time Clock Timer <Counter> Register         | RTCCR   | 0x 01F8 0080 |
| Real Time Clock Timer <Scaler> Register          | RTCSR   | 0x 01F8 0084 |
| General Purpose Timer <Counter> Register         | GPTCR   | 0x 01F8 0088 |
| General Purpose Timer <Scaler> Register          | GPTSR   | 0x 01F8 008C |
| Timers Control Register                          | TIMCTR  | 0x 01F8 0098 |
| General Purpose Interface Configuration Register | GPICNFR | 0x 01F8 00A8 |
| General Purpose Interface Data Register          | GPIDATR | 0x 01F8 00AC |
| UART "A" Rx & Tx Register                        | UARTAR  | 0x 01F8 00E0 |
| UART "B" Rx & Tx Register                        | UARTBR  | 0x 01F8 00E4 |
| UART Status Register                             | UARTSR  | 0x 01F8 00E8 |

### Wait-state and Time-out Generator

It is possible to control the wait state generation by programming a Waitstate Configuration Register. The maximum programmable number of wait-states is applied by default at reset.

It is possible to program the number of wait states for the following combinations:

- RAM read and write
- PROM read and write (i.e. EEPROM or Flash write)
- Exchange Memory read/write
- Four individual I/O peripherals read/write

A bus time-out function of 256 system clock cycles is provided for the bus ready controlled memory areas, i.e. the Extended PROM, Exchange Memory, Extended RAM, Extended I/O and the Extended General areas.

**EDAC** The TSC695F includes a 32-bit EDAC (Error Detection And Correction). Seven bits (CB[6:0]) are used as check bits over the data bus. The Data Bus Parity signal (DPA) is used to check and generate the odd parity over the 32-bit data bus. This means that altogether 40 bits are used when the EDAC is enabled.

The TSC695F EDAC uses a 7-bit Hamming code which detects any double bit error on the 40-bit bus as a non-correctable error. In addition, the EDAC detects all bits stuck-at-one and stuck-at-zero failure for any nibble in the data word as a non-correctable error. Stuck-at-one and stuck-at-zero for all 32 bits of the data word is also detected as a non-correctable error.

**Memory and I/O Parity** The TSC695F handles parity towards memory and I/O in a special way. The processor can be programmed to use no parity, only parity or parity and EDAC protection towards memory and to use parity or no towards I/O. The signal used for the parity bit is DPA.

**Memory Redundancy** Programming the Memory Configuration Register, the TSC695F provides chip selects for two redundant memory banks for replacement of faulty banks.

**Memory Access Protection**

- Unimplemented Areas - Access to all unimplemented memory areas are handled by the TSC695F and detected as illegal.
- RAM Write Access Protection - The TSC695F can be programmed to detect and mask write accesses in any part of the RAM. The protection scheme is enabled only for data area, not for the instruction area. The programmable write access protection is based on two segments.
- Boot PROM Write Protection - The TSC695F supports a qualified PROM write for an 8-bit wide PROM and/or for a 40-bit wide PROM.

## DMA

**DMA Interface** The TSC695F supports Direct Memory Access (DMA). The DMA unit requests access to the processor bus by asserting the DMA request signal ( $\overline{\text{DMAREQ}}$ ). When the DMA unit receives the  $\overline{\text{DMAGNT}}$  signal in response, the processor bus is granted. In case the processor is in the power-down mode the processor is permanent tri-stated, and a  $\overline{\text{DMAREQ}}$  will directly give a  $\overline{\text{DMAGNT}}$ . The TSC695F includes a DMA session time-out function.

**Bus Arbiter** The TSC695F always has the lowest priority on the system bus.

**Traps** A trap is a vectored transfer of control to the supervisor through a special trap table that contains the first four instructions of each trap handler. The base address of the table is established by supervisor and the displacement, within the table, is determined by the trap type. Two categories of traps can appear.



## Synchronous Traps

Table 4. Synchronous Traps

| Trap                                               |                                  | Priority |     | Trap Type (tt) | Comments                                                                                                                                                                                          |
|----------------------------------------------------|----------------------------------|----------|-----|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Reset                                              |                                  | 1        |     | -              | Sources: SYSRESET* pin<br>software reset<br>watchdog reset<br>IU or System error reset                                                                                                            |
| Hardware Error                                     | Non-restartable, imprecise error | 2        | 2.1 | 64h            | Severe error requiring a re-boot<br>TSC695F enters (if not masked) in halt or reset mode.                                                                                                         |
|                                                    | Non-restartable, precise error   |          | 2.2 | 62h            | Error not removable, PC & nPC OK<br>TSC695F enters (if not masked) in halt or reset mode.                                                                                                         |
|                                                    | Register file error              |          | 2.3 | 65h            | Special case of non-restartable, precise error.<br>TSC695F enters (if not masked) in halt or reset mode.                                                                                          |
|                                                    | Restartable, late error          |          | 2.4 | 63h            | Retrying instruction but PC & nPC have to be re-adjusted<br>TSC695F enters (if not masked) in halt or reset mode.                                                                                 |
|                                                    | Restartable, precise error       | 2.5      | 61h |                | Retrying instruction<br>TSC695F enters (if not masked) in halt or reset mode.                                                                                                                     |
| Instruction access<br>(Error on instruction fetch) |                                  | 3        |     | 01h            | Parity error on control bus<br>Parity error on data bus<br>Parity error on address bus<br>Access to protected or unimplemented area<br>Uncorrectable error in memory<br>Bus time out<br>Bus error |
| Illegal Instruction                                |                                  | 4        |     | 02h            | -                                                                                                                                                                                                 |
| Privileged instruction                             |                                  | 5        |     | 03h            | -                                                                                                                                                                                                 |
| FPU disabled                                       |                                  | 6        |     | 04h            | -                                                                                                                                                                                                 |
| Window                                             | Overflow                         | 7        |     | 05h            | During SAVE instruction or trap taken                                                                                                                                                             |
|                                                    | Underflow                        |          |     | 06h            | During RESTORE instruction or RETT instruction                                                                                                                                                    |
| Memory address not aligned                         |                                  | 8        |     | 07h            | -                                                                                                                                                                                                 |
| FPU exception                                      | Non-restartable error            | 9        | 9.1 |                | Severe error, cannot restart the instruction.                                                                                                                                                     |
|                                                    | Data bus error                   |          | 9.2 |                | Parity error on FPU data bus.                                                                                                                                                                     |
|                                                    | Restartable error                |          | 9.3 |                | Can be removed restarting the instruction.                                                                                                                                                        |
|                                                    | Sequence error                   |          | 9.4 |                | -                                                                                                                                                                                                 |
|                                                    | Unimplemented FPop               |          | 9.5 |                | -                                                                                                                                                                                                 |
|                                                    | IEEE exceptions:                 | 9.6      | 08h |                | Invalid operation<br>Division by zero<br>Overflow<br>Underflow<br>Inexact                                                                                                                         |

**Table 4. Synchronous Traps (Continued)**

| Trap                                          | Priority | Trap Type (tt) | Comments                                                      |
|-----------------------------------------------|----------|----------------|---------------------------------------------------------------|
| Data access exception<br>(Error on data load) | 10       | 09h            | Idem "instruction access"<br>System register access violation |
| Tag overflow                                  | 11       | 0Ah            | TADDccTV and TSUBccTV instructions                            |
| Trap instructions                             | 12       | 80h to FFh     | Trap on integer condition codes (Ticc)                        |

**Table 5. Interrupts or Asynchronous Traps**

| Trap                        |                                 | Priority | Trap Type (tt) | Comments                                                                                           |
|-----------------------------|---------------------------------|----------|----------------|----------------------------------------------------------------------------------------------------|
| Watchdog time-out           |                                 | 13       | 1Fh            | Internal or external (EWDINT pin)                                                                  |
| External INT 4              |                                 | 14       | 1Eh            | EXTINTAK on only one of EXTINT[4:0]                                                                |
| Real time clock timer       |                                 | 15       | 1Dh            | -                                                                                                  |
| General purpose timer       |                                 | 16       | 1Ch            | -                                                                                                  |
| External INT 3              |                                 | 17       | 1Bh            | EXTINTAK on only one of EXTINT[4:0]                                                                |
| External INT 2              |                                 | 18       | 1Ah            | EXTINTAK on only one of EXTINT[4:0]                                                                |
| DMA time-out                |                                 | 19       | 19h            | -                                                                                                  |
| DMA access error            |                                 | 20       | 18h            | -                                                                                                  |
| UART Error                  |                                 | 21       | 17h            | -                                                                                                  |
| Correctable error in memory |                                 | 22       | 16h            | Data read OK but source not updated                                                                |
| UART B                      | Data ready<br>Transmitter ready | 23       | 15h            | -                                                                                                  |
| UART A                      | Data ready<br>Transmitter ready | 24       | 14h            | -                                                                                                  |
| External INT 1              |                                 | 25       | 13h            | EXTINTAK on only one of EXTINT[4:0]                                                                |
| External INT 0              |                                 | 26       | 12h            | EXTINTAK on only one of EXTINT[4:0]                                                                |
| Masked hardware errors      |                                 | 27       | 11h            | Logical OR of:<br>IU hardware error masked<br>IU error mode masked<br>System hardware error masked |

It is possible to mask each individual interrupt (except Watchdog time-out). The interrupts in the Interrupt Pending Register are cleared automatically when the interrupt is acknowledged.

By programming the Interrupt Shape Register, it is possible to define the external interrupts to be either active low or active high and to define the external interrupts to be either edge or level sensitive.

## Timers

In software debug mode the timers are controlled by a system register bit and the external pin DEBUG.

### General Purpose Timer

The General Purpose Timer (GPT) provides, in addition to a generalized counter function, a mechanism for setting the step size in which actual time counts are performed.

GPT is clocked by the internal system clock. They are possible to program to be either of single-shot type or periodical type and in both cases generate an interrupt when the delay time has elapsed. The current value of the scaler and counter of the GPT can be read.

### Real Time Clock Timer

The only functional differences between the two timers are that the Real Time Clock Timer (RTCT) has an 8-bit scaler (16-bit scaler for GPT) and that the RTCT interrupt has higher priority than the GPT interrupt.

RTCT information is available on RTC output pin.

### Watchdog Timer

Setting the external pin IWDE to Vcc enables the internal watchdog timer. Otherwise the watchdog function must be externally provided.

The watchdog is supplied from a separate external input (WDCLK). After reset, the timer is enabled and starts running with the maximum range. If the timer is not refreshed (reprogrammed) before the counter reaches zero value, an interrupt is sent. Simultaneously, the timer starts counting a reset time-out period. If the timer is not acknowledged before the reset time-out period elapses, a reset is applied to TSC695F.

## UARTs

Two full duplex asynchronous receiver transmitters (UART) are included. In software debug mode the UART's are controlled by system register bits.

The data format of the UART's is eight bits. It is possible to choose between even or odd parity, or no parity, and between one and two stop bits. The UART's provide double buffering, i.e. each UART consists of a transmitter holding register, a receiver holding register, a transmitter shift register, and a receiver shift register. Each of these registers are 8-bit wide. For each UART a RX and TX Register is provided. The UART's generate an interrupt each time a byte has been received or a byte has been sent. There is another interrupt to indicate errors.

The baud rate of both the UART's is programmable. The clock is derived either from the system clock or can use the watchdog clock.

### General Purpose Interface

The General Purpose Interface (GPI) is an 8-bit parallel I/O port. Each pin can be configured as an input or an output.

A falling or rising edge detection is made on each selected GPI inputs. Every input transition on GPI generates an external positive pulse on GPIINT pin of two SYSCLK width.

## Execution Modes

### Reset Mode

Reset mode is entered when:

- The  $\overline{\text{SYSRES}}$  input is asserted
- Software reset which is caused by the software writing to a Software Reset Register,
- Watchdog reset which is caused by a Watchdog counter time-out
- Error reset which is caused by a hardware parity error

This  $\overline{\text{RESET}}$  output has a minimum of 1024 SYSCLK width to allow the usage of flash memories.

The error and Reset Status Register contain the source of the last processor reset.

## Run Mode

In this mode the IU/FPU is executing, while all peripherals are running (if software enabled).

## System Halt Mode

System Halt mode is entered when the  $\overline{\text{SYSHALT}}$  input is asserted. In this mode, the IU and FPU are frozen, while the timers (including the internal watchdog timer) and UART's are stopped.

## Power Down Mode

This mode is entered by writing to the Power Down Register. In this mode, the IU and FPU are frozen. The TSC695F leaves the power-down mode if an external interrupt is asserted.

## Error Halt Mode

Error Halt mode is entered under the following circumstances:

- A internal hardware parity error.
- The IU enters error mode.

The only way to exit Error Halt Mode is through Cold Reset by asserting  $\overline{\text{SYSRESET}}$ .

## Error Handler

The TSC695F has one error output signal ( $\overline{\text{SYSERR}}$ ) which indicates that an unmasked error has occurred. Any error signalled on the error inputs from the IU and the FPU is latched and reflected in the Error and Reset Status Register. By default, an error leads to a processor halt.

## Parity Checking

The TSC695F includes:

- Parity checking and generation (if required) on the external data bus,
- Parity checking on the external address bus,
- Parity checking on ASI and SIZE,
- Parity checking and generation on all system registers,
- Parity generation and checking on the internal control bus to the IU,

All external parity checking can be disabled using the  $\overline{\text{NOPAR}}$  signal.

## System Clock

The TSC695F uses CLK2 clock input directly and creates a system clock signal by dividing CLK2 by two. It drives SYSCLK pin with a nominal 50% duty cycle for the application. It is highly recommended that only SYSCLK rising edge is used as reference as far as possible.

## System Availability

The SYSAV bit in the Error and Reset Status Register can be used by software to indicate system availability.

## Test Mode

The TSC695F includes a number of software test facilities such as EDAC test, Parity test, Interrupt test, Error test and a simple Test Access Port. These test functions are controlled using the Test Control Register.

## Test and Diagnostic Hardware Functions

A variety of TSC695F test and diagnostic hardware functions, including boundary scan, internal scan, clock control and On-chip Debugger, are controlled through an IEEE 1149.1 (JTAG) standard Test Access Port (TAP).

### Test Access Port

The TAP interfaces to the JTAG bus via 5 dedicated pins on the TSC695F chip. These pins are:

- TCK (input): Test Clock
- TMS (input): Test Mode Select
- TDI (input): Test Data Input
- TDO (output): Test Data Output
- $\overline{\text{TRST}}$  (input): Test Reset

### Instruction Register

Five standard instructions are supported by the TSC695F TAP.

| Binary Value | Name of Instruction | Data Register          | Scan Chain Accessed    |
|--------------|---------------------|------------------------|------------------------|
| 00. 0000     | EXTEST              | Boundary Scan Register | Boundary scan chain    |
| 00. 0001     | SAMPLE/PRELOAD      | Boundary Scan Register | Boundary scan chain    |
| 00. 0011     | INTEST              | Boundary Scan Register | Boundary scan chain    |
| 11. 1111     | BYPASS              | Bypass Register        | Bypass register        |
| 10. 0000     | IDCODE              | Device ID Register     | ID register scan chain |

### Debugging

The design is highly testable with the support of an On-Chip Debugger (OCD), an internal and boundary scan through JTAG interface.

## Electrical Characteristics

### Absolute Maximum Ratings

|                           |                 |
|---------------------------|-----------------|
| Military Range .....      | -55°C to +125°C |
| Storage Temperature ..... | -65°C to +150°C |
| Supply Voltage .....      | -0.5V to +7.0V  |
| Input Voltage .....       | -0.5V to +7.0V  |

Note: Stresses at or above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

### DC Characteristics

**Table 6.** DC Characteristics at VDD +5V ± 10%

| Symbol                  | Parameter                                    | Min | Typ | Max | Unit | Test Conditions                                           |
|-------------------------|----------------------------------------------|-----|-----|-----|------|-----------------------------------------------------------|
| V <sub>IL</sub> trigger | Input Low Voltage for trigger input          | –   | –   | 0.8 | V    | V <sub>CC</sub> = 4.5 to 5.5V                             |
| V <sub>IH</sub> trigger | Input High Voltage for trigger input         | 3.0 | –   | –   | V    | V <sub>CC</sub> = 4.5 to 5.5V                             |
| ΔVT                     | Input Hysteresis for trigger input           | –   | 0.9 | –   | V    | V <sub>CC</sub> = 4.5 to 5.5V                             |
| V <sub>IL</sub> TTL     | Input Low Voltage for TTL input              | –   | –   | 0.8 | V    | V <sub>CC</sub> = 4.5 to 5.5V                             |
| V <sub>IH</sub> TTL     | Input High Voltage for TTL input             | 2.2 | –   | –   | V    | V <sub>CC</sub> = 4.5 to 5.5V                             |
| V <sub>OL</sub> 400 pF  | Output Low Voltage for 400 pF buffer         | –   | 0.3 | 0.4 | V    | V <sub>CC</sub> = 4.5 to 5.5V<br>I <sub>OL</sub> = 12 mA  |
| V <sub>OH</sub> 400 pF  | Output High Voltage for 400 pF buffer        | 2.4 | 0.3 | –   | V    | V <sub>CC</sub> = 4.5 to 5.5V<br>I <sub>OH</sub> = -16 mA |
| V <sub>OL</sub> 150 pF  | Output Low Voltage for 150 pF buffer         | –   | 0.3 | 0.4 | V    | V <sub>CC</sub> = 4.5 to 5.5V<br>I <sub>OL</sub> = 4 mA   |
| V <sub>OH</sub> 150 pF  | Output High Voltage for 150 pF buffer        | 2.4 | 4.3 | –   | V    | V <sub>CC</sub> = 4.5 to 5.5V<br>I <sub>OH</sub> = -6 mA  |
| I <sub>CC</sub> OP      | Operating Supply Current for core processor  | –   | –   | 230 | mA   | V <sub>CC</sub> = 5.5V, f = 25 MHz                        |
|                         |                                              | –   | –   | 210 |      | V <sub>CC</sub> = 5.5V, f = 20 MHz                        |
|                         |                                              | –   | –   | 170 |      | V <sub>CC</sub> = 5.5V, f = 10 MHz                        |
| I <sub>CC</sub> PD      | Power Down Supply Current for core processor | –   | –   | 41  | mA   | V <sub>CC</sub> = 5.5V, f = 25 MHz                        |
|                         |                                              | –   | –   | 38  |      | V <sub>CC</sub> = 5.5V, f = 20 MHz                        |
|                         |                                              | –   | –   | 30  |      | V <sub>CC</sub> = 5.5V, f = 10 MHz                        |

## Capacitance Ratings

| Parameter | Description              | Max  |
|-----------|--------------------------|------|
| $C_{IN}$  | Input Capacitance        | 7 pF |
| $C_{OUT}$ | Output Capacitance       | 8 pF |
| $C_{IO}$  | Input/Output Capacitance | 8 pF |

## AC Characteristics

Table 7. AC Characteristics (SYSCLK Freq. = 25 MHz - 5V  $\pm$  10%)  $C_{load} = 50$  pF,  $V_{ref} = 2.5$ V

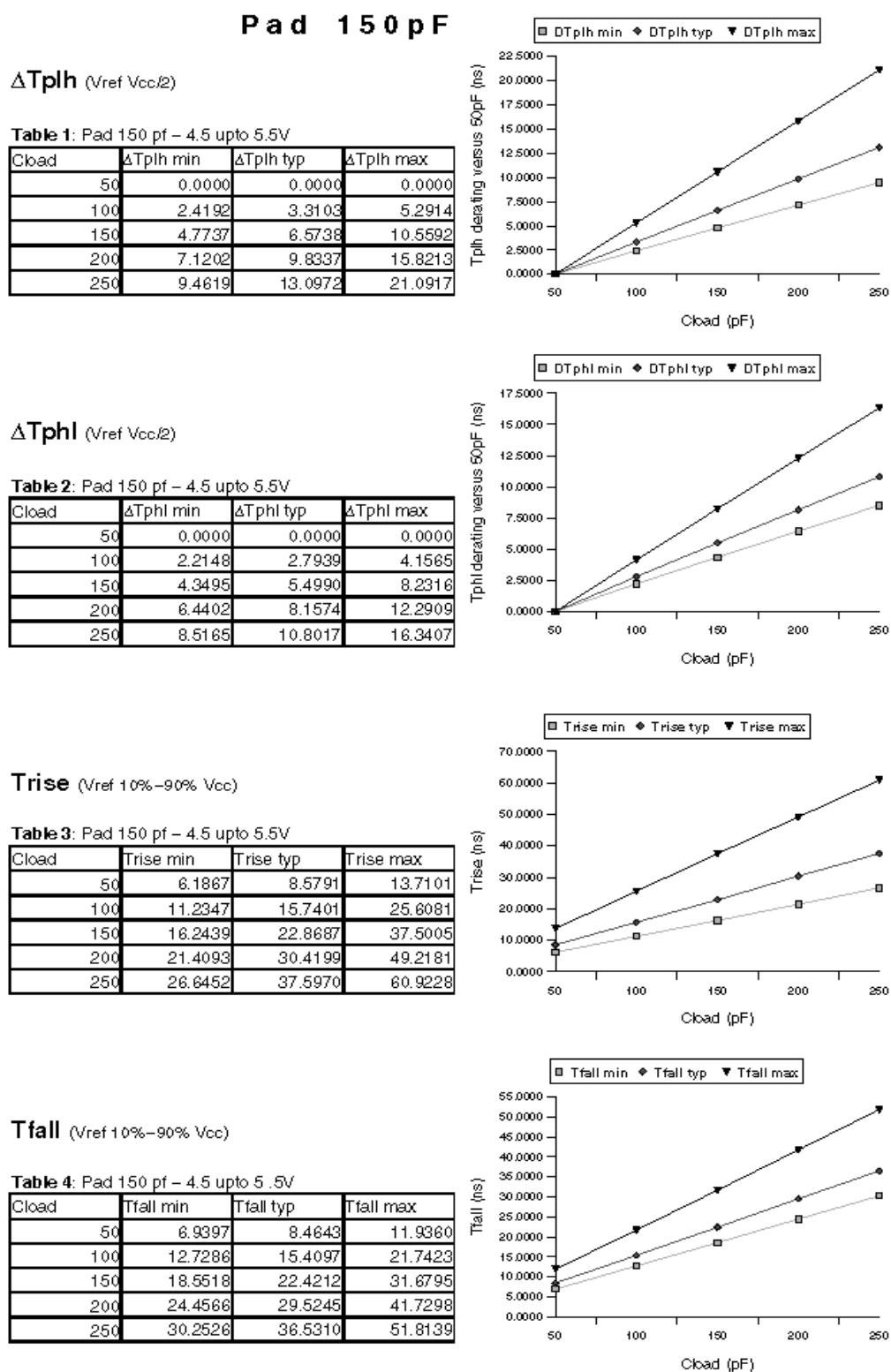
| Parameter | Min (ns) | Max (ns) | Comment                                                                          | Reference Edge     |
|-----------|----------|----------|----------------------------------------------------------------------------------|--------------------|
| t1        | 20       | –        | CLK2 period                                                                      | –                  |
| t2        | 40       | –        | SYSCLK period                                                                    | –                  |
| t3        | 9.75     | –        | CLK2 high and low pulse width                                                    | –                  |
| t4        | –        | 6.5      | RA(31:0) RAPAR RSIZE RLDSTO LOCK output delay                                    | SYSCLK+            |
| t5        | –        | 12.5     | MEMCS*(9:0) ROMCS* EXMCS* output delay                                           | SYSCLK+            |
| t6        | –        | 15       | DDIR DDIR* output delay                                                          | SYSCLK+            |
| t7        | –        | 23.5     | MEMWR* IOWR* output delay<br><u>formula:</u> $13.5 \text{ ns} + \frac{1}{4} t_2$ | SYSCLK- or SYSCLK+ |
| t8        | –        | 20.5     | OE* HL output delay<br><u>formula:</u> $10.5 \text{ ns} + \frac{1}{4} t_2$       | SYSCLK+            |
| t9        | 11.5     | –        | Data setup time during load                                                      | SYSCLK+            |
| t10       | 5        | –        | Data hold time during load                                                       | SYSCLK+            |
| t11       | –        | 28       | Data output delay                                                                | SYSCLK-            |
| t12       | 8        | –        | Data output valid to HZ – guaranteed by design                                   | SYSCLK+            |
| t13       | –        | 19       | CB output delay                                                                  | SYSCLK+            |
| t14       | –        | 13       | ALE* output delay                                                                | SYSCLK-            |
| t15       | –        | 21       | BUFFEN* HL output delay<br><u>formula:</u> $11 \text{ ns} + \frac{1}{4} t_2$     | SYSCLK+            |
| t16       | –        | 15       | MHOLD* output delay – guaranteed by design                                       | SYSCLK+            |
| t17       | –        | 15       | MDS* DRDY* output delay                                                          | SYSCLK+            |
| t20       | –        | 15       | MEXC* output delay                                                               | SYSCLK-            |
| t21       | 10       | –        | RASI(3:0) RSIZE(1:0) RASPAR setup time                                           | SYSCLK+            |
| t22       | 3        | –        | RASI(3:0) RSIZE(1:0) RASPAR hold time                                            | SYSCLK+            |
| t23       | –        | 13       | BOOT PROM address output delay                                                   | SYSCLK+            |
| t24       | 12       | –        | BUSRDY* setup time                                                               | SYSCLK+            |
| t25       | 0        | –        | BUSRDY* hold time                                                                | SYSCLK+            |

**Table 7. AC Characteristics (SYSCLK Freq. = 25 MHz - 5V  $\pm$  10%) C<sub>load</sub> = 50 pF, V<sub>ref</sub> = 2.5V (Continued)**

| Parameter | Min (ns) | Max (ns) | Comment                                                                                       | Reference Edge           |
|-----------|----------|----------|-----------------------------------------------------------------------------------------------|--------------------------|
| t27       | –        | 15       | IOSEL output delay                                                                            | SYSCLK+ HL<br>SYSCLK- LH |
| t28       | 12       | 20       | DMAAS setup time<br><u>formula of max:</u> $\frac{1}{2}t_2$                                   | SYSCLK+                  |
| t29       | 0        | 20       | DMAAS hold time<br><u>formula of max:</u> $\frac{1}{2}t_2$                                    | SYSCLK-                  |
| t30       | 12       | –        | DMAREQ* setup time                                                                            | SYSCLK+                  |
| t31       | –        | 15       | DMAGNT* output delay                                                                          | SYSCLK+                  |
| t32       | 10       | –        | RA(31:0) RAPAR CPAR setup time                                                                | SYSCLK+                  |
| t33       | 3        | –        | RA(31:0) RAPAR CPAR hold time                                                                 | SYSCLK+                  |
| t36       | 100      | –        | TCK period                                                                                    | -                        |
| t37       | 10       | –        | TMS setup time                                                                                | TCK+                     |
| t38       | 4        | –        | TMS hold time                                                                                 | TCK+                     |
| t39       | 10       | –        | TDI setup time                                                                                | TCK+                     |
| t40       | 10       | –        | TDI hold time                                                                                 | TCK+                     |
| t41       | –        | 20       | TDO output delay                                                                              | TCK-                     |
| t46       | –        | 22       | INULL output delay                                                                            | SYSCLK+                  |
| t48       | –        | 22       | RESET* CPUHALT* output delay                                                                  | SYSCLK+                  |
| t49       | –        | 20       | SYSERR* SYSAV output delay                                                                    | SYSCLK+                  |
| t50       | –        | 20       | IUERR* output delay                                                                           | SYSCLK+                  |
| t52       | 12       | –        | EXTINT(4:0) setup time                                                                        | SYSCLK-                  |
| t53       | 0        | –        | EXTINT(4:0) hold time                                                                         | SYSCLK+                  |
| t54       | –        | 15       | EXTINTACK output delay                                                                        | SYSCLK+                  |
| t56       | –        | 8.5      | OE* LH output delay (no DMA mode)                                                             | SYSCLK+                  |
| t57       | –        | 9        | BUFFEN* LH output delay                                                                       | SYSCLK+                  |
| t60       | –        | 22       | INST output delay                                                                             | SYSCLK+                  |
| t61       | 20       | –        | Data output delay to low-Z – guaranteed by design<br><u>formula:</u> 10 ns + $\frac{1}{4}t_2$ | SYSCLK+                  |



Figure 3. 150 pF Buffer Response (Data from simulation)



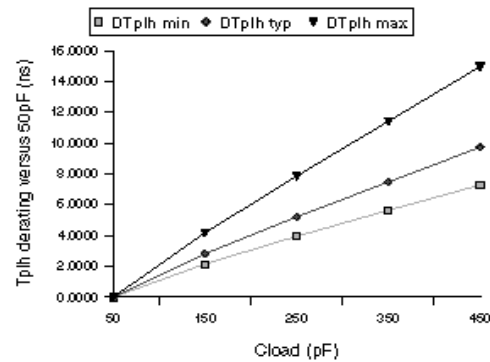
**Figure 4. 400 pF Buffer Response (Data from simulation)**

### Pad 400pF

$\Delta T_{plh}$  ( $V_{ref} V_{cc}/2$ )

**Table 5:** Pad 400 pf – 4.5 upto 5.5V

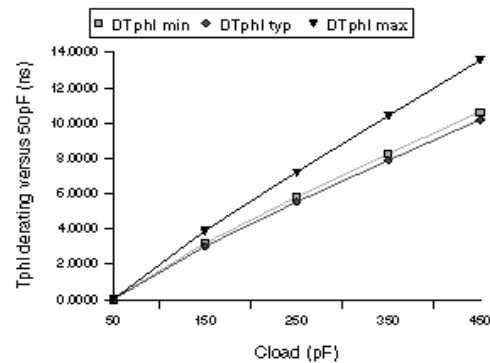
| Clod | $\Delta T_{plh}$ min | $\Delta T_{plh}$ typ | $\Delta T_{plh}$ max |
|------|----------------------|----------------------|----------------------|
| 50   | 0.0000               | 0.0000               | 0.0000               |
| 150  | 2.1601               | 2.8177               | 4.1663               |
| 250  | 3.9576               | 5.2119               | 7.8496               |
| 350  | 5.6386               | 7.4818               | 11.4194              |
| 450  | 7.2733               | 9.7184               | 14.9618              |



$\Delta T_{phi}$  ( $V_{ref} V_{cc}/2$ )

**Table 6:** Pad 400 pf – 4.5 upto 5.5V

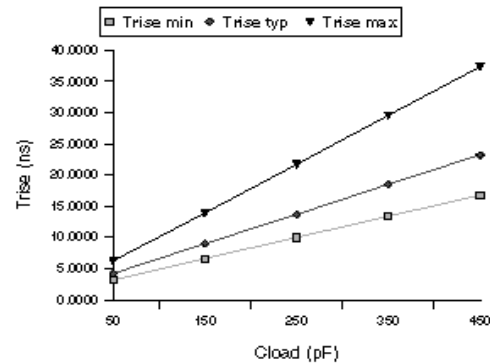
| Clod | $\Delta T_{phi}$ min | $\Delta T_{phi}$ typ | $\Delta T_{phi}$ max |
|------|----------------------|----------------------|----------------------|
| 50   | 0.0000               | 0.0000               | 0.0000               |
| 150  | 3.1851               | 3.0049               | 3.8823               |
| 250  | 5.8077               | 5.5149               | 7.2185               |
| 350  | 8.2550               | 7.8853               | 10.4133              |
| 450  | 10.6267              | 10.1911              | 13.5505              |



$T_{rise}$  ( $V_{ref} 10\% - 90\% V_{cc}$ )

**Table 7:** Pad 400 pf – 4.5 upto 5.5V

| Clod | $T_{rise}$ min | $T_{rise}$ typ | $T_{rise}$ max |
|------|----------------|----------------|----------------|
| 50   | 3.1666         | 4.2291         | 6.2607         |
| 150  | 6.6263         | 9.0002         | 13.8948        |
| 250  | 10.0104        | 13.6901        | 21.7273        |
| 350  | 13.4251        | 18.5600        | 29.5949        |
| 450  | 16.7768        | 23.2394        | 37.3774        |



$T_{fall}$  ( $V_{ref} 10\% - 90\% V_{cc}$ )

**Table 8:** Pad 400 pf – 4.5 upto 5.5V

| Clod | $T_{fall}$ min | $T_{fall}$ typ | $T_{fall}$ max |
|------|----------------|----------------|----------------|
| 50   | 4.3868         | 4.4176         | 5.7936         |
| 150  | 9.1148         | 9.5715         | 12.7515        |
| 250  | 13.6747        | 14.6117        | 19.6288        |
| 350  | 18.2245        | 19.6467        | 26.6077        |
| 450  | 22.8149        | 24.6813        | 33.5087        |

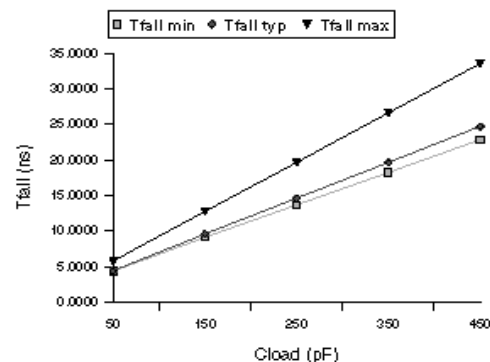
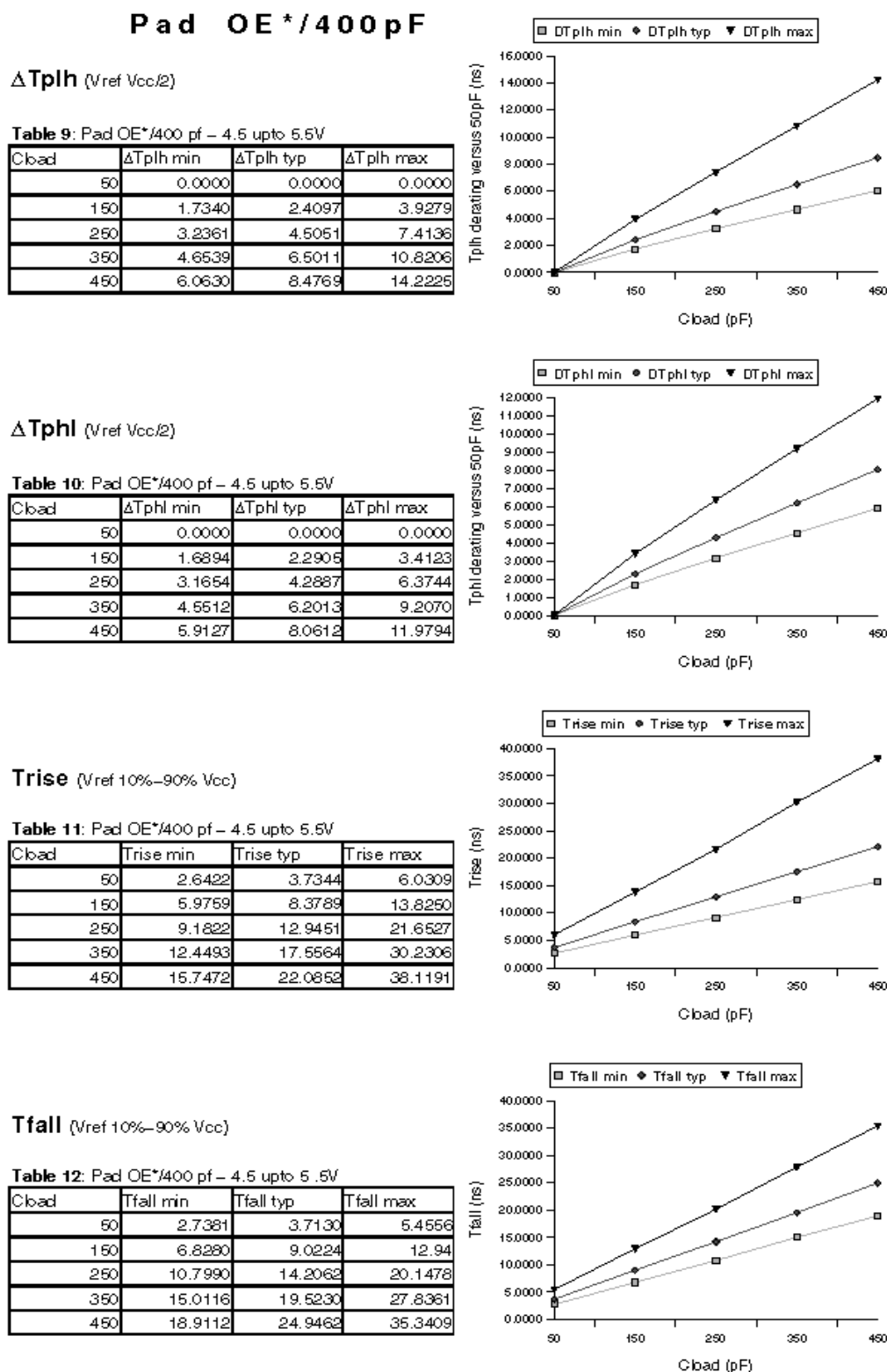


Figure 5. OE\*/400 pF Buffer Response (Data from simulation)



## Timing Diagrams

**Figure 6.** RAM Fetch, RAM Load and RAM Store Sequence - n Waitstates for Read, m Waitstates for Write

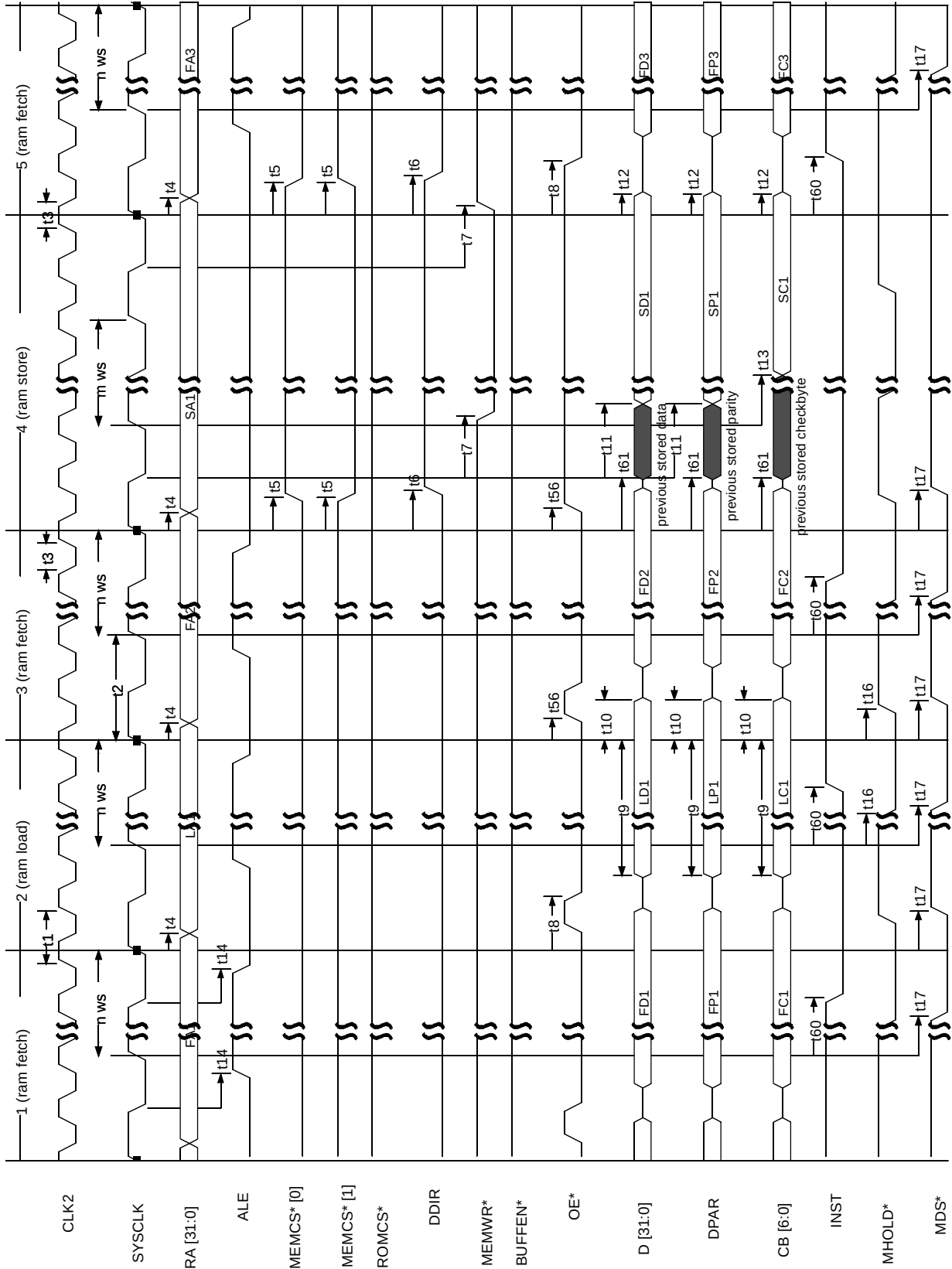
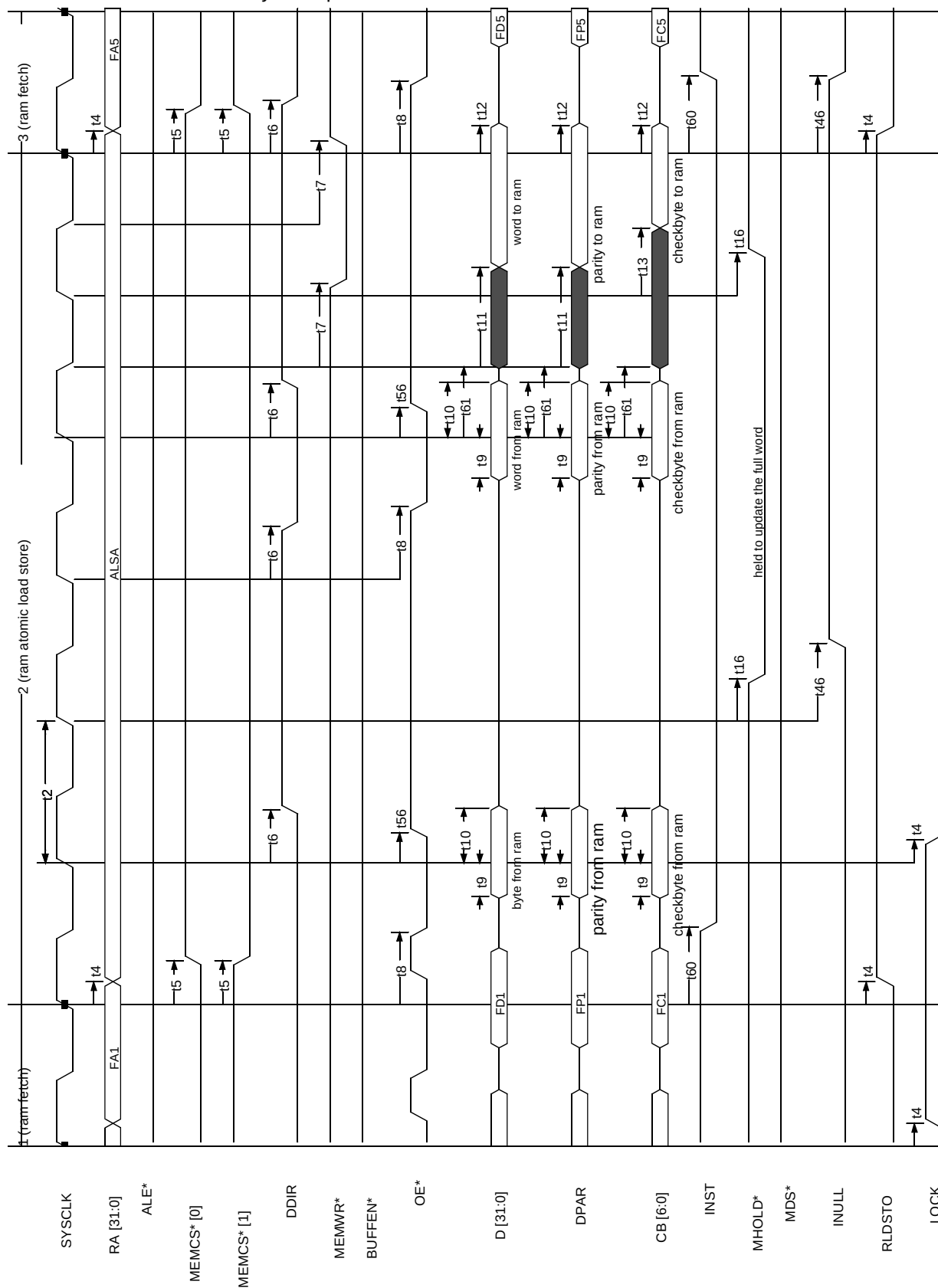


Figure 7. RAM Atomic-load-store byte Sequence - 0 Waitstate



**Figure 8. RAM Load-double and RAM Store-double Sequence - 0 Waitstate**

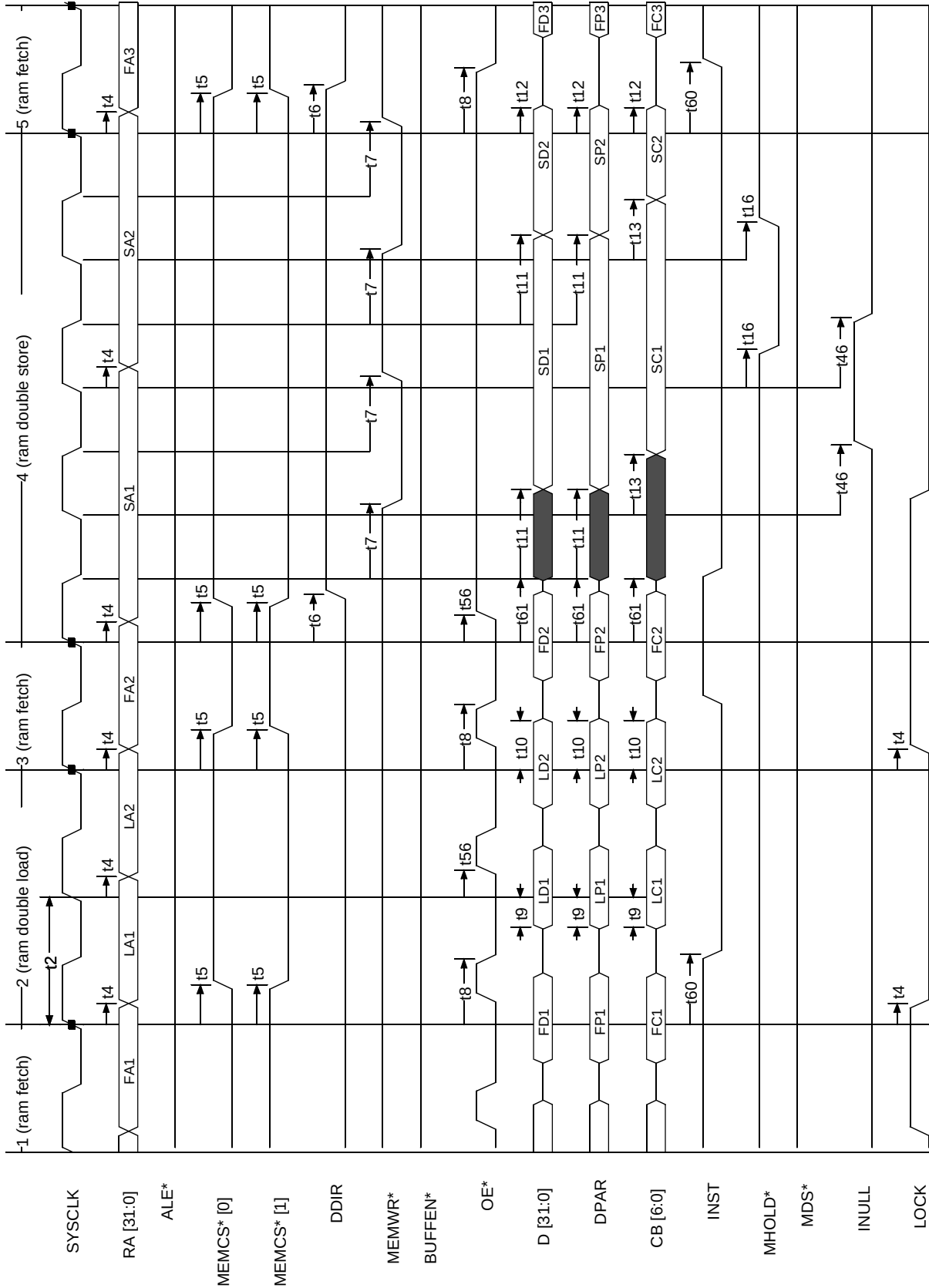
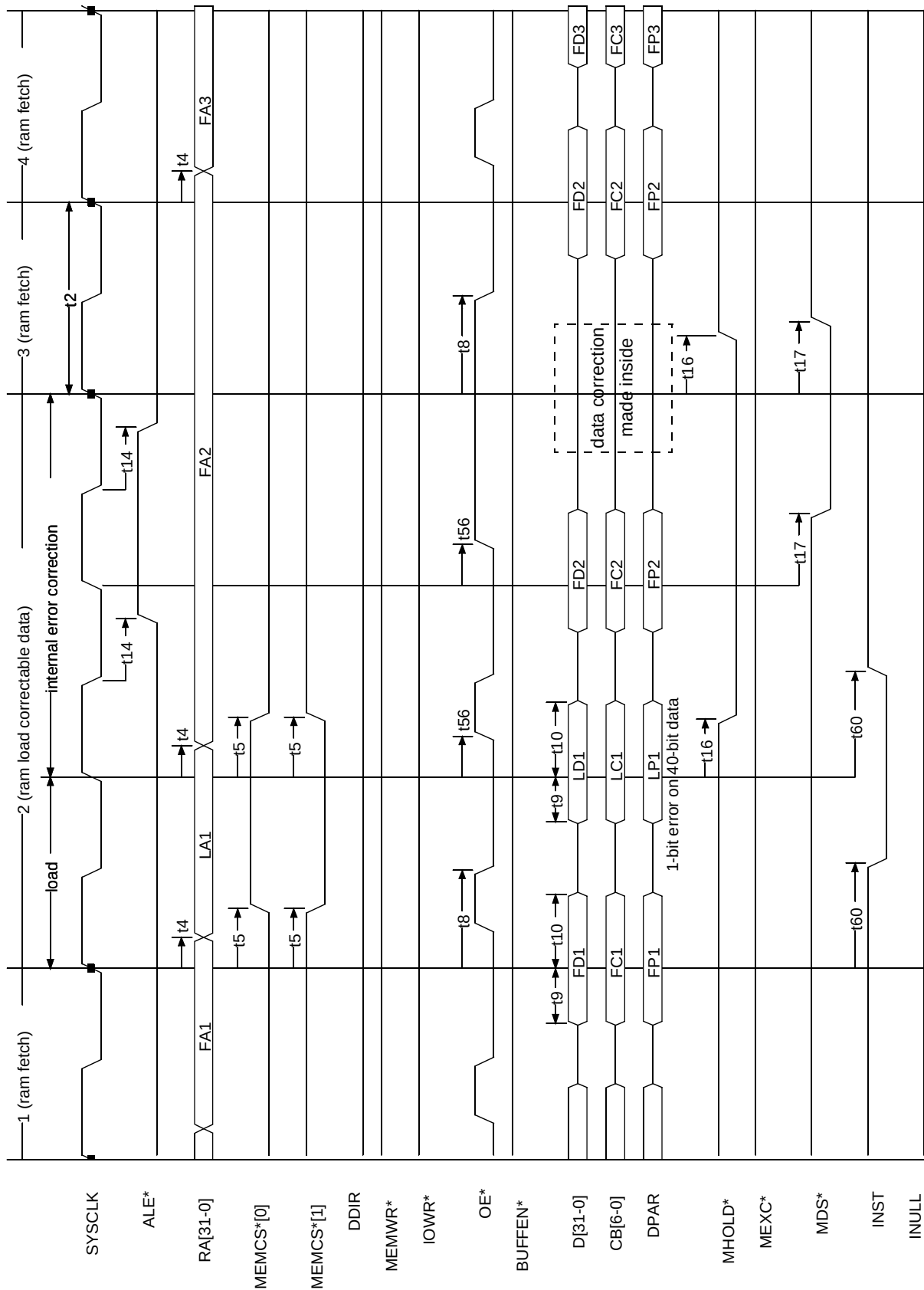


Figure 9. RAM Load with Correctable Error - 0 Waitstate



**Figure 10. RAM Load with Uncorrectable Error - 0 Waitstate**

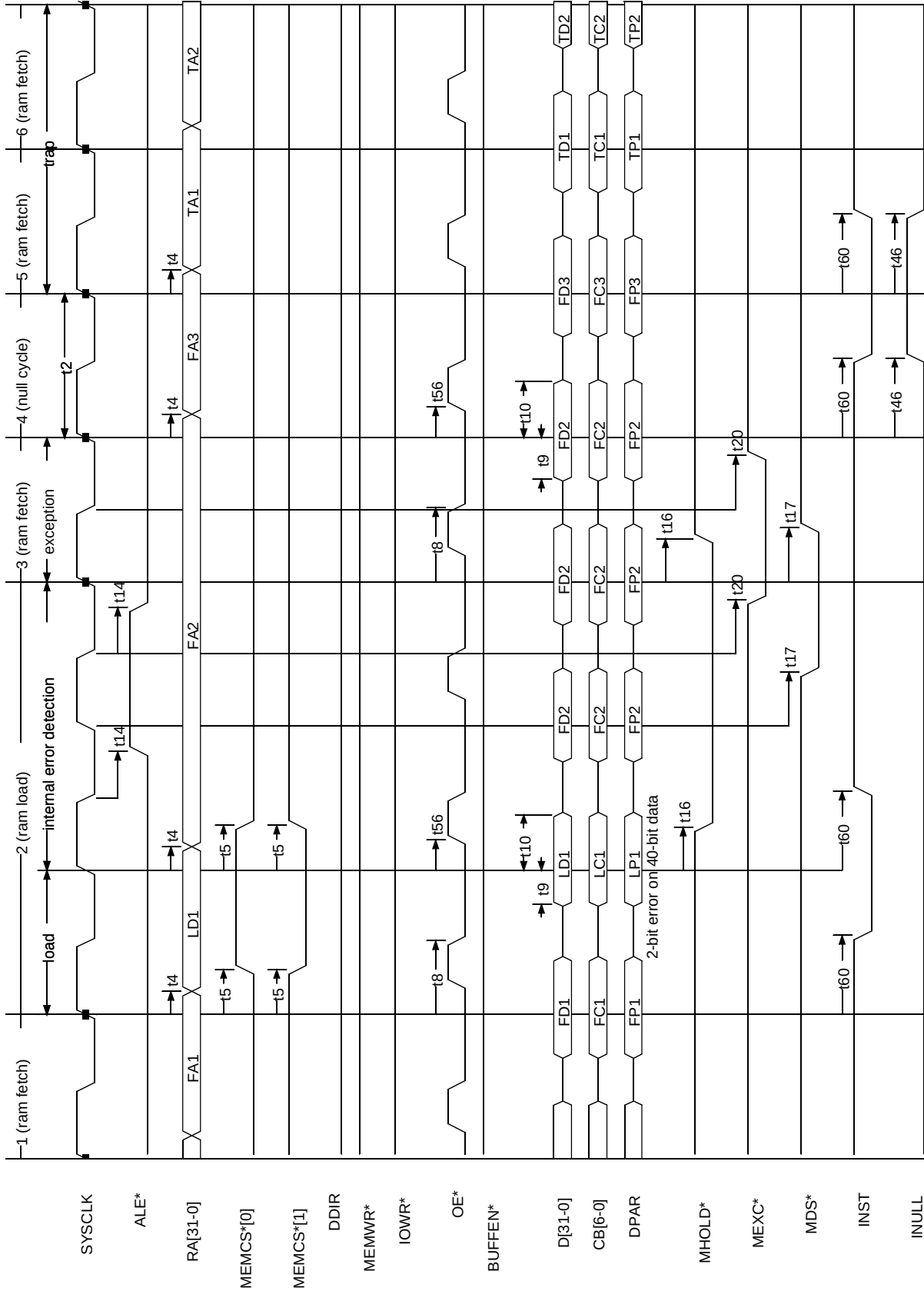
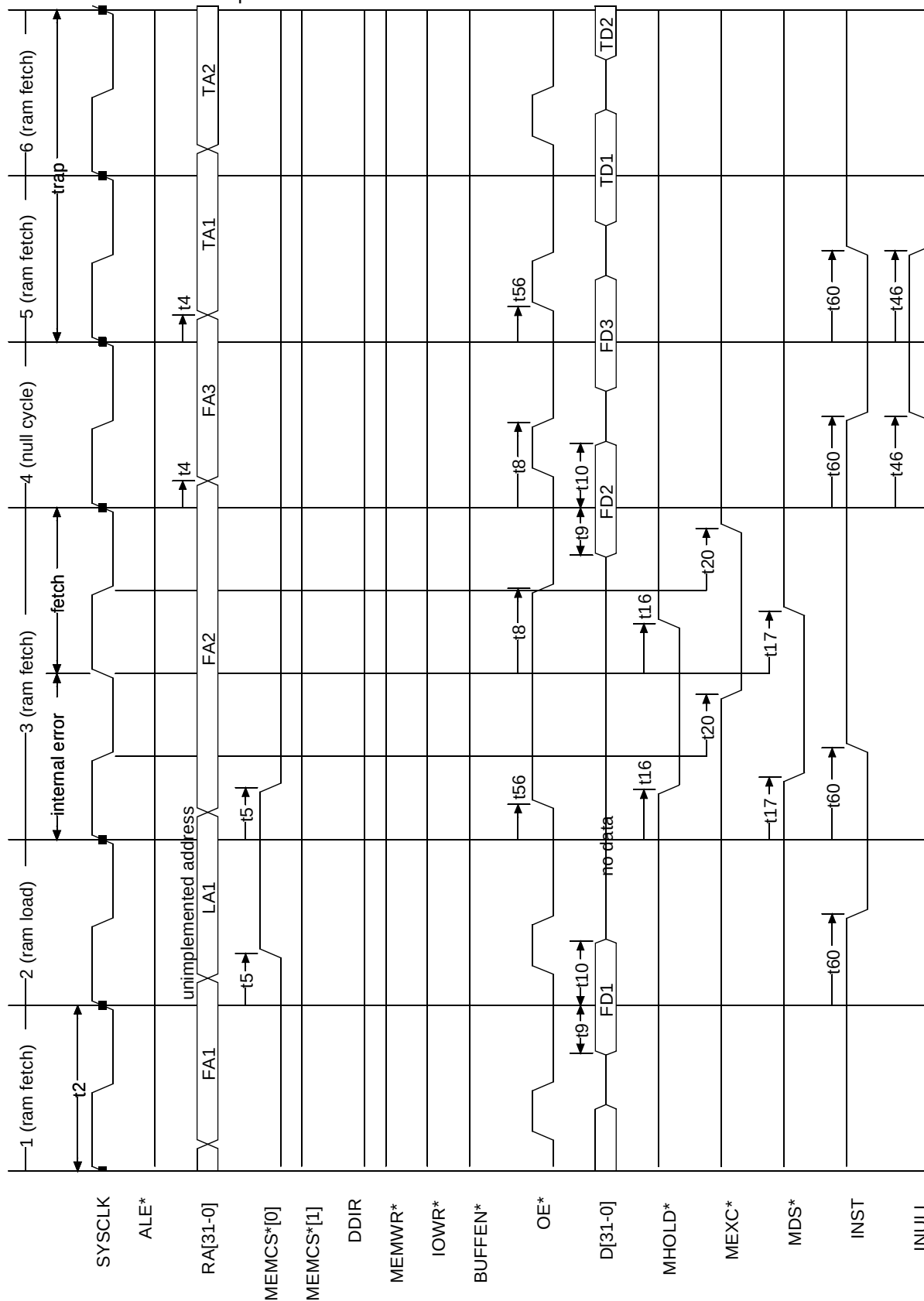
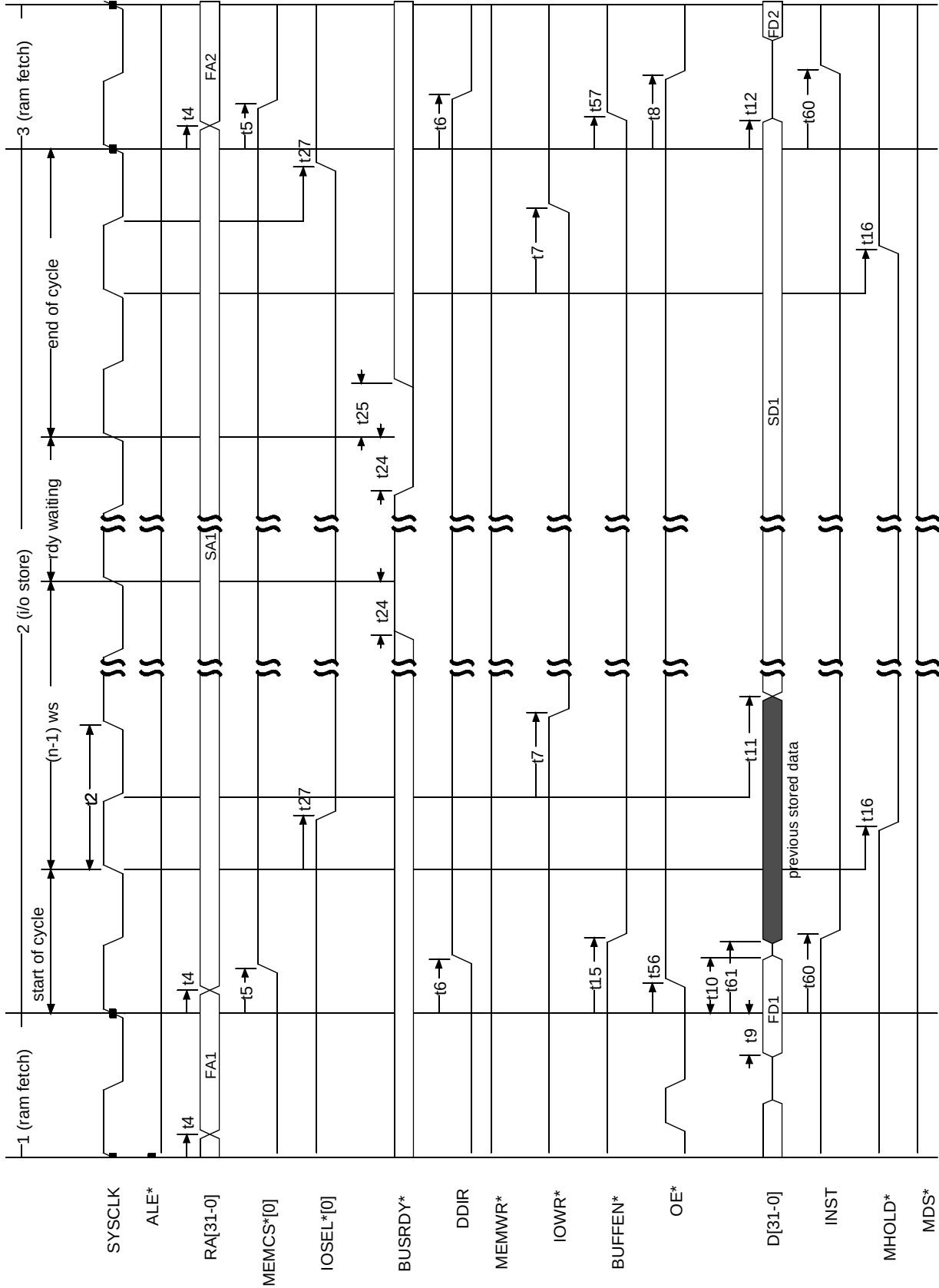




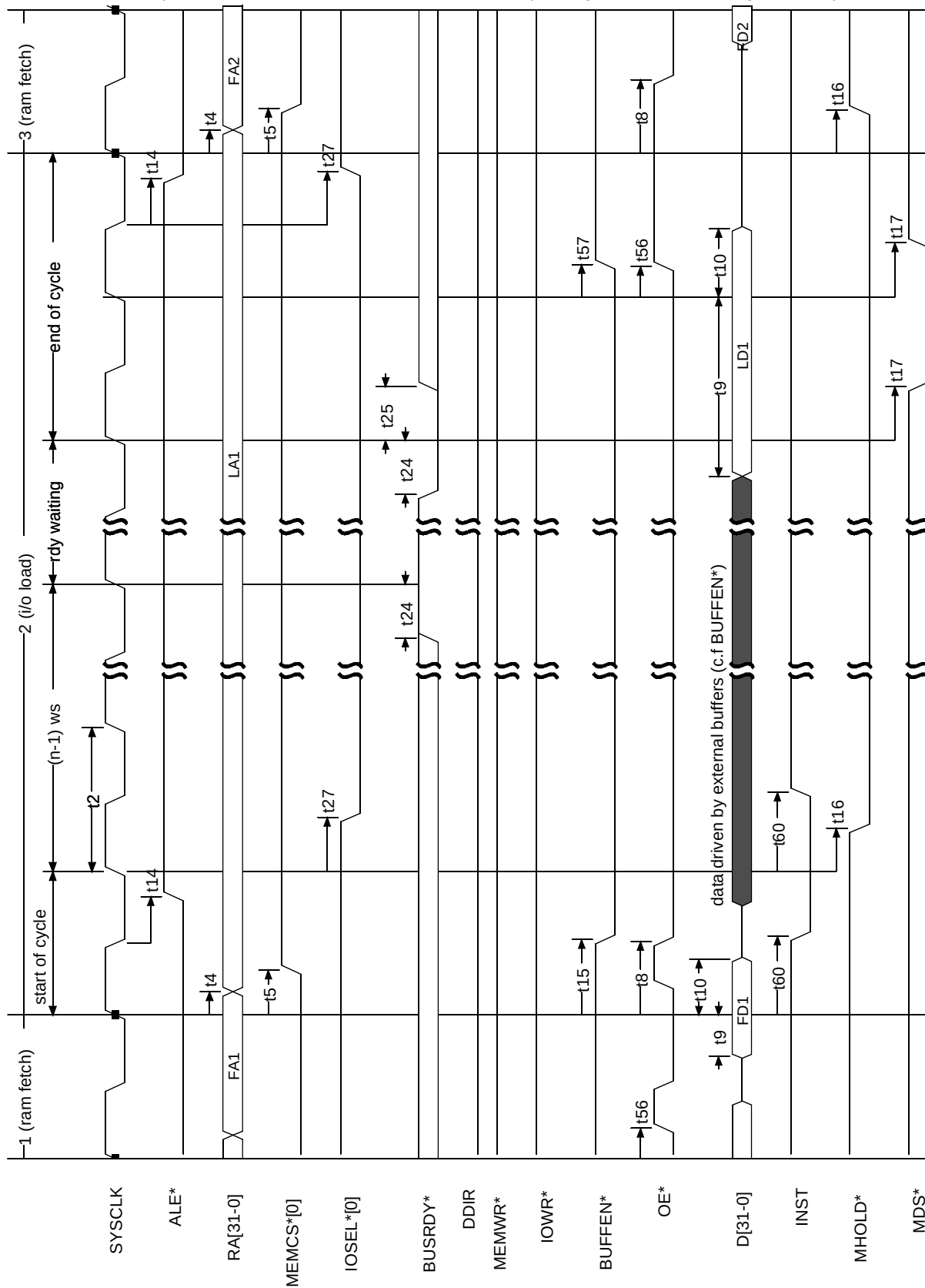
Figure 11. RAM Load with Unimplemented Area Access - 0 Waitstate



**Figure 12.** I/O Store Sequence with BUSRDY\* and n Waitstates (Timing for 0 Waitstate = Timing for 1 Waitstates)



**Figure 13.** I/O Load Sequence with BUSRDY\* and n Waitstates (Timing for 0 ws = Timing for 1 ws)



**Figure 14.** EXCHANGE RAM Store with BUSDRY\* and n Waitstates

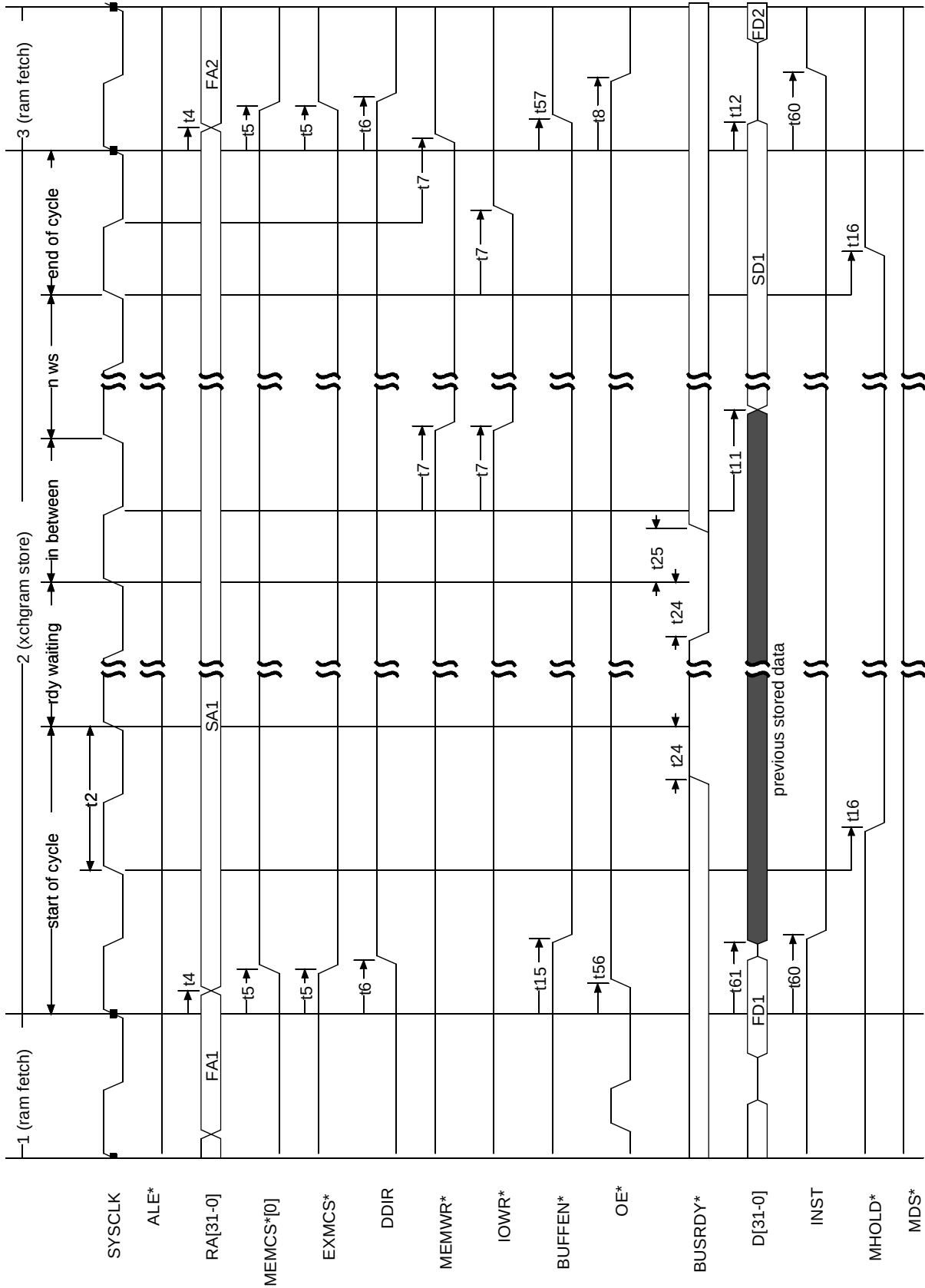
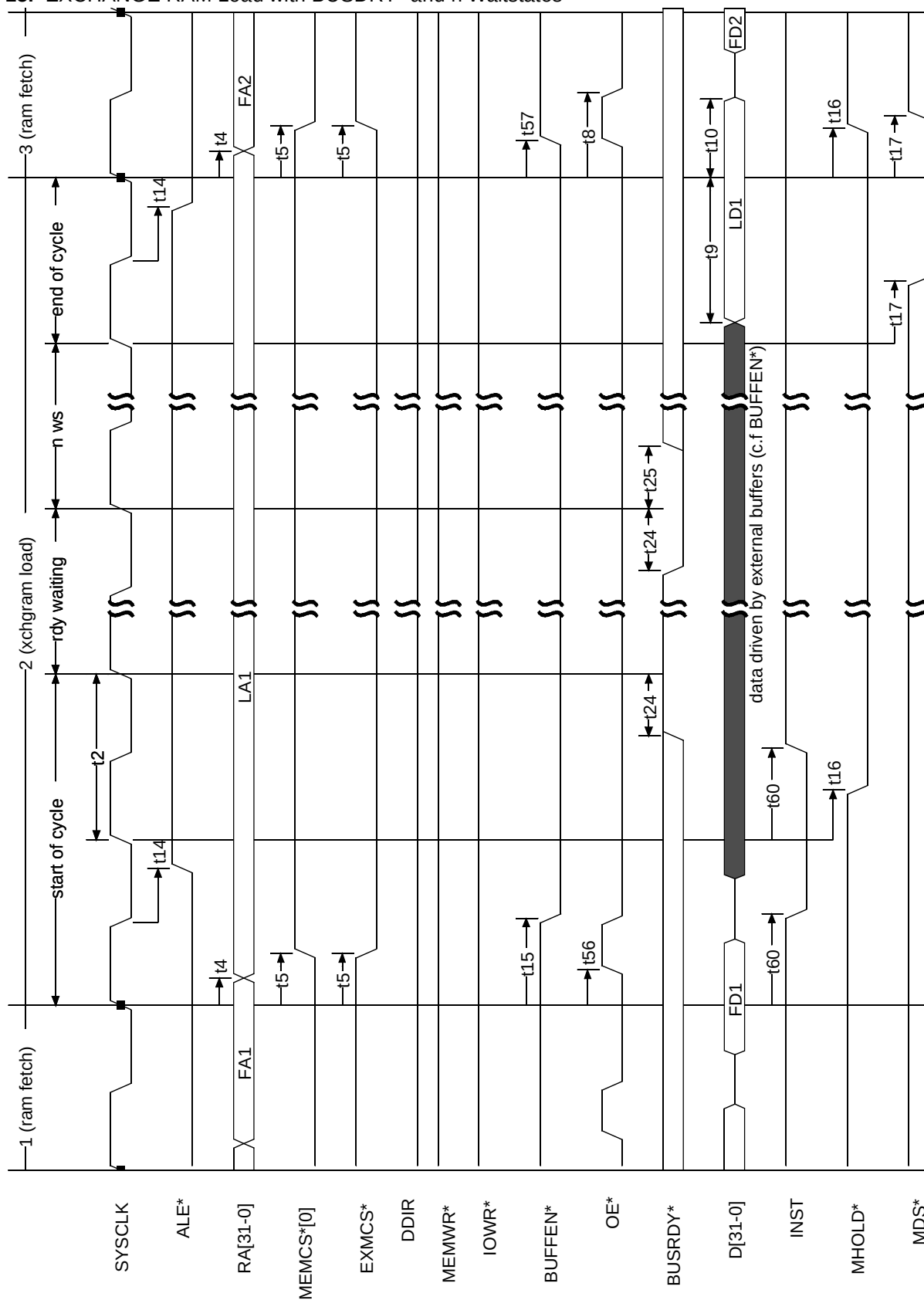


Figure 15. EXCHANGE RAM Load with BUSDRY\* and n Waitstates



**Figure 16. 8-bit BOOT PROM Fetch (or Load Word) - n Waitstates**

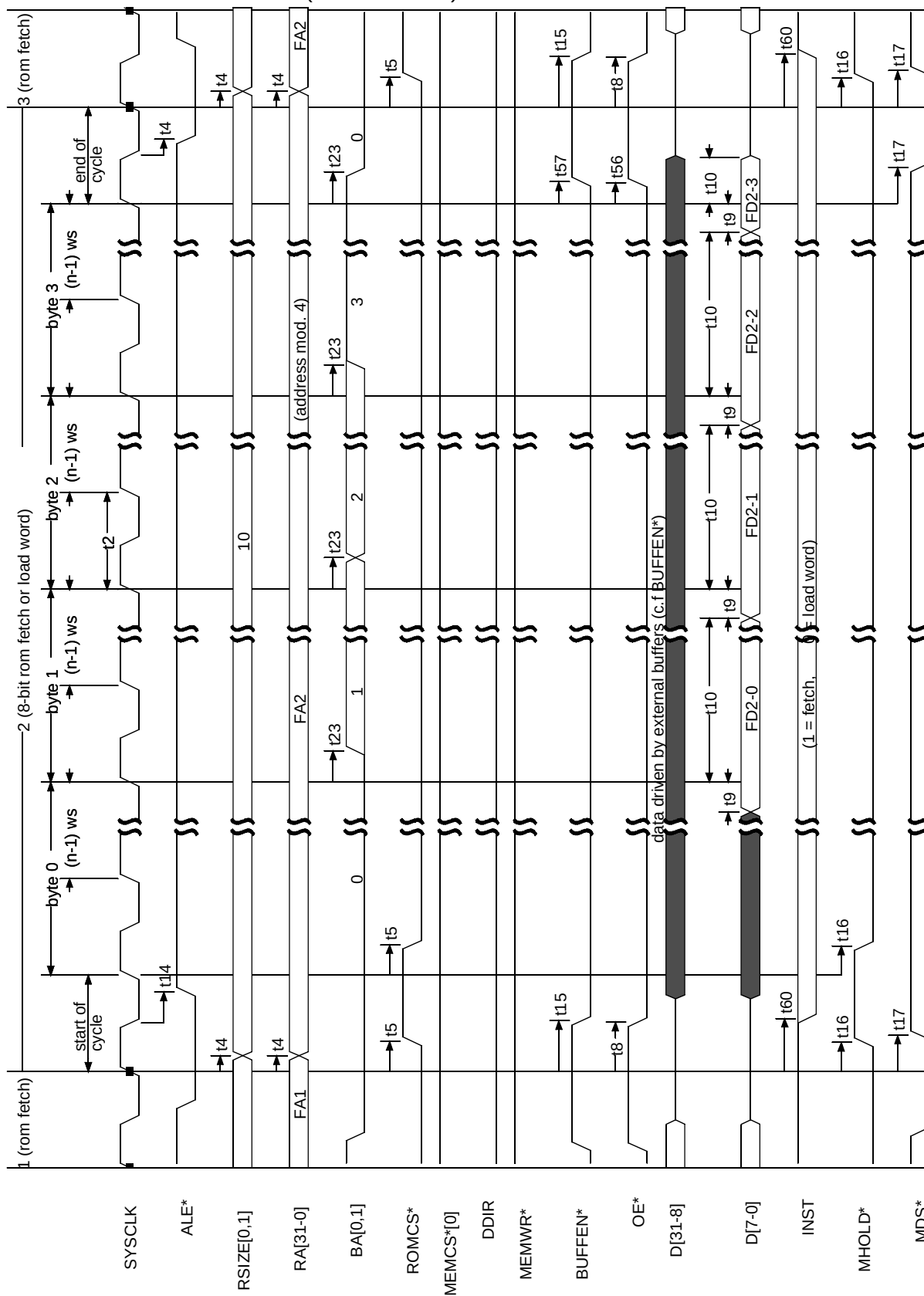
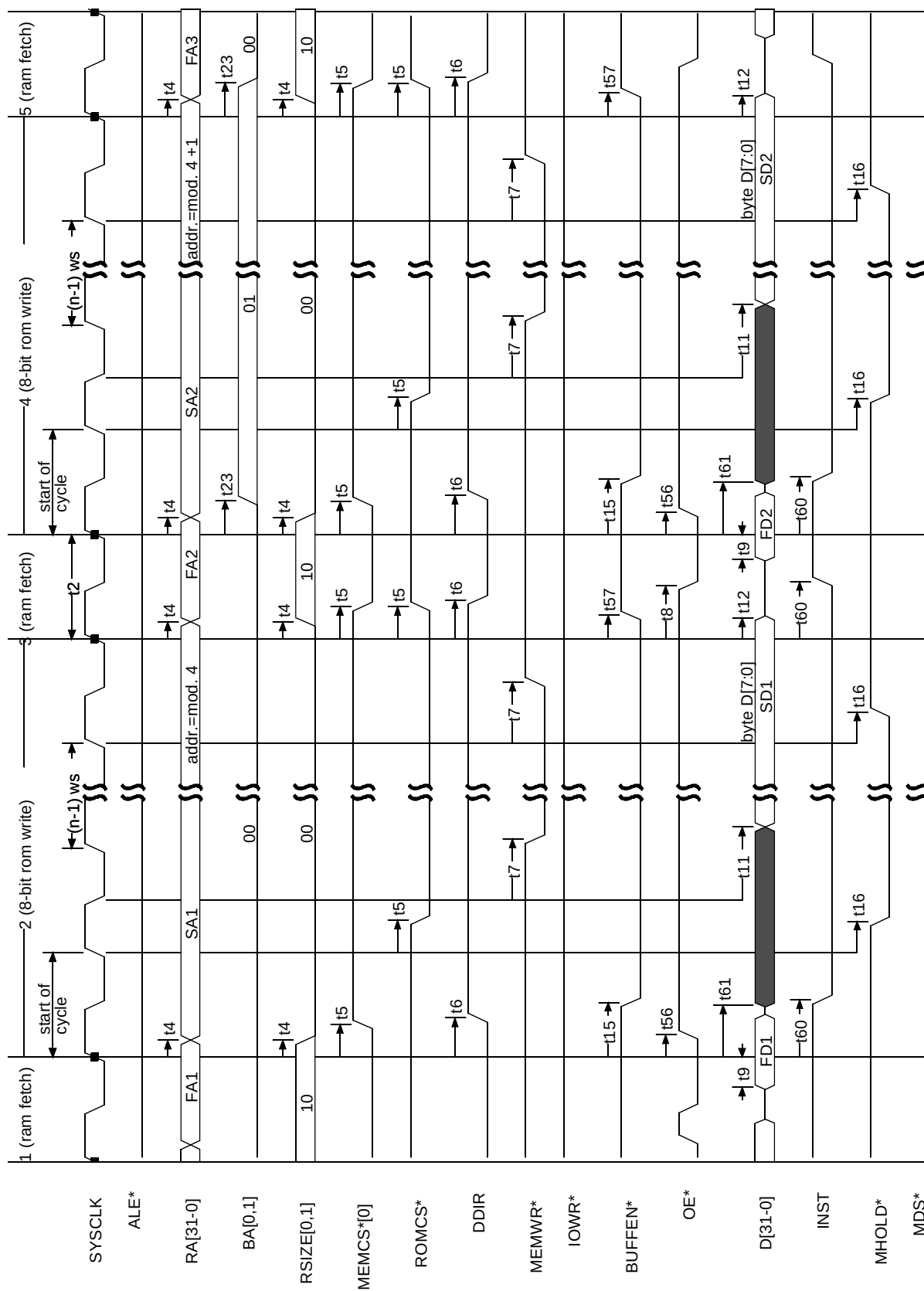


Figure 17. 8-bit BOOT PROM 2x Store byte - n Waitstate



**Figure 18.** DMA RAM load with or without Correctable Error and DMA RAM Store - 0 Waitstates

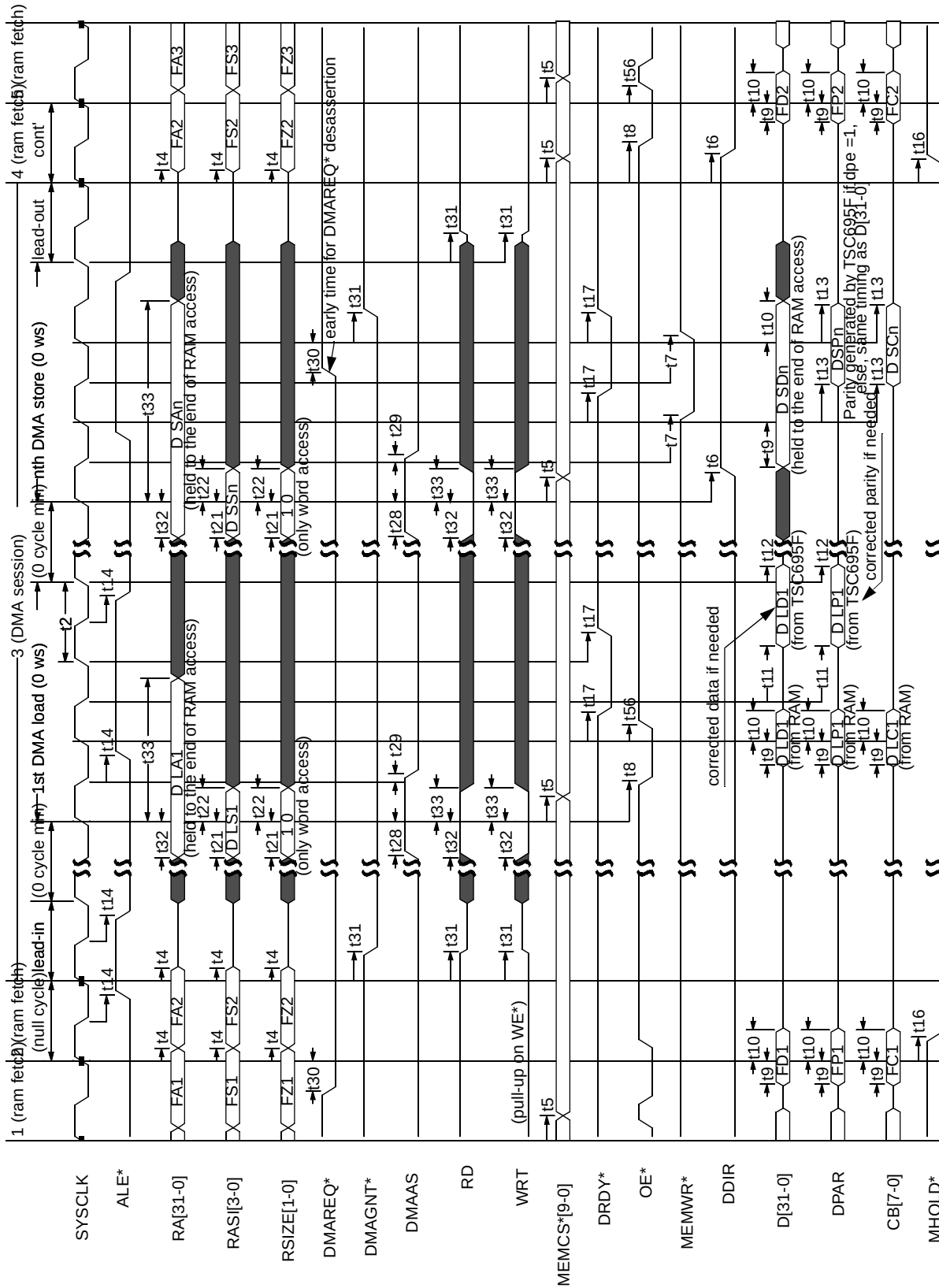
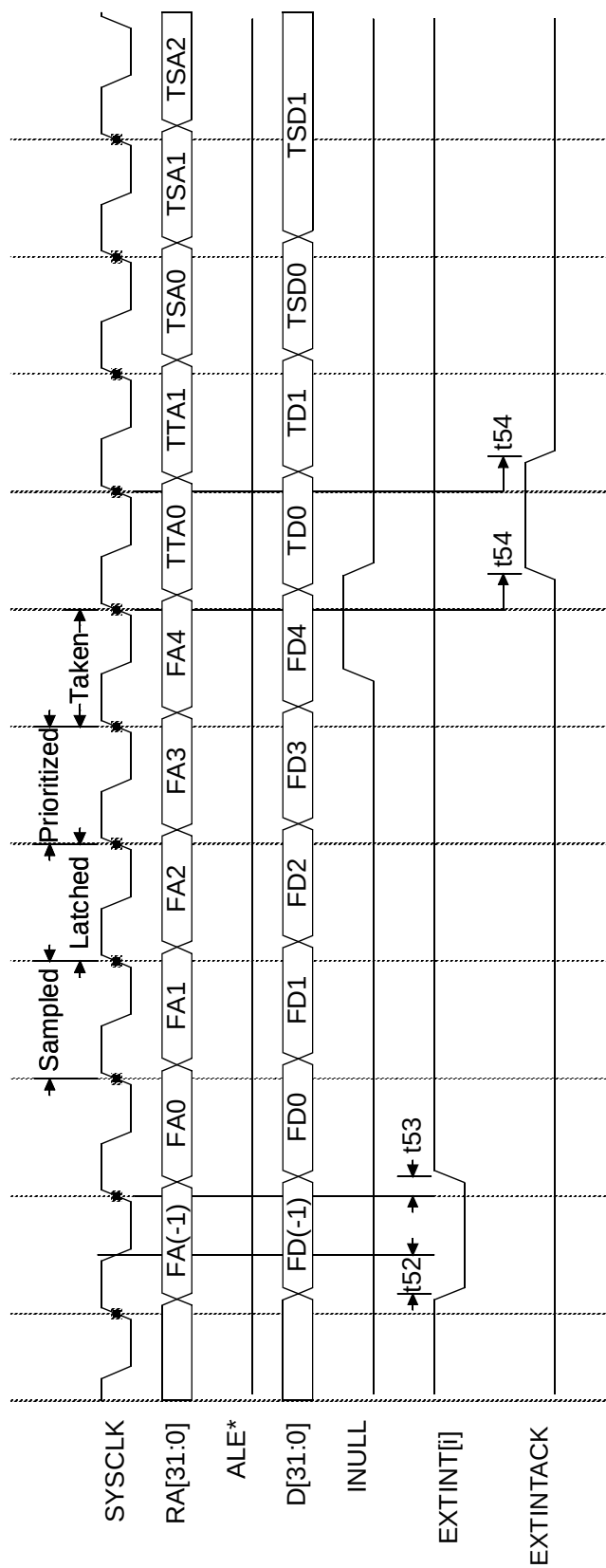




Figure 19. Edge Triggered Interrupt Timing



**Figure 20. Halt Timing**

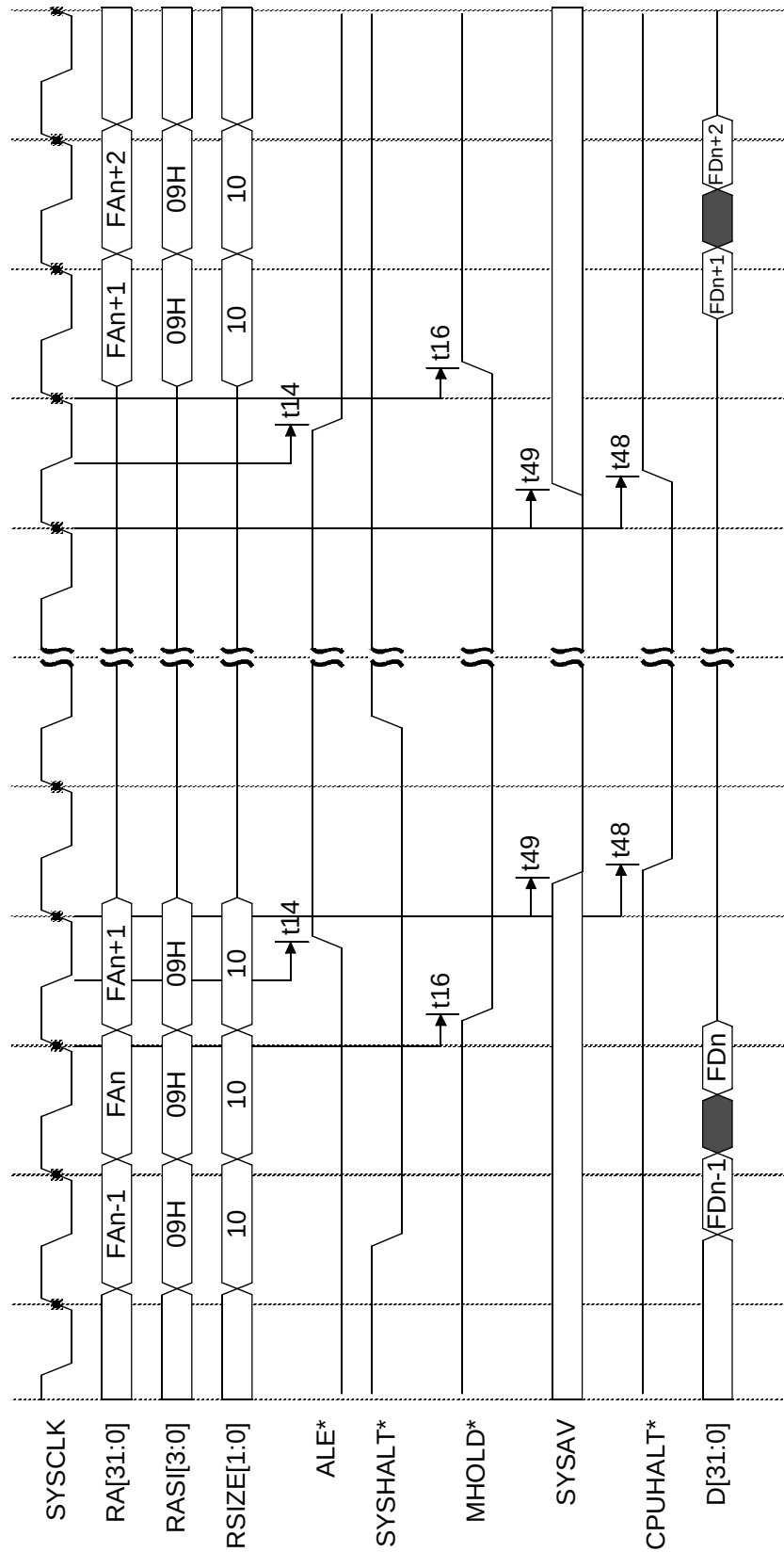
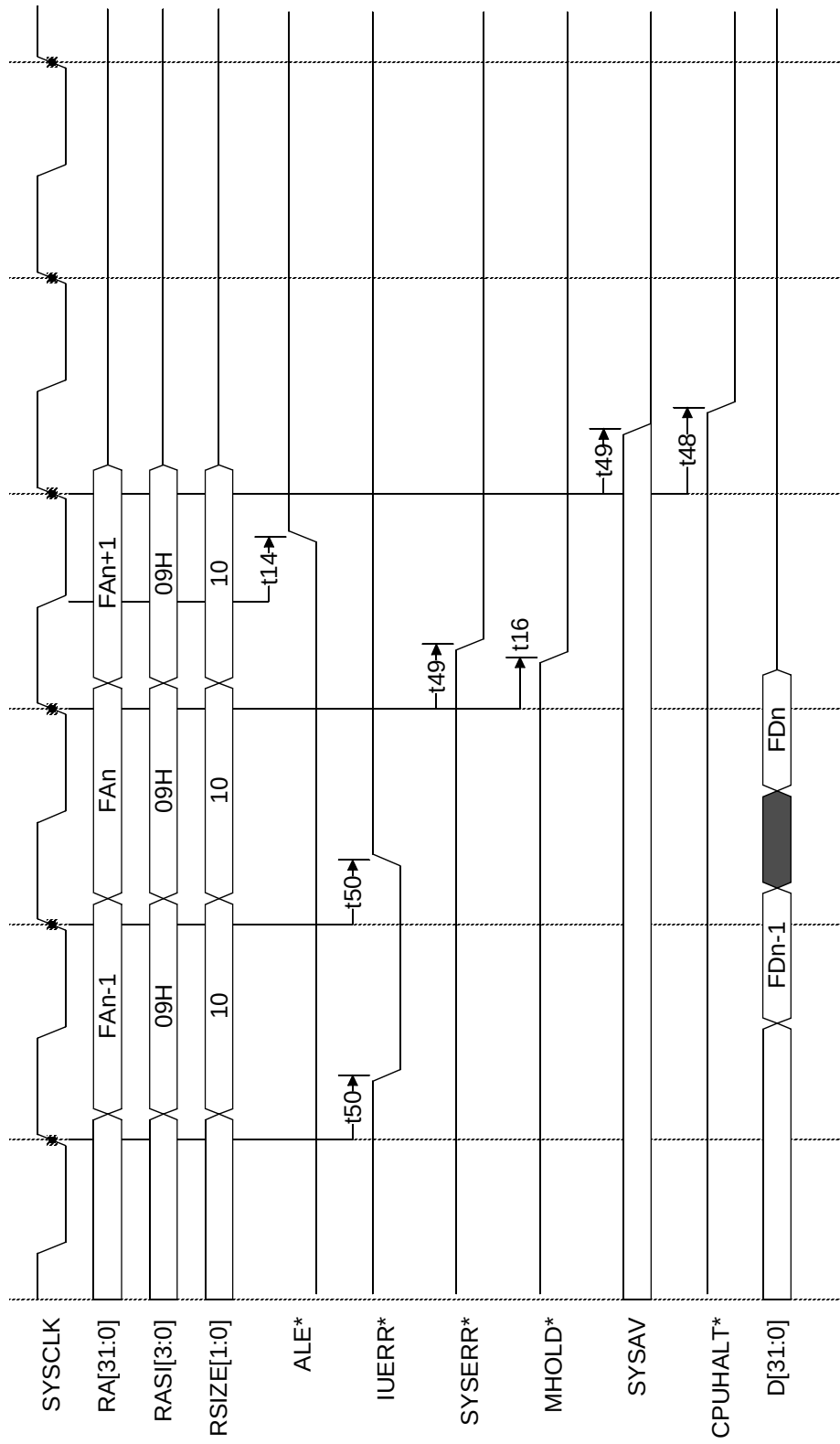
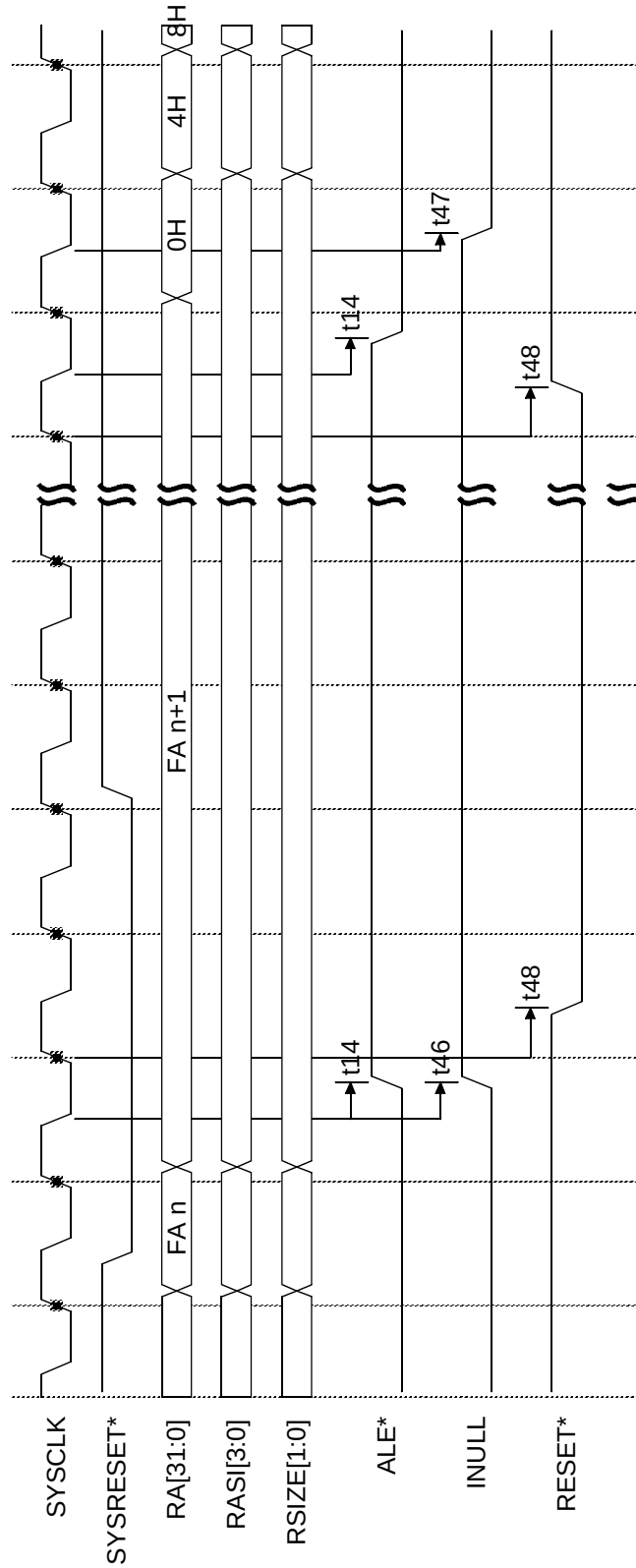


Figure 21. External Error with Halt Timing



**Figure 22. Reset Timing**



## Package Description

### Thermal Characteristics

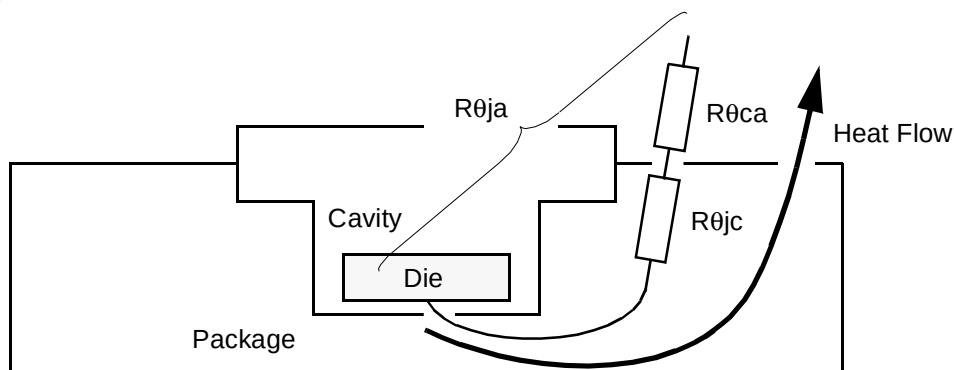
The thermal performance of a package is measured by its ability to dissipate the power required by the device into its surroundings. The electrical power drawn by the device generates heat on the top surface of the die. This heat is conducted through the package to the surface and then transferred to the surrounding air by convection. Each heat transfer step has corresponding resistance to the heat flow, which is given the value  $R\theta$ , the thermal resistance coefficient. Subscripts are added to the coefficient to specify the two points that the heat is transferred between. Commonly used coefficients are  $R\theta_{ja}$  (junction to ambient air),  $R\theta_{jc}$  (junction to case) and  $R\theta_{ca}$  (case to ambient).

An electrical analogy can be made, as shown in the figure below, to illustrate the heat flow of a package. The heat transfer can be characterized mathematically by the following equation:

$$T_j - T_a = P \times R\theta_{ja}$$

- Where:
- $P$  = Device operating power (Watts)
- $T_j$  = Temperature of a junction on the device ( $^{\circ}\text{C}$ )
- $T_a$  = Temperature of the surrounding ambient air ( $^{\circ}\text{C}$ )
- $R\theta_{ja} = R\theta_{jc} + R\theta_{ca}$  in  $^{\circ}\text{C/W}$

**Figure 23.** Thermal Model

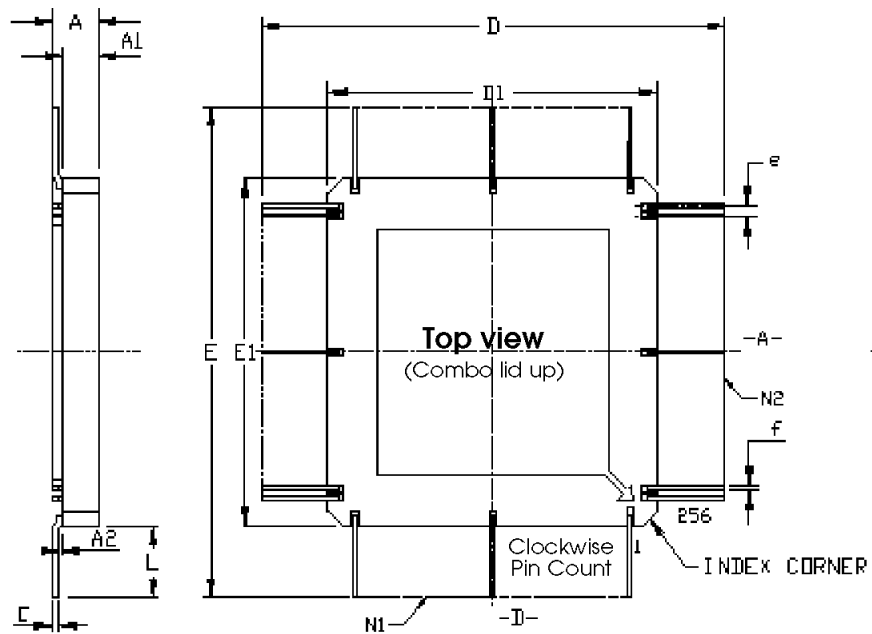


**Table 8.** Thermal Characteristics

**Table 9.**

| Rθ - | Value       | Unit                 | Conditions               |                |                  |
|------|-------------|----------------------|--------------------------|----------------|------------------|
|      |             |                      | Temperature              | Air            | Dissipated Power |
| ja   | 19.8 ~ 23.1 | $^{\circ}\text{C/W}$ | 25/90 $^{\circ}\text{C}$ | Blown air      | 1-2 W            |
| jc   | 0.4         |                      |                          |                |                  |
| ja   | 31.6 ~ 36.9 |                      |                          | Stationary air | 2 W              |
| jc   | 0.4         |                      |                          |                |                  |
| ja   | 35.1 ~ 41   |                      |                          |                | 1 W              |
| jc   | 0.4         |                      |                          |                |                  |

## 256-lead MQFP-F Package



|    | mm        |       | mils     |       |
|----|-----------|-------|----------|-------|
|    | Min       | Max   | Min      | Max   |
| A  | 2.41      | 3.18  | .095     | .125  |
| C  | 0.10      | 0.20  | .004     | .008  |
| D  | 53.23     | 55.74 | 2.095    | 2.195 |
| D1 | 36.83     | 37.34 | 1.450    | 1.470 |
| E  | 53.23     | 55.74 | 2.095    | 2.195 |
| E1 | 36.83     | 37.34 | 1.450    | 1.470 |
| e  | 0.508 BSC |       | .020 BSC |       |
| f  | 0.15      | 0.25  | .006     | .010  |
| A1 | 2.06      | 2.56  | .081     | .101  |
| A2 | 0.05      | 0.36  | .002     | .014  |
| L  | 8.20      | 9.20  | .323     | .362  |
| N1 | 64        |       | 64       |       |
| N2 | 64        |       | 64       |       |

## 256-lead MQFP-F Pin Assignments

**Table 10.** Pin Assignments

| Pin | Signal | Pin | Signal   | Pin | Signal                      | Pin | Signal                       |
|-----|--------|-----|----------|-----|-----------------------------|-----|------------------------------|
| 1   | GPIINT | 65  | D[0]     | 129 | RA[0]                       | 193 | DXFER                        |
| 2   | GPI[7] | 66  | RSIZE[1] | 130 | VCCO                        | 194 | $\overline{\text{MEXC}}$     |
| 3   | VCCO   | 67  | RSIZE[0] | 131 | VSSO                        | 195 | VCCO                         |
| 4   | VSSO   | 68  | RASI[3]  | 132 | RAPAR                       | 196 | VSSO                         |
| 5   | GPI[6] | 69  | VCCO     | 133 | RASPAR                      | 197 | $\overline{\text{RESET}}$    |
| 6   | GPI[5] | 70  | VSSO     | 134 | DPAR                        | 198 | $\overline{\text{SYSRESET}}$ |
| 7   | GPI[4] | 71  | RASI[2]  | 135 | VCCO                        | 199 | BA[1]                        |
| 8   | GPI[3] | 72  | RASI[1]  | 136 | VSSO                        | 200 | BA[0]                        |
| 9   | VCCO   | 73  | RASI[0]  | 137 | SYSCLK                      | 201 | CB[6]                        |
| 10  | VSSO   | 74  | RA[31]   | 138 | TDO                         | 202 | CB[5]                        |
| 11  | GPI[2] | 75  | RA[30]   | 139 | $\overline{\text{TRST}}$    | 203 | VCCO                         |
| 12  | GPI[1] | 76  | VCCO     | 140 | TMS                         | 204 | VSSO                         |
| 13  | GPI[0] | 77  | VSSO     | 141 | TDI                         | 205 | CB[4]                        |
| 14  | D[31]  | 78  | RA[29]   | 142 | TCK                         | 206 | CB[3]                        |
| 15  | D[30]  | 79  | RA[28]   | 143 | CLK2                        | 207 | CB[2]                        |
| 16  | VCCO   | 80  | RA[27]   | 144 | $\overline{\text{DRDY}}$    | 208 | CB[1]                        |
| 17  | VSSO   | 81  | VCCO     | 145 | DMAAS                       | 209 | VCCO                         |
| 18  | D[29]  | 82  | VSSO     | 146 | VCCO                        | 210 | VSSO                         |
| 19  | D[28]  | 83  | RA[26]   | 147 | VSSO                        | 211 | CB[0]                        |
| 20  | VCCI   | 84  | RA[25]   | 148 | $\overline{\text{DMAGNT}}$  | 212 | $\overline{\text{ALE}}$      |
| 21  | VSSI   | 85  | RA[24]   | 149 | $\overline{\text{EXMCS}}$   | 213 | VCCI                         |
| 22  | D[27]  | 86  | VCCI     | 150 | VCCI                        | 214 | VSSI                         |
| 23  | D[26]  | 87  | VSSI     | 151 | VSSI                        | 215 | $\overline{\text{PROM8}}$    |
| 24  | VCCO   | 88  | VCCO     | 152 | $\overline{\text{DMAREQ}}$  | 216 | $\overline{\text{ROMCS}}$    |
| 25  | VSSO   | 89  | VSSO     | 153 | $\overline{\text{BUSERR}}$  | 217 | $\overline{\text{MEMCS[9]}}$ |
| 26  | D[25]  | 90  | RA[23]   | 154 | $\overline{\text{BUSRDY}}$  | 218 | VCCO                         |
| 27  | D[24]  | 91  | RA[22]   | 155 | $\overline{\text{ROMWRT}}$  | 219 | VSSO                         |
| 28  | D[23]  | 92  | RA[21]   | 156 | $\overline{\text{NOPAR}}$   | 220 | $\overline{\text{MEMCS[8]}}$ |
| 29  | D[22]  | 93  | VCCO     | 157 | $\overline{\text{SYSHALT}}$ | 221 | $\overline{\text{MEMCS[7]}}$ |
| 30  | VCCO   | 94  | VSSO     | 158 | $\overline{\text{CPUHALT}}$ | 222 | $\overline{\text{MEMCS[6]}}$ |
| 31  | VSSO   | 95  | RA[20]   | 159 | VCCO                        | 223 | $\overline{\text{MEMCS[5]}}$ |
| 32  | D[21]  | 96  | RA[19]   | 160 | VSSO                        | 224 | $\overline{\text{MEMCS[4]}}$ |
| 33  | D[20]  | 97  | RA[18]   | 161 | SYSERR                      | 225 | $\overline{\text{MEMCS[3]}}$ |

**Table 10. Pin Assignments (Continued)**

| Pin | Signal | Pin | Signal | Pin | Signal                       | Pin | Signal                       |
|-----|--------|-----|--------|-----|------------------------------|-----|------------------------------|
| 34  | D[19]  | 98  | VCCO   | 162 | SYSAV                        | 226 | VCCO                         |
| 35  | D[18]  | 99  | VSSO   | 163 | EXTINT[4]                    | 227 | VSSO                         |
| 36  | VCCO   | 100 | RA[17] | 164 | EXTINT[3]                    | 228 | $\overline{\text{MEMCS}}[2]$ |
| 37  | VSSO   | 101 | RA[16] | 165 | EXTINT[2]                    | 229 | $\overline{\text{MEMCS}}[1]$ |
| 38  | D[17]  | 102 | RA[15] | 166 | EXTINT[1]                    | 230 | $\overline{\text{MEMCS}}[0]$ |
| 39  | D[16]  | 103 | VCCO   | 167 | EXTINT[0]                    | 231 | VCCI                         |
| 40  | VCCI   | 104 | VSSO   | 168 | VCCI                         | 232 | VSSI                         |
| 41  | VSSI   | 105 | RA[14] | 169 | VSSI                         | 233 | $\overline{\text{OE}}$       |
| 42  | D[15]  | 106 | VCCI   | 170 | EXTINTACK                    | 234 | VCCO                         |
| 43  | D[14]  | 107 | VSSI   | 171 | $\overline{\text{IUERR}}$    | 235 | VSSO                         |
| 44  | VCCO   | 108 | RA[13] | 172 | VCCO                         | 236 | $\overline{\text{MEMWR}}$    |
| 45  | VSSO   | 109 | RA[12] | 173 | VSSO                         | 237 | $\overline{\text{BUFFEN}}$   |
| 46  | D[13]  | 110 | VCCO   | 174 | CPAR                         | 238 | DDIR                         |
| 47  | D[12]  | 111 | VSSO   | 175 | TXA                          | 239 | VCCO                         |
| 48  | D[11]  | 112 | RA[11] | 176 | RXA                          | 240 | VSSO                         |
| 49  | D[10]  | 113 | RA[10] | 177 | RXB                          | 241 | $\overline{\text{DDIR}}$     |
| 50  | VCCO   | 114 | RA[9]  | 178 | TXB                          | 242 | $\overline{\text{MHOLD}}$    |
| 51  | VSSO   | 115 | VCCO   | 179 | $\overline{\text{IOWR}}$     | 243 | $\overline{\text{MDS}}$      |
| 52  | D[9]   | 116 | VSSO   | 180 | $\overline{\text{IOSEL}}[3]$ | 244 | WDCLK                        |
| 53  | D[8]   | 117 | RA[8]  | 181 | VCCO                         | 245 | IWDE                         |
| 54  | D[7]   | 118 | RA[7]  | 182 | VSSO                         | 246 | EWDINT                       |
| 55  | D[6]   | 119 | RA[6]  | 183 | $\overline{\text{IOSEL}}[2]$ | 247 | TMODE[1]                     |
| 56  | VCCO   | 120 | VCCO   | 184 | $\overline{\text{IOSEL}}[1]$ | 248 | TMODE[0]                     |
| 57  | VSSO   | 121 | VSSO   | 185 | $\overline{\text{IOSEL}}[0]$ | 249 | DEBUG                        |
| 58  | D[5]   | 122 | RA[5]  | 186 | WRT                          | 250 | INULL                        |
| 59  | D[4]   | 123 | RA[4]  | 187 | $\overline{\text{WE}}$       | 251 | DIA                          |
| 60  | D[3]   | 124 | RA[3]  | 188 | VCCO                         | 252 | VCCO                         |
| 61  | D[2]   | 125 | VCCO   | 189 | VSSO                         | 253 | VSSO                         |
| 62  | VCCO   | 126 | VSSO   | 190 | RD                           | 254 | FLUSH                        |
| 63  | VSSO   | 127 | RA[2]  | 191 | RLDSTO                       | 255 | INST                         |
| 64  | D[1]   | 128 | RA[1]  | 192 | LOCK                         | 256 | RTC                          |



## Ordering Information

**Table 11.** Possible Order Entries

| Part-Number     | Supply Voltage | Temperature Range | Maximum Speed | Packaging | Quality Flow         |
|-----------------|----------------|-------------------|---------------|-----------|----------------------|
| TSC695F-25MA-E  | 5V             | Military          | 25            | MQFP-F256 | Engineering Samples  |
| TSC695F-25MB-E  | 5V             | Military          | 25            | Die       | Engineering Samples  |
| TSC695F-25SASB  | 5V             | Military          | 25            | MQFP-F256 | ESA level B          |
| TSC695F-25MA    | 5V             | Military          | 25            | MQFP-F256 | Military temperature |
| TSC695F-25/883  | 5V             | Military          | 25            | MQFP-F256 | 883 level B          |
| 5962-005401-QXC | 5V             | Military          | 25            | MQFP-F256 | QML-V                |
| 5962-005401-VXC | 5V             | Military          | 25            | Die       | QML-Q                |
| 5962-005401-V9A | 5V             | Military          | 25            | Die       | QML-V                |



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