

- **High-Performance Static CMOS Technology**
 - 100 MHz (10-ns Cycle Time)
 - Low-Power (1.8-V Core, 3.3-V I/O) Design
 - 3.3-V Flash Voltage
- **JTAG Boundary Scan Support†**
- **High-Performance 32-Bit CPU (TMS320C28x)**
 - 16 x 16 and 32 x 32 MAC Operations
 - 16 x 16 Dual MAC
 - Harvard Bus Architecture
 - Atomic Operations
 - Fast Interrupt Response and Processing
 - Unified Memory Programming Model
 - Code-Efficient (in C/C++ and Assembly)
- **On-Chip Memory**
 - F2808: 64-KW Flash, 18-KW SARAM
 - F2806: 32-KW Flash, 10-KW SARAM
 - F2801: 16-KW Flash, 6-KW SARAM
 - 1K x 16 OTP ROM
- **Boot ROM (4K x 16)**
 - With Software Boot Modes
 - Standard Math Tables
- **Clock and System Control**
 - Dynamic PLL Ratio Changes Supported
 - On-Chip Oscillator
 - Clock-Fail-Detect Mode
 - Watchdog Timer Module
- **Three External Interrupts (Any GPIO Pin Can Be the Interrupt Source)**
- **Peripheral Interrupt Expansion (PIE) Block That Supports up to 96 Peripheral Interrupts**
- **128-Bit Security Key/Lock**
 - Protects Flash/OTP
 - Prevents Firmware Reverse Engineering
- **Three 32-Bit CPU-Timers**
- **Up to 32 Individually Programmable, Multiplexed General-Purpose Input/Output (GPIO) Pins**
- **Enhanced Control Peripherals**
 - Up to 16 PWM Outputs
 - Up to Four Capture Inputs
 - Up to Two Quadrature Encoder Interfaces
 - Up to Six 32-bit Timers
 - Up to Six 16-bit Timers
- **Serial Port Peripherals**
 - Up to 4 Serial Peripheral Interfaces (SPIs)
 - Up to 2 Serial Communications Interfaces (SCIs), Standard UART
 - Up to 2 Enhanced Controller Area Networks (eCANs)
 - One Inter-Integrated-Circuit (I²C) Bus
- **12-Bit ADC, 16 Channels**
 - 2 x 8 Channel Input Multiplexer
 - Two Sample-and-Hold
 - Single/Simultaneous Conversions
 - Fast Conversion Rate: 160 ns/6.25 MSPS
- **Advanced Emulation Features**
 - Analysis and Breakpoint Functions
 - Real-Time Debug via Hardware
- **Development Tools Include**
 - ANSI C/C++ Compiler/Assembler/Linker
 - Supports TMS320C24x™/240x Instructions
 - Code Composer Studio™ IDE
 - DSP/BIOS™
 - JTAG Scan Controllers† [Texas Instruments (TI) or Third-Party]
 - Evaluation Modules
 - Broad Third-Party Digital Motor Control Support
- **Low-Power Modes and Power Savings**
 - IDLE, STANDBY, HALT Modes Supported
 - Disable Individual Peripheral Clocks
- **Package Options**
 - Thin Quad Flatpack (LQFP) (2808, 2806, 2801)
 - MicroStar BGA (2808, 2806)
- **Temperature Options:**
 - A: –40°C to 85°C
 - S: –40°C to 125°C



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† IEEE Standard 1149.1–1990, IEEE Standard Test-Access Port

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TMS320F2801, TMS320F2806, TMS320F2808 DIGITAL SIGNAL PROCESSORS

SPRS230 – OCTOBER 2003

description

The TMS320F2808, TMS320F2806, and TMS320F2801 devices, members of the TMS320C28x™ DSP generation, are highly integrated, high-performance solutions for demanding control applications.

Throughout this document, TMS320F2808, TMS320F2806, and TMS320F2801 are abbreviated as F2808, F2806, and F2801, respectively.

Table 1 provides a summary of each device's features.

Table 1. Hardware Features

FEATURE	F2808	F2806	F2801
Instruction cycle (at 100 MHz)	10 ns	10 ns	10 ns
Single-access RAM (SARAM) (16-bit word)	18 kW† (L0, L1, M0, M1, H0)	10 kW† (L0, L1, M0, M1)	6 kW† (L0, M0, M1)
3.3-V on-chip flash (16-bit word)	64 kW	32 kW	16 kW
Code security for on-chip flash	Yes	Yes	Yes
Boot ROM (4K)	Yes	Yes	Yes
One-time programmable (OTP) ROM	Yes	Yes	Yes
External memory interface	—	—	—
Enhanced PWM outputs (six 16-bit timer-based modules with 2 PWM outputs/module)	12	12	6
Enhanced 32-bit CAPTURE inputs or auxiliary PWM outputs	4	4	2
Enhanced 32-bit QEP channels (four inputs/channel)	2	2	1
Watchdog timer	Yes	Yes	Yes
12-Bit ADC	Yes	Yes	Yes
– Channels	16	16	16
32-Bit CPU timers	3	3	3
SPI	4	4	2
SCI	2	2	1
CAN	2	1	1
I ² C	1	1	1
Digital I/O pins (shared)	32	32	32
External interrupts	3	3	3
Supply voltage	1.8-V Core, 3.3-V I/O	1.8-V Core, 3.3-V I/O	1.8-V Core, 3.3-V I/O
Packaging	100 Pin	100 Pin	100 Pin
Temperature options	A: –40°C to 85°C	Yes	Yes
	S: –40°C to 125°C	Yes	Yes
Product status	PP	PP	PP

† L0 and L1 – 4K X 16 each single-access RAM (SARAM) (0 wait-state)
M0 and M1 – 1K X 16 each SARAM (0 wait-state)
H0 – 8K X 16 (1 wait-state).

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PRODUCT PREVIEW

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