

5-V Low-Drop Voltage Regulator

TLE 4275

Preliminary Data

Features

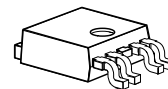
- Output voltage $5\text{ V} \pm 2\%$
- Very low current consumption
- Power-on and undervoltage reset
- Reset low down to $V_O = 1\text{ V}$
- Very low-drop voltage
- Short-circuit-proof
- Reverse polarity proof
- Suitable for use in automotive electronics

Type	Ordering Code	Package
▼ TLE 4275 D	Q67006-A9354	P-TO252-5-1 (SMD)
▼ TLE 4275 G	Q67006-A9343	P-TO263-5-1 (SMD)
▼ TLE 4275	Q67000-A9342	P-TO220-5-11

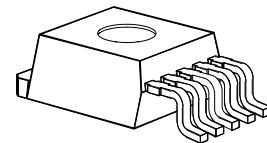
▼ New type

Functional Description

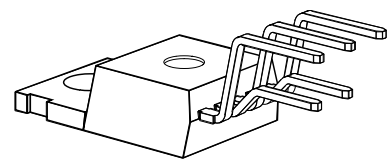
The TLE 4275 is a monolithic integrated low-drop voltage regulator in a 5 pin TO-package. An input voltage up to 45 V is regulated to $V_O = 5.0\text{ V}$. The IC is able to drive loads up to 450 mA and is short-circuit proof. At over temperature the TLE 4275 is disabled by the incorporated temperature protection. A reset signal is generated for an output voltage V_O of typ. 4.65 V. The delay time can be programmed by the external delay capacitor.



P-TO252-5-1 (D-PAK)



P-TO263-5-1



P-TO220-5-11

Dimensioning Information on External Components

The input capacitor C_i is necessary for compensating line influences. Using a resistor of approx. $1\ \Omega$ in series with C_i , the oscillating of input inductivity and input capacitance can be damped. The output capacitor C_o is necessary for the stability of the regulation circuit. Stability is guaranteed at values $C_o \geq 22\ \mu\text{F}$ and an ESR of $\leq 5\ \Omega$ within the operating temperature range.

Circuit Description

The control amplifier compares a reference voltage to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any oversaturation of the power element. The IC also incorporates a number of internal circuits for protection against:

- Overload
- Over-temperature
- Reverse polarity

Pin Configuration (top view)

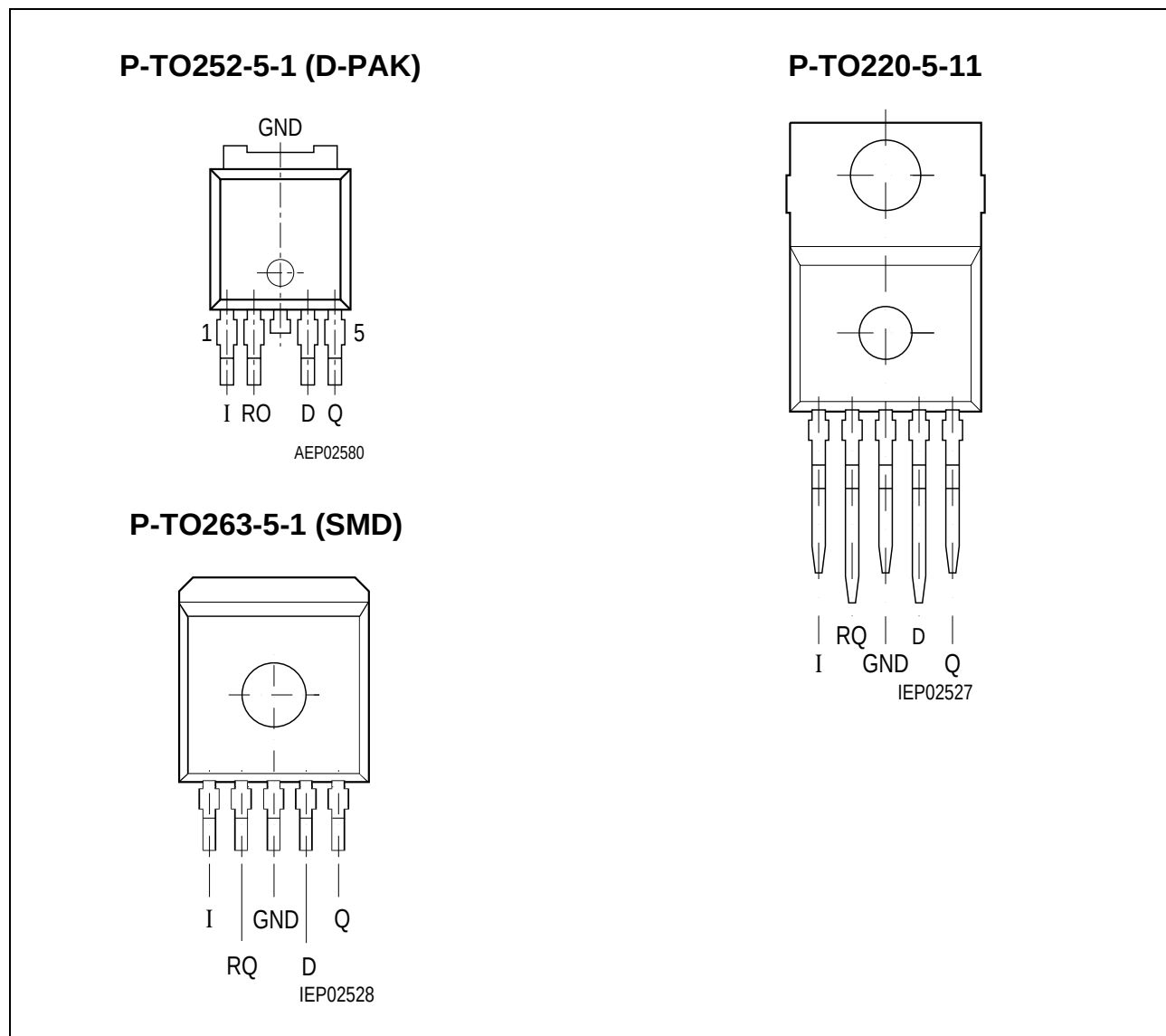


Figure 1

Pin Definitions and Functions

Pin No.	Symbol	Function
1	I	Input ; block to ground directly at the IC with a ceramic capacitor.
2	RQ	Reset Output ; open collector output
3	GND	Ground ; Pin 3 internally connected to heatsink
4	D	Reset Delay ; connected capacitor to GND for setting delay time
5	Q	Output ; block to ground with a $\geq 22 \mu\text{F}$ capacitor, ESR $< 5 \Omega$ at 10 kHz.

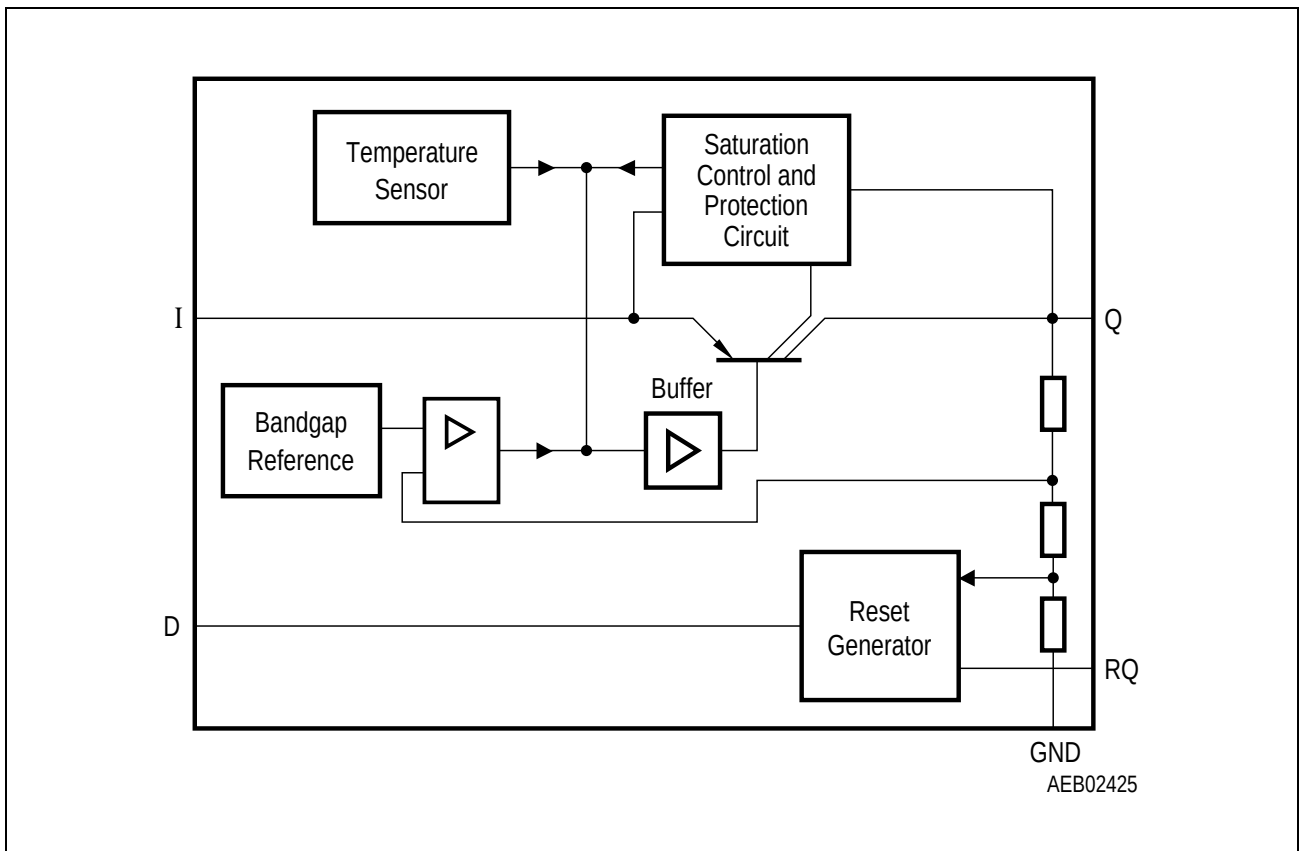


Figure 2
Block Diagram

Absolute Maximum Ratings $T_j = -40$ to $150\text{ }^{\circ}\text{C}$

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		

Voltage Regulator**Input**

Voltage	V_I	- 42	45	V	–
Current	I_I	–	–	–	Internally limited

Output

Voltage	V_Q	- 1.0	16	V	–
Current	I_Q	–	–	–	Internally limited

Reset Output

Voltage	V_{RO}	- 0.3	25	V	–
Current	I_{RO}	- 5	5	mA	–

Reset Delay

Voltage	V_D	- 0.3	7	V	–
Current	I_D	- 2	2	mA	–

Temperature

Junction temperature	T_j	–	150	$^{\circ}\text{C}$	–
Storage temperature	T_{stg}	- 50	150	$^{\circ}\text{C}$	–

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Input voltage	V_I	5.5	42	V	–
Junction temperature	T_j	– 40	150	°C	–

Thermal Resistance

Junction case	R_{thjc}	–	4	K/W	–
Junction ambient	R_{thja}	–	70	K/W	TO263
Junction ambient	R_{thja}	–	70	K/W	TO252 ¹⁾
Junction ambient	R_{thja}	–	65	K/W	TO220

1) Soldered in, minimal footprint

Characteristics

$V_I = 13.5 \text{ V}$; $-40 \text{ °C} < T_j < 150 \text{ °C}$ (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Measuring Condition
		min.	typ.	max.		

Output

Output voltage	V_Q	4.9	5.0	5.1	V	$5 \text{ mA} < I_Q < 400 \text{ mA}$ $6 \text{ V} < V_I < 40 \text{ V}$
Output current limitation ¹⁾	I_Q	450	700	–	mA	–
Current consumption; $I_q = I_I - I_Q$	I_q	–	150	200	μA	$I_Q = 1 \text{ mA}$; $T_j = 25 \text{ °C}$
Current consumption; $I_q = I_I - I_Q$	I_q	–	150	220	μA	$I_Q = 1 \text{ mA}$; $T_j \leq 85 \text{ °C}$
Current consumption; $I_q = I_I - I_Q$	I_q I_q	–	5 12	10 22	mA mA	$I_Q = 250 \text{ mA}$ $I_Q = 400 \text{ mA}$
Drop voltage ¹⁾	V_{dr}	–	250	500	mV	$I_Q = 300 \text{ mA}$ $V_{dr} = V_I - V_Q$
Load regulation	ΔV_Q	–	15	30	mV	$I_Q = 5 \text{ mA to } 400 \text{ mA}$
Line regulation	ΔV_Q	– 15	5	15	mV	$\Delta V_I = 8 \text{ V to } 32 \text{ V}$ $I_Q = 5 \text{ mA}$

Test Circuit

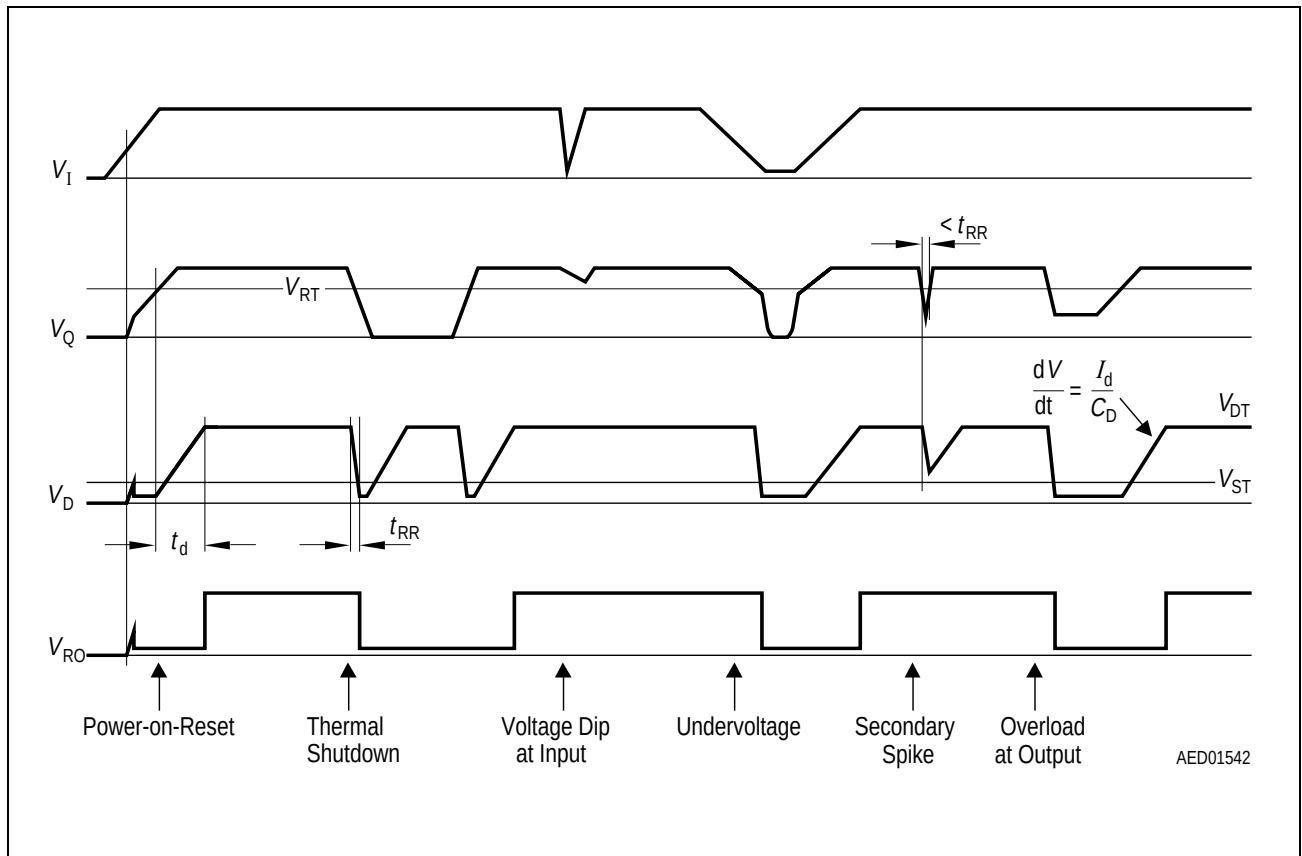
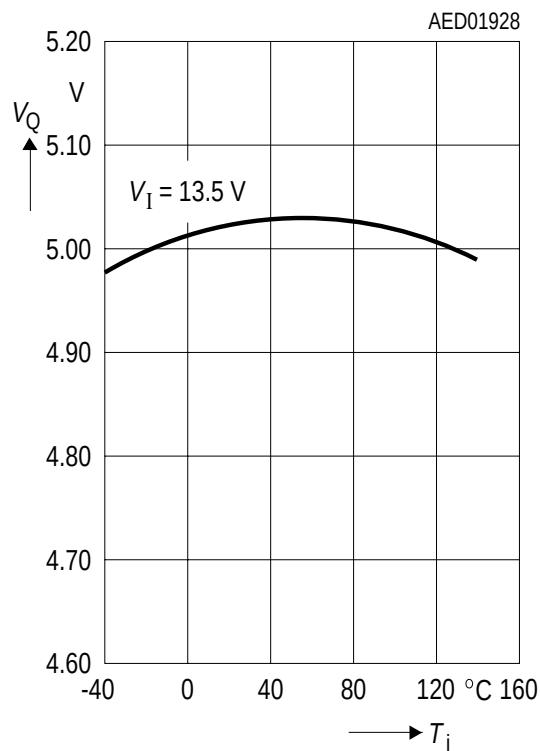
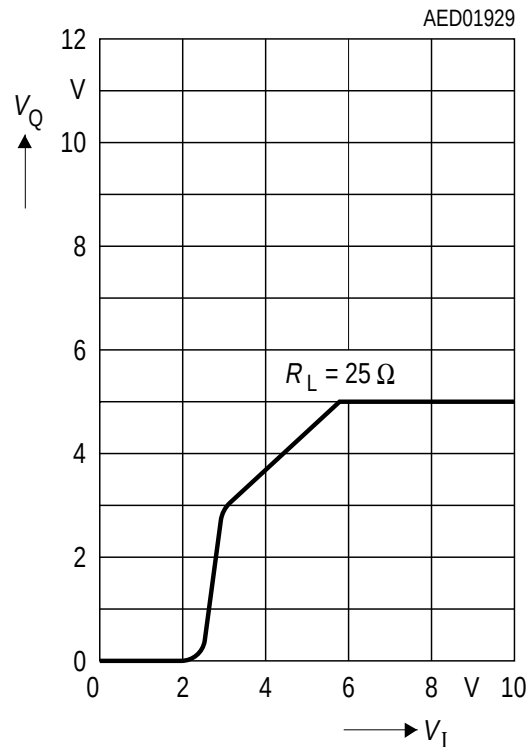


Figure 4
Reset Timing

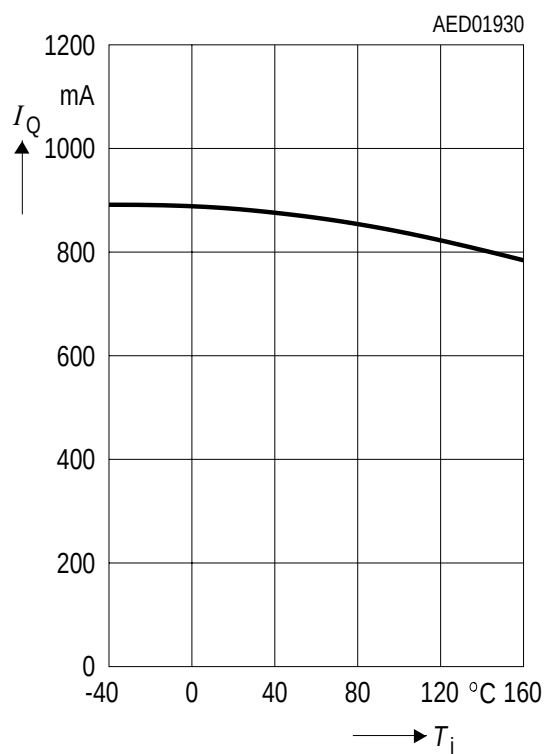
Output Voltage V_Q versus Temperature T_j



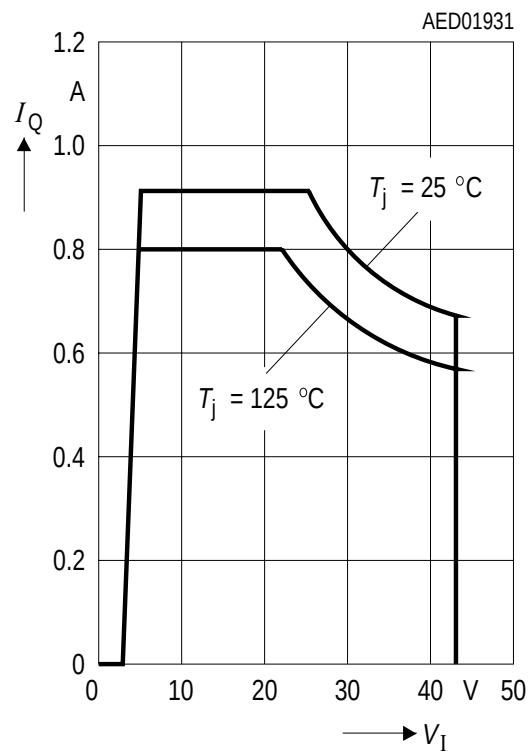
Output Voltage V_Q versus Input Voltage V_I



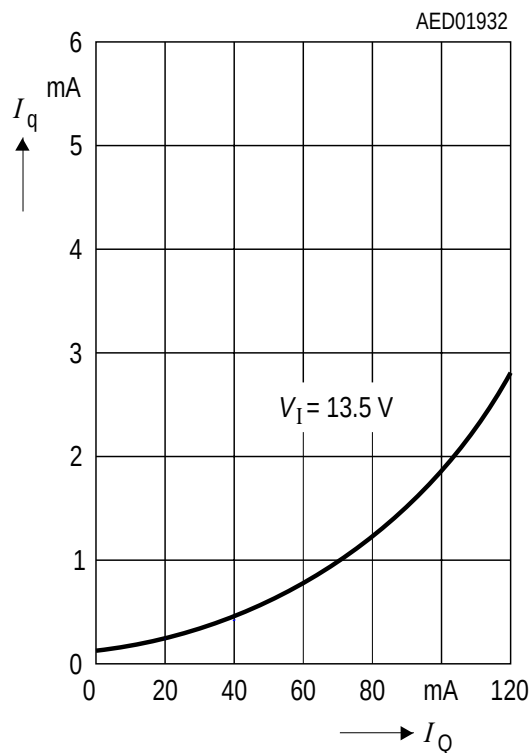
Output Current I_Q versus Temperature T_j



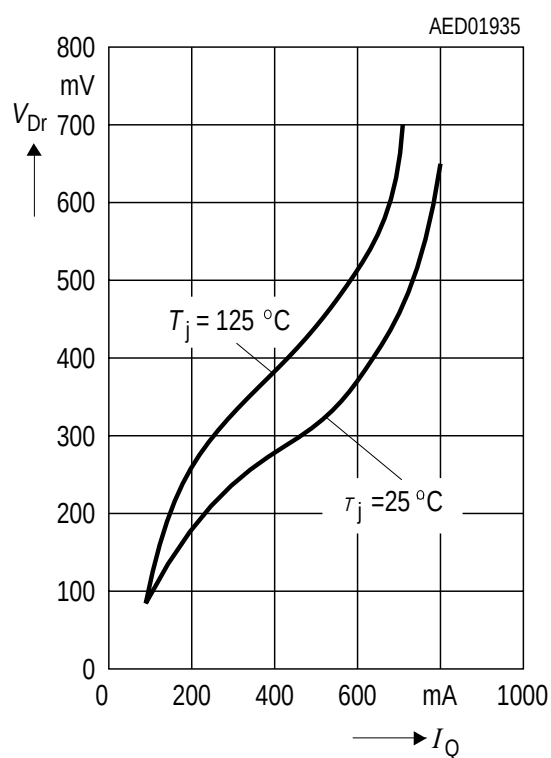
Output Current I_Q versus Input Voltage V_I



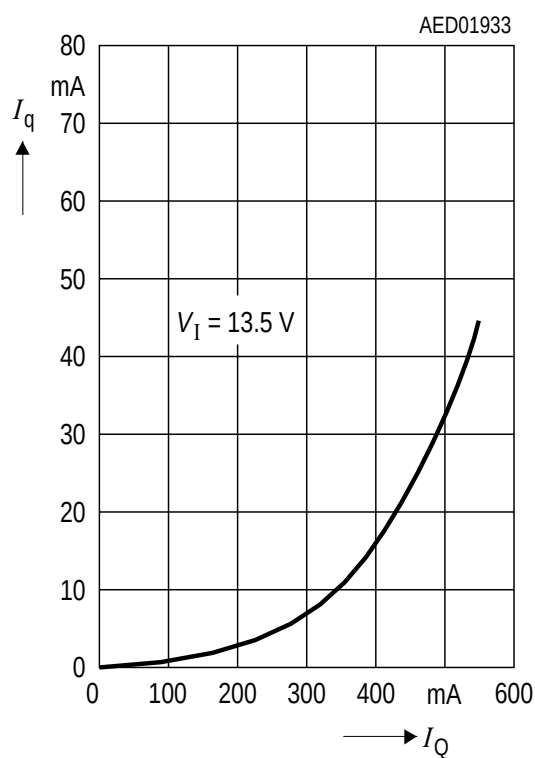
**Current Consumption I_q
versus Output Current I_Q**



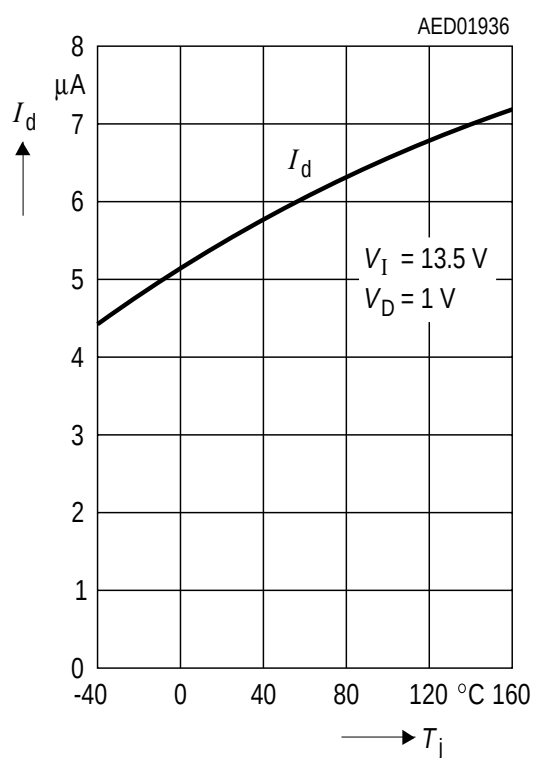
**Drop Voltage V_{Dr} versus
Output Current I_Q**



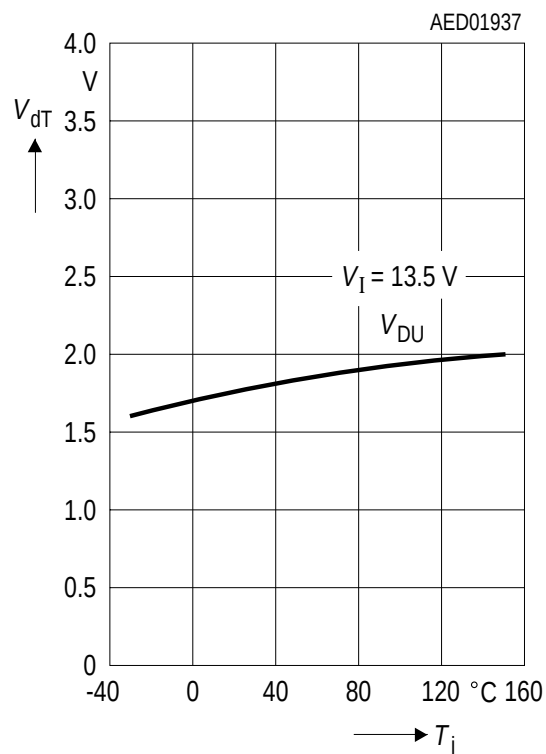
**Current Consumption I_q
versus Output Current I_Q**



**Charge Current I_d
versus Temperature T_j**

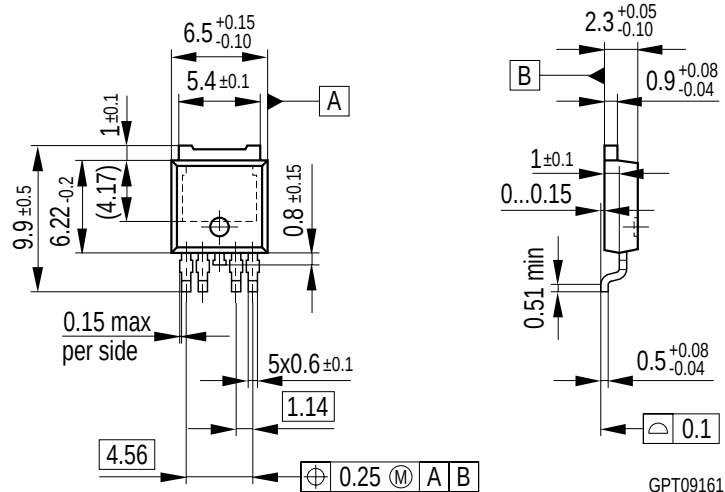


**Delay Switching Threshold V_{DU}
versus Temperature T_j**



Package Outlines

P-TO252-5-1 (D-PAK) (Plastic Transistor Single Outline)



Sorts of Packing

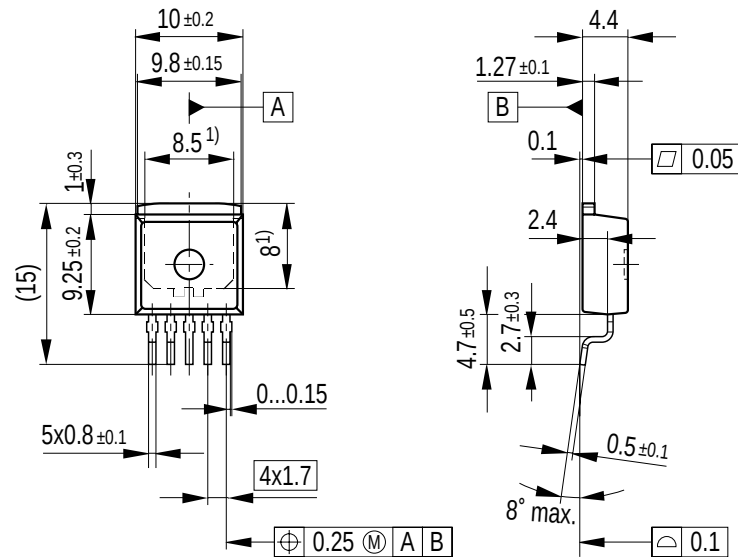
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

P-TO263-5-1 (SMD)

(Plastic Transistor Single Outline)



¹⁾ Typical

All metal surfaces tin plated, except area of cut.

GPT09113

Sorts of Packing

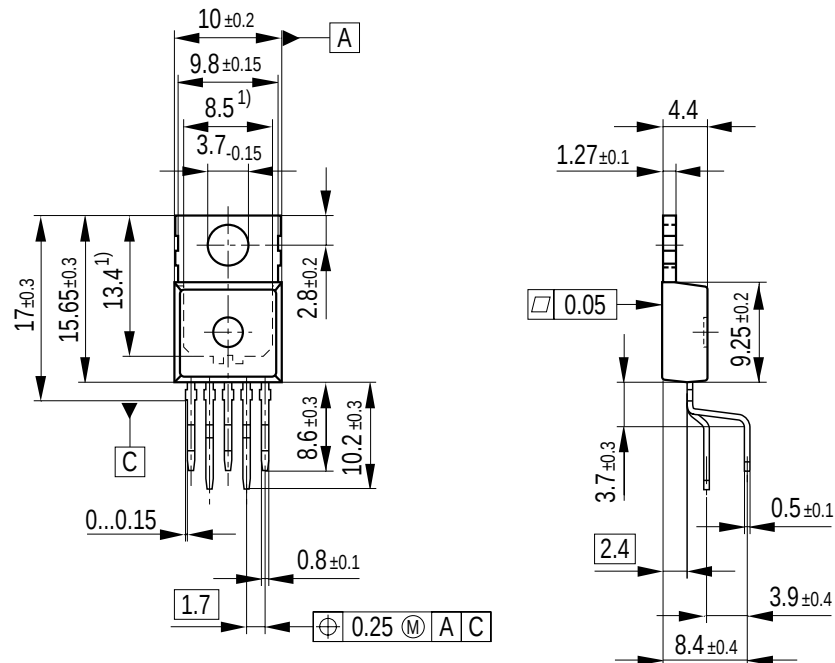
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SMD = Surface Mounted Device

Dimensions in mm

P-TO220-5-11

(Plastic Transistor Single Outline)



¹⁾ Typical

All metal surfaces tin plated, except area of cut.

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Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

Dimensions in mm