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P1 98.2

MOS FIELD EFFECT POWER TRANSISTORS

2SJ327, 2SJ327-Z

SWITCHING

P-CHANNEL POWER MOS FET

INDUSTRIAL USE

DESCRIPTION

The 2SJ327 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} = 0.13 \Omega$ TYP. ($V_{GS} = -10$ V, $I_D = -2$ A)
 $R_{DS(on)} = 0.21 \Omega$ TYP. ($V_{GS} = -4$ V, $I_D = -1.6$ A)
- Low C_{iss} $C_{iss} = 750$ pF TYP.
- Built-in G-S Gate Protection Diode

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

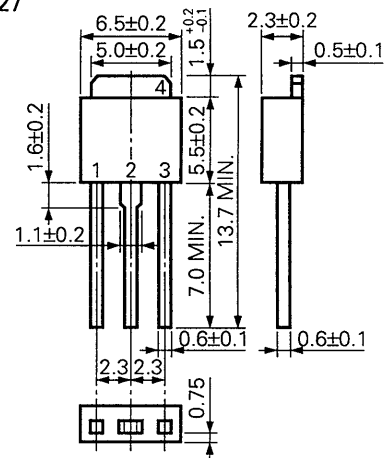
Drain to Source Voltage	V_{DSS}	-60	V
Gate to Source Voltage (AC)	V_{GSS}	± 20	V
Gate to Source Voltage (DC)	V_{GSS}	-20, +10	V
Drain Current (DC)	$I_{D(DC)}$	± 4.0	A
Drain Current (pulse)	$I_{D(pulse)^*}$	± 16	A
Total Power Dissipation ($T_c = 25^\circ\text{C}$)	P_{T1}	20	W
Total Power Dissipation ($T_a = 25^\circ\text{C}$)	P_{T2}	1.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

* $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

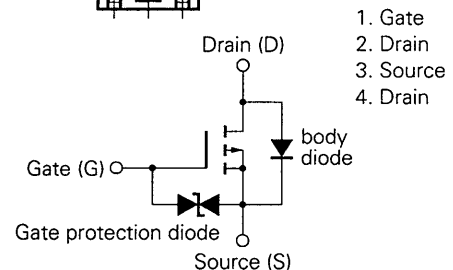
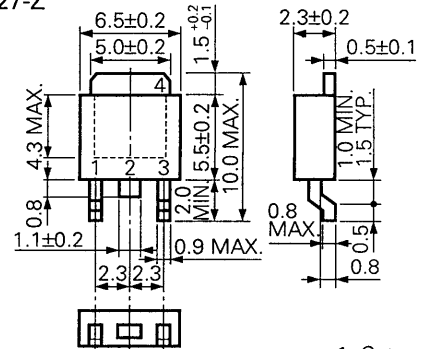
PACKAGE DIMENSIONS

in millimeters

2SJ327



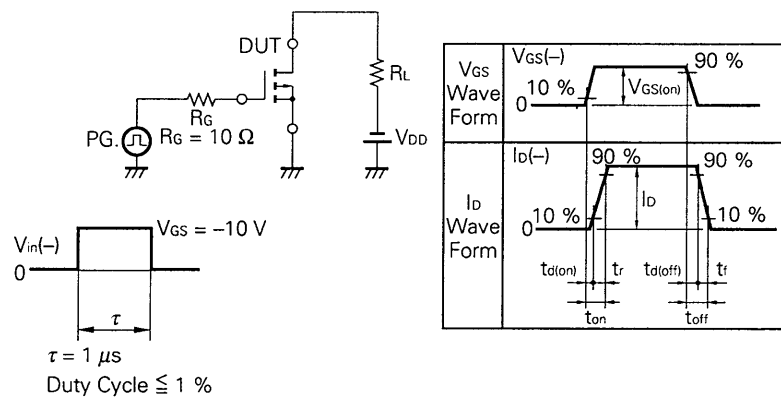
2SJ327-Z



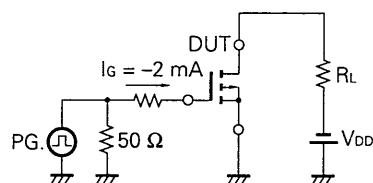
ELECTRICAL CHARACTERISTICS ($T_a = 25\text{ }^{\circ}\text{C}$)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	$R_{DS(on)}$		0.13	0.17	Ω	$V_{GS} = -10\text{ V}$, $I_D = -2.0\text{ A}$
Drain to Source On-state Resistance	$R_{DS(on)}$		0.21	0.34	Ω	$V_{GS} = -4\text{ V}$, $I_D = -1.6\text{ A}$
Gate to Source Cutoff Voltage	$V_{GS(off)}$	-1.0	-1.5	-2.0	V	$V_{DS} = -10\text{ V}$, $I_D = -1\text{ mA}$
Forward Transfer Admittance	$ y_{fs} $	3.0	3.8		S	$V_{DS} = -10\text{ V}$, $I_D = -2.0\text{ A}$
Drain Leakage Current	I_{DSS}			-10	μA	$V_{DS} = -60\text{ V}$, $V_{GS} = 0$
Gate to Source Leakage Current	I_{GSS}			± 10	μA	$V_{GS} = \pm 16\text{ V}$, $V_{DS} = 0$
Input Capacitance	C_{iss}		750		pF	$V_{DS} = -10\text{ V}$ $V_{GS} = 0$ $f = 1\text{ MHz}$
Output Capacitance	C_{oss}		410		pF	
Reverse Transfer Capacitance	C_{rss}		165		pF	
Turn-On Delay Time	$t_{d(on)}$		10		ns	$V_{GS(on)} = -10\text{ V}$ $V_{DD} = -30\text{ V}$ $I_D = -2.0\text{ A}$, $R_G = 10\text{ }\Omega$ $R_L = 15\text{ }\Omega$
Rise Time	t_r		35		ns	
Turn-Off Delay Time	$t_{d(off)}$		85		ns	
Fall Time	t_f		45		ns	
Total Gate Charge	Q_G		27		nC	$V_{GS} = -10\text{ V}$ $I_D = -4.0\text{ A}$ $V_{DD} = -48\text{ V}$
Gate to Source Charge	Q_{GS}		2		nC	
Gate to Drain Charge	Q_{GD}		11		nC	
Body Diode Forward Voltage	V_F		0.9		V	$I_F = 4.0\text{ A}$, $V_{GS} = 0$
Reverse Recovery Time	t_{rr}		85		ns	$I_F = 4.0\text{ A}$, $V_{GS} = 0$
Reverse Recovery Charge	Q_{rr}		130		nC	$di/dt = 50\text{ A}/\mu\text{s}$

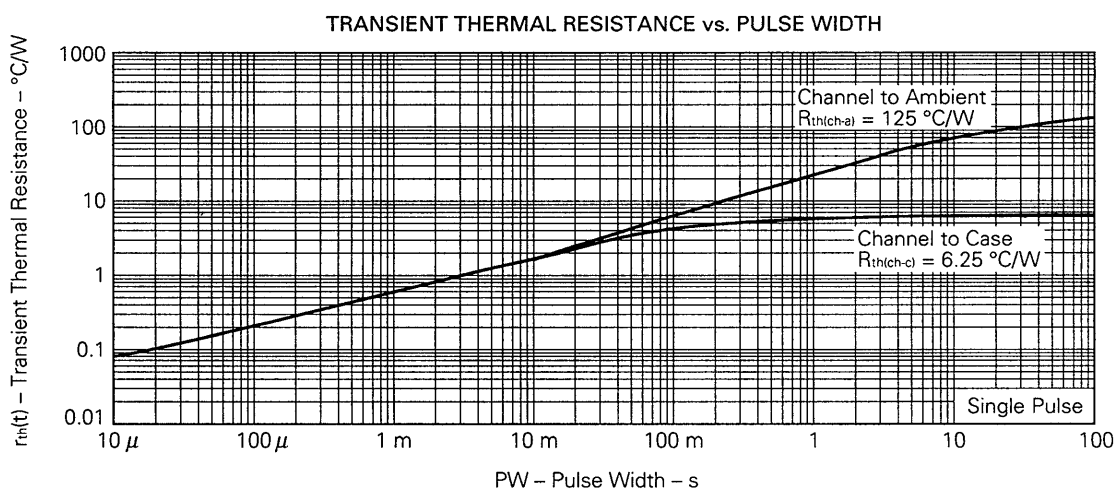
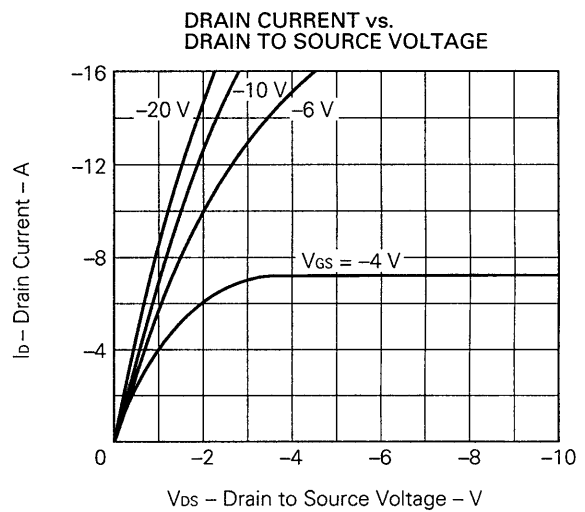
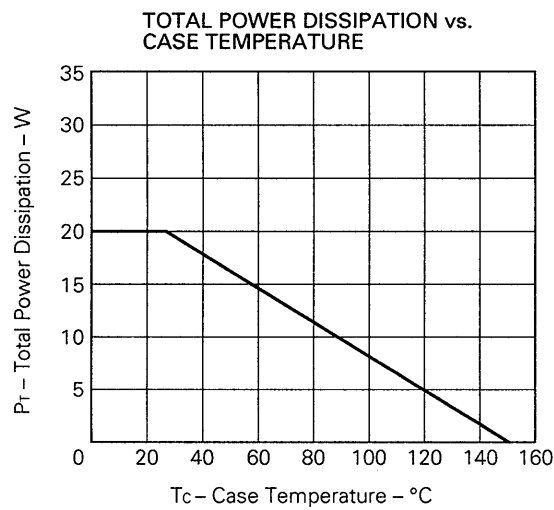
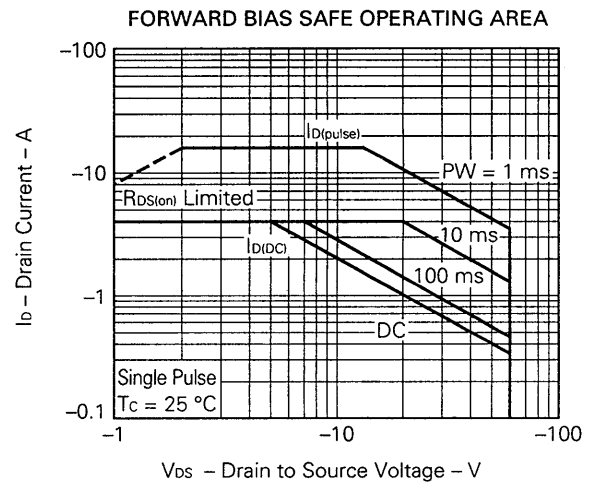
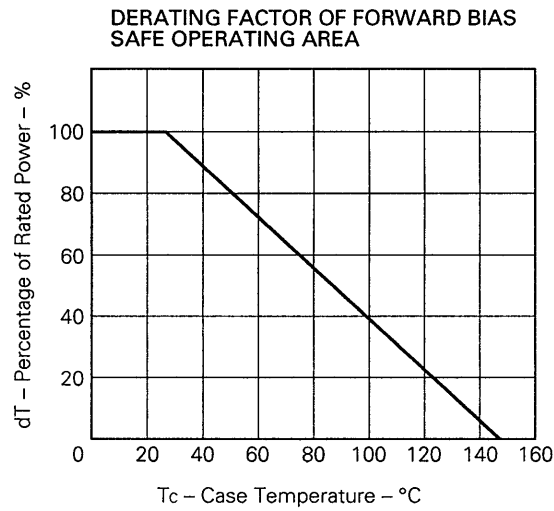
Test Circuit 1: Switching Time

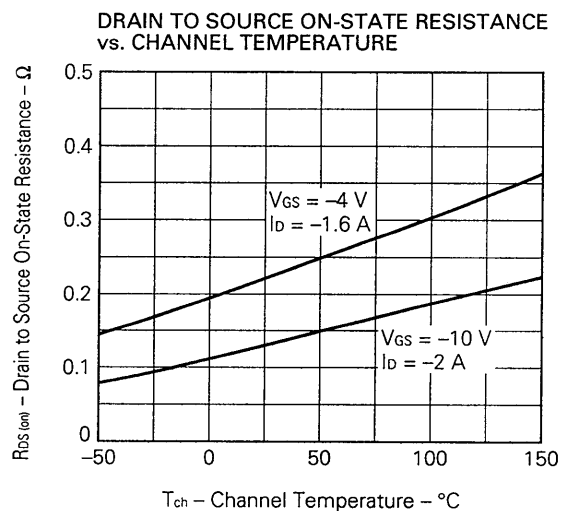
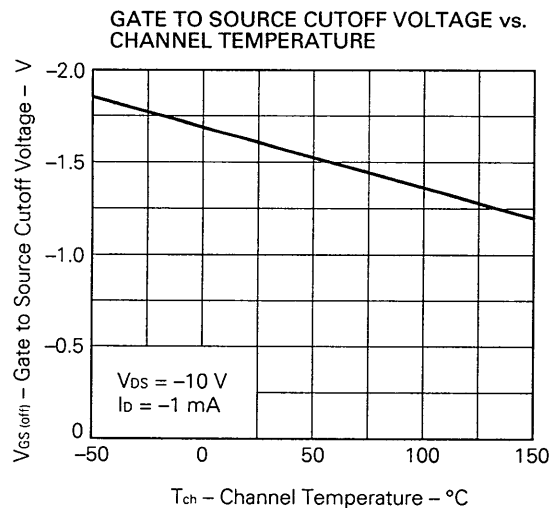
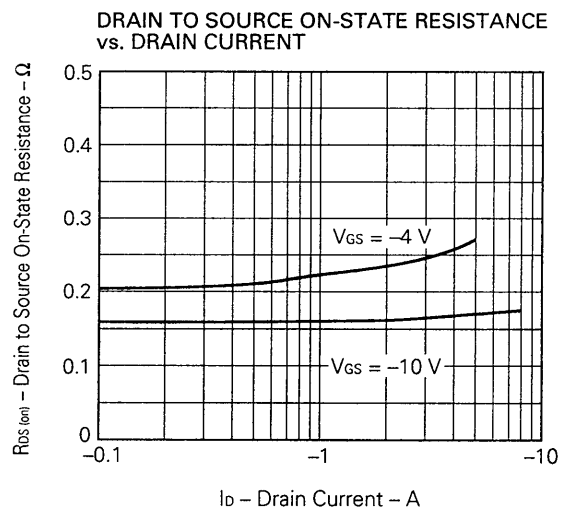
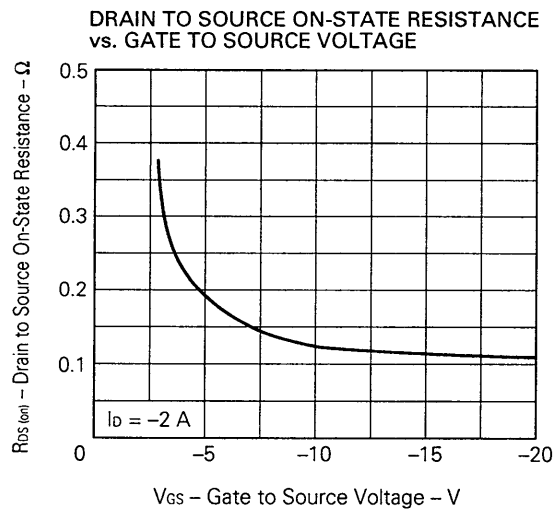
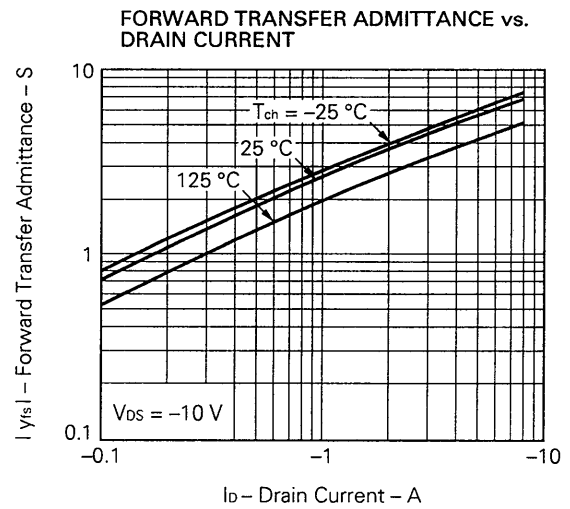
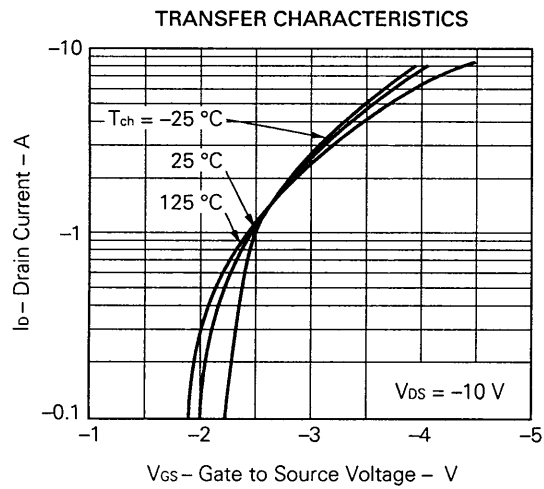


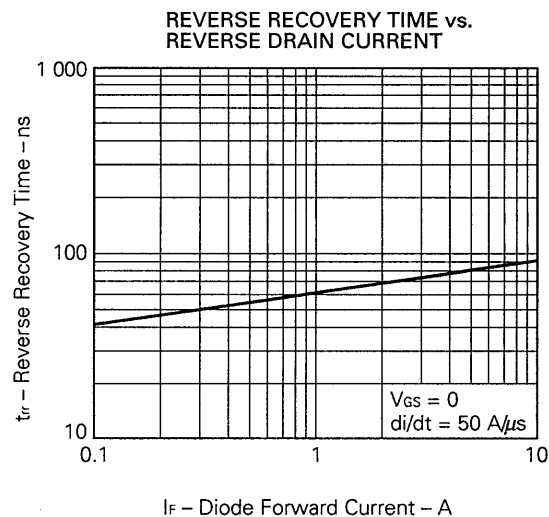
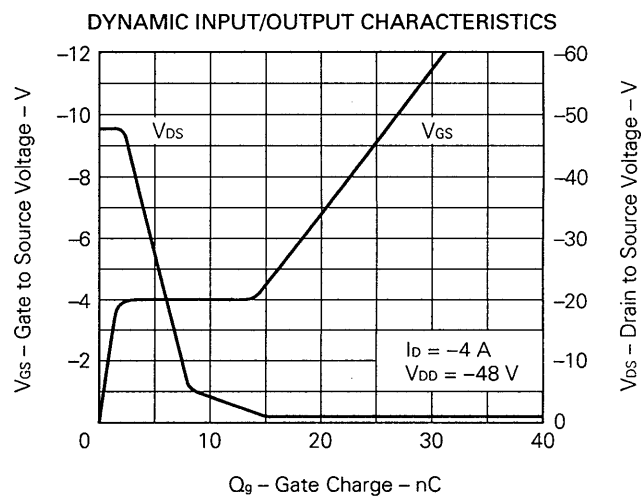
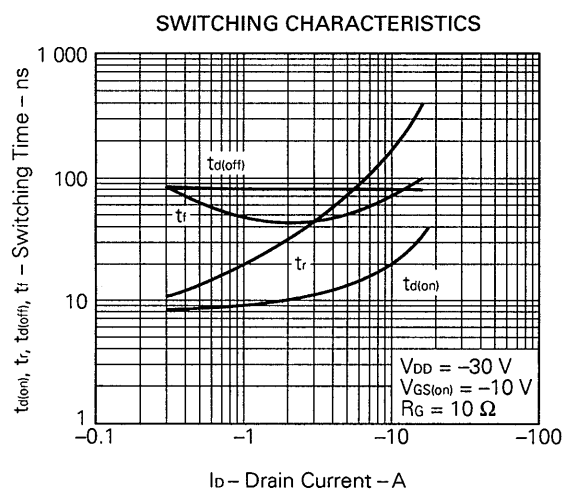
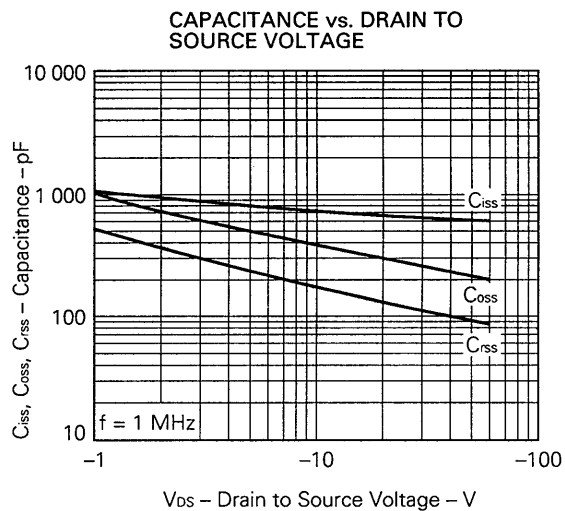
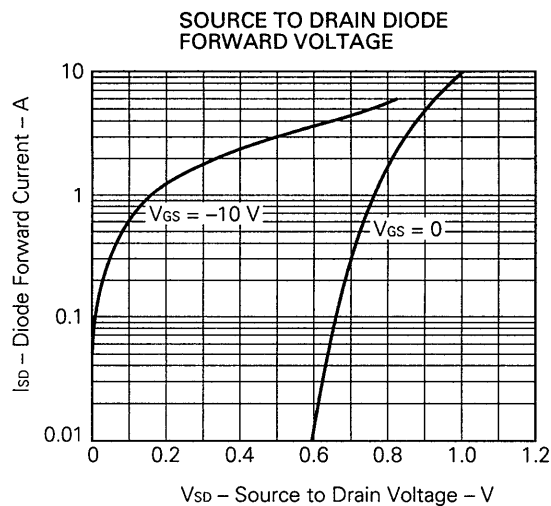
Test Circuit 2: Gate Charge



ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)







Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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