Features

- **Supply voltage up to 40 V**
- **R_{DSon} typ. 0.5 Ω @ 25°C, max. 1Ω @ 150°C**
- **Up to 1.5 A output current**
- **Three high-side and three low-side drivers usable as single outputs or half bridges**
- **Capable to switch all kinds of loads such as DC motors, bulbs, resistors, capacitors and inductors**
- **PWM capability for each output controlled by external PWM signal**
- **No crossover current**
- **Very low quiescent current Is < 10 µA in stand-by mode over total temperature range**
- **Outputs short-circuit protected**
- **Selective overtemperature protection for each switch and overtemperature prewarning**
- **Undervoltage protection**
- **Various diagnosis functions such as shorted output, open load, overtemperature and power-supply fail**
- **Serial data interface, daisy chain capable, up to 2 MHz clock frequency**
- **SO16 power package**

Dual Triple DMOS Output Driver with Serial Input Control

T6819
T6829

Description

T6819 / T6829 are fully protected driver interfaces designed in 0.8 µm BCDMOS technology. It is used to control up to 6 different loads by a microcontroller in automotive and industrial applications.

Each of the 3 high-side and 3 low-side drivers is capable to drive currents up to 1.5 A. Each driver is free configurable and can be controlled separately from a standard serial data interface. Therefore, all kinds of loads such as bulbs, resistors, capacitors and inductors can be combined. The IC design especially supports the applications of H-bridges to drive DC motors. The capability to control each output with an external PWM signal opens additional applications.

Protection is guaranteed in terms of short-circuit conditions, overtemperature and undervoltage. Various diagnosis functions and a very low quiescent current in stand-by mode opens a wide range of applications. Automotive qualification referring to conducted interferences, EMC protection and 2 kV ESD protection give added value and enhanced quality for demanding up-market applications.

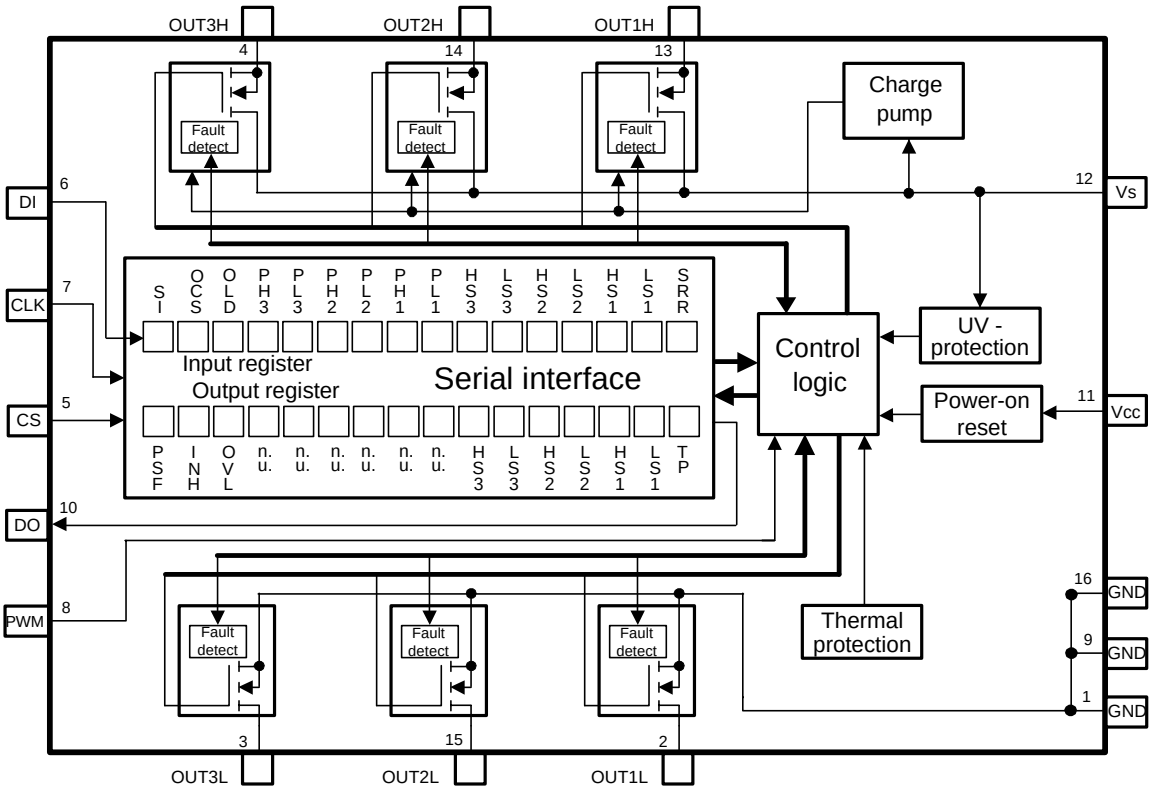
Ordering Information

Extended Type Number	Package	Remarks
T6819-TBS	SO16	Power package, tubed
T6819-TBQ	SO16	Power package, taped and reeled
T6829-TBS	SO16	Power package with heat slug, tubed
T6829-TBQ	SO16	Power package with heat slug, taped and reeled

Rev. A1, 12-Nov-01

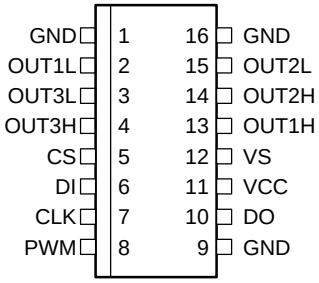
Block Diagram

Figure 1.



Pin Configuration

Figure 2.



Pin Description

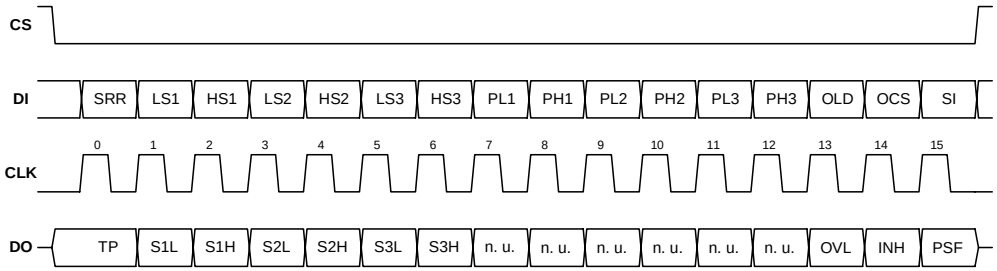
Pin	Symbol	Function
1	GND	T6819: Ground; reference potential; internal connection to Pin 9 and Pin 16; cooling tab T6829: Additional connection to heat slug
2	OUT1L	Low-side driver output 1; Power-MOS open drain with internal reverse diode; short-circuit protection; overtemperature protection; diagnosis for short and open load; PWM ability
3	OUT3L	Low-side driver output 3; see Pin 2
4	OUT3H	High-side driver output 3; Power-MOS open source with internal reverse diode; short-circuit protection; overtemperature protection; diagnosis for short and open load; PWM ability
5	CS	Chip select input; 5-V CMOS logic level input with internal pull up; low = serial communication is enabled, high = disabled
6	DI	Serial data input; 5-V CMOS logic level input with internal pull down; receives serial data from the control device; DI expects a 16-bit control word with LSB being transferred first
7	CLK	Serial clock input; 5-V CMOS logic level input with internal pull down; controls serial data input interface and internal shift register (f_{max} = 2 MHz)
8	PWM	PWM input; 5-V CMOS logic level input with internal pull down; receives PWM signal to control outputs which are selected for PWM mode by the serial data interface
9	GND	Ground; see Pin 1
10	DO	Serial data output; 5-V CMOS logic-level tristate output for output (status) register data; sends 16-bit status information to the µC (LSB is transferred first); output will remain tristated, unless device is selected by CS = low, therefore, several ICs can operate on one data-output line only.
11	VCC	Logic supply voltage (5 V)
12	VS	Power supply for high-side output stages OUT1H, OUT2H, OUT3H, internal supply
13	OUT1H	High-side driver output 3; see PIN 4
14	OUT2H	High-side driver output 2; see PIN 4
15	OUT2L	Low-side driver output 2; see Pin 2
16	GND	Ground; see Pin 1

Functional Description

Serial Interface

Data transfer starts with the falling edge of the CS signal. Data must appear at DI synchronized to CLK and are accepted on the falling edge of the CLK signal. LSB (bit 0, SRR) has to be transferred first. Execution of new input data is enabled on the rising edge of the CS signal. When CS is high, Pin DO is in tristate condition. This output is enabled on the falling edge of CS. Output data will change their state with the rising edge of CLK and stay stable until the next rising edge of CLK appears. LSB (bit 0, TP) is transferred first.

Figure 3. Data transfer



Input Data Protocol

Bit	Input Register	Function
0	SRR	Status register reset (high = reset; the bits PSF and OVL in the output data register are set to low)
1	LS1	Controls output LS1 (high = switch output LS1 on)
2	HS1	Controls output HS1 (high = switch output HS1 on)
3	LS2	See LS1
4	HS2	See HS1
5	LS3	See LS1
6	HS3	See HS1
7	PL1	Output LS1 additionally controlled by PWM Input
8	PH1	Output HS1 additionally controlled by PWM Input
9	PL2	See PL1
10	PH2	See PH1
11	PL3	See PL1
12	PH3	See PH1
13	OLD	Open load detection (low = on)
14	OCS	Overcurrent shutdown (high = overcurrent shutdown is active)
15	SI	Software inhibit; low = stand by, high = normal operation (data transfer is not affected by stand by function because the digital part is still powered)

Output Data Protocol

Bit	Output (Status) Register	Function
0	TP	Temperature prewarning: high = warning
1	Status LS1	Normal operation: high = output is on, low = output is off Open load detection: high = open load, low = no open load (correct load condition is detected if the corresponding output is switched off); not affected by SRR
2	Status HS1	Normal operation: high = output is on, low = output is off Open load detection: high = open load, low = no open load (correct load condition is detected if the corresponding output is switched off); not affected by SRR
3	Status LS2	Description see LS1
4	Status HS2	Description see HS1
5	Status LS3	Description see LS1
6	Status HS3	Description see HS1
7	n. u.	Not used
8	n. u.	Not used
9	n. u.	Not used
10	n. u.	Not used
11	n. u.	Not used
12	n. u.	Not used
13	OVL	Overload detected: set high, when at least one output is switched off by a short circuit condition or an overtemperature event. Bits 1 to 6 can be used to detect the affected switch. (open-load detection bit OLD = high)
14	INH	Inhibit: this bit is controlled by software (bit SI in input register) High = standby, low = normal operation
15	PSF	Power-supply fail: undervoltage at Pin VS detected

After power-on reset, the input register has the following status

Bit 15 SI	Bit 14 OCS	Bit 13 OLD	Bit 12 PH3	Bit 11 PL3	Bit 10 PH2	Bit 9 PL2	Bit 8 PH1	Bit 7 PL1	Bit 6 HS3	Bit 5 LS3	Bit 4 HS2	Bit 3 LS2	Bit 2 HS1	Bit 1 LS1	Bit 0 SRR
H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L

Power-Supply Fail

In case of undervoltage at Pin VS the power-supply fail bit (PSF) in the output register is set and all outputs are disabled. An undervoltage condition is only detected if it occurs over the undervoltage detection delay time t_{dUV}. After the undervoltage occurred the outputs are enabled immediately. The PSF bit keeps high until it is reset by the SRR bit in the input register.

Open-Load Detection

f the open-load detection bit (OLD) is set to low, a pull-up current for each high-side switch and a pull-down current for each low-side switch is turned on (open-load detec-

tion current I_{HS1-3}, I_{LS1-3}). If the current through a high-side or low-side switch in ON-state does not reach the open-load detection threshold, the corresponding bit of the output in the output register is set to high.

Switching on an output stage with OLD bit set to low disables the open-load function for this output.

Overtemperature Protection

If the junction temperature at one ore more switches exceeds the thermal prewarning threshold $T_{jPW\ set}$, the temperature prewarning bit (TP) in the output register is set. When temperature falls below the thermal prewarning threshold $T_{jPW\ reset}$, the Bit TP is reset. The TP bit can be read without transferring a complete 16-bit data word: with CS = high to low the state of TP appears at Pin DO. After the µC has read this information CS is set high and the data transfer is interrupted without affecting the state of input and output registers.

If the junction temperature at a switch exceeds the thermal shutdown threshold $T_{j\ switch\ off}$, the affected output is disabled and the corresponding bit in the output register is set to low. Additional the overload detection bit (OVL) in the output register is set. The output can be enabled again when the temperature falls below the thermal shutdown threshold $T_{jswitch\ on}$ and writing a high to the SRR bit in the input register. Thermal prewarning and shutdown threshold have hysteresis.

Short-Circuit Protection

The output currents are limited by a current regulator. If the overcurrent shutdown bit (OCS) in the input register is set, the affected output is switched off after a short delay time (t_{dSd}) when the current exceeds the overcurrent limitation and shutdown threshold. In this case the overload detection bit (OVL) is set and the corresponding status bit in the output register is set to low. For OCS = low the overcurrent shutdown is inactive and the OVL bit is not set by an overcurrent. By writing a high to the SRR bit in the input register the OVL bit is reset and the disabled outputs are enabled.

Inhibit

To inhibit the T6819 / T6829 the INH bit in the input register must be set to zero.

In this case all output stages are turned off but the serial interface stays active. The current consumption is reduced to less than 10 µA out of V_S and less than 20 µA out of V_{CC}. The output stages can be activated again by bit SI = 1.

Absolute Maximum Ratings

All values refer to GND pins

Parameter		Symbol	Value	Unit
Supply voltage	Pin 12	V_{VS}	-0.3 to 40	V
Supply voltage t<0.5s; IS>-2A	Pin 12	V_{VS}	-1	V
Logic supply voltage	Pin 11	V_{VCC}	-0.3 to 7	V
Logic input voltage	Pins 5to 8	V_{CS},V_{DI}, V_{CLK}, V_{PWM}	-0.3 to V_{VCC}+0.3	V
Logic output voltage	Pin 10	V_{DO}	-0.3 to V_{VCC}+0.3	V
Input current	Pins 5to 8	I_{CS},I_{DI}, I_{CLK}, I_{PWM}	-10 to +10	mA
Output current	Pin 10	I_{DO}	-10 to +10	mA
Output current	Pins 2 to 4 and 13 to 15	I_{Out3H}, $I_{Out2H,}$ I_{Out1H} I_{Out3L}, $I_{Out2L,}$ I_{Out1L}	Internal limited, see output specification	
Reverse conducting current (tpulse = 150 µs)	Pins 2 to 4 and 13 to 15 towards Pin 3	I_{Out3H}, $I_{Out2H,}$ I_{Out1H} I_{Out3L}, $I_{Out2L,}$ I_{Out1L}	17	A
Junction-temperature range		T_J	-40 to 150	°C
Storage-temperature range		T_{STG}	-55 to 150	°C

Thermal Resistance

Parameter	Test Conditions	Symbol	Value	Unit
T6819				
Junction – pin	Measured to GND Pins 1, 9, 16	R_{thJP}	30	K/W
Junction – ambient		R_{thJA}	65	K/W
T6829				
Junction – pin	Measured to heat slug, GND Pins 1, 9, 16	R_{thJP}	5	K/W
Junction – ambient		R_{thJA}	30	K/W

Operating Range

Parameter	Symbol	Value	Unit
Supply voltage	V_{VS}	V_{UV} [1)] to 40	V
Logic supply voltage	V_{VCC}	4.75 to 5.25	V
Logic input voltage	V_{CS},V_{DI}, V_{CLK}, V_{PWM}	-0.3 to V_{VCC}	V
Serial interface clock frequency	f_{CLK}	2	MHz
PWM input frequency	f_{PWM}	1	kHz
Junction-temperature range	T_j	-40 to 150	°C

Note: 1. Threshold for undervoltage detection

Noise and Surge Immunity

Parameter	Test Conditions	Value
Conducted interferences	ISO 7637–1	Level 4 [1)]
Interference suppression	VDE 0879 Part 3	Level 6
ESD (Human Body Model)	ESD S 5.1	2 kV
ESD (Machine Model)	JEDEC A115A	200 V

Electrical Characteristics

7.5 V < V_S < 40 V; 4.75 V < V_{CC} < 5.25 V; INH = High; -40°C < Tj < 150°C; unless otherwise specified, all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**Current Consumption**								
1.1	Quiescent current (VS)	V_{VS} < 16 V, SI = low	12	I_{VS}		1	5	µA	A
1.2	Quiescent current (VCC)	4.75 V < V_{VCC} < 5.25 V, SI = low	11	I_{VCC}		60	100	µA	A
1.3	Supply current (VS)	V_{VS} < 16 V normal operating, one output stage on, no load	12	I_{VS}		6	10	mA	A
1.4	Supply current (VCC)	4.75 V < V_{VCC} < 5.25 V, normal operating	11	I_{VCC}		350	600	µA	A
2	**Undervoltage Detection, Power-On Reset**								
2.1	Power-on reset threshold		11	V_{VCC}	3.4	3.9	4.4	V	A
2.2	Power-on reset delay time	After switching on V_{CC}		t_{dPor}	30	95	160	µs	A
2.3	Undervoltage-detection threshold	V_{CC} = 5 V	12	V_{Uv}	5.5		7.0	V	A
2.4	Undervoltage-detection hysteresis	V_{CC} = 5 V	12	ΔV_{Uv}		0.6		V	A
2.5	Undervoltage-detection delay time			t_{dUV}	10		40	µs	A
3	**Thermal Prewarning and Shutdown**								
3.1	Thermal prewarning			$T_{jPW\ set}$	120	145	170	°C	B
3.2	Thermal prewarning			$T_{jPW\ reset}$	105	130	155	°C	B
3.3	Thermal prewarning hysteresis			ΔT_{jPW}		15		K	B
3.4	Thermal shutdown			$T_{j\ switch\ off}$	150	175	200	°C	B
3.5	Thermal shutdown			$T_{j\ switch\ on}$	135	160	185	°C	B
3.6	Thermal shutdown hysteresis			$\Delta T_{j\ switch\ off}$		15		K	B
*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter									

Electrical Characteristics

7.5 V < V_S < 40 V; 4.75 V < V_{CC} < 5.25 V; INH = High; -40°C < Tj < 150°C; unless otherwise specified, all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
3.7	Ratio thermal shutdown / thermal prewarning			$T_{j\ switch\ off}$ / $T_{jPW\ set}$	1.05	1.2			B
3.8	Ratio thermal shutdown / thermal prewarning			$T_{j\ switch\ on}$ / $T_{jPW\ reset}$	1.05	1.2			B
4	**Output Specification (OUT1-OUT3)**								
4.1	On resistance	I_{Out} = 1.5 A	2, 3, 15	$R_{DS\ On\ L}$			1	W	A
4.2	On resistance	I_{Out} = -1.5 A	4, 13, 14	$R_{DS\ On\ H}$			1	W	A
4.3	Source output leakage current	V_{Out1-3} = 0 V, output stages off	4, 13, 14	I_{Out1-3}	-5			µA	A
4.4	Sink output leakage current	V_{Out1-3} = V_{VS}, output stages off	2, 3, 15	I_{Out1-3}			5	µA	A
4.5	High-side switch reverse diode forward voltage	I_{Out} = 1.5 A	4, 13, 14	V_{Out1-3}–V_{VS}			1.3	V	A
4.6	Low-side switch reverse diode forward voltage	I_{Out} = -1.5 A	2, 3, 15	V_{Out1-3}			1.3	V	A
4.7	Source overcurrent limitation and shutdown threshold		4, 13, 14	I_{Out1-3}	-2.5	-2	-1.5	A	A
4.8	Sink overcurrent limitation and shutdown threshold		2, 3, 15	I_{Out1-3}	1.5	2	2.5	A	A
4.9	Overcurrent shutdown delay time			t_{dSd}	10		40	µs	A
4.10	Source open load detection current	Input register bit 13 (OLD) = low, output off	4, 13, 14	I_{Out1-3}	-4	-2		mA	A
4.11	Sink open load detection current	Input register bit 13 (OLD) = low, output off	2, 3, 15	I_{Out1-3}		2	4	mA	A
4.12	Source output switch on delay [1)]	V_{VS} = 13 V, RLoad=30Ω		t_{don}		5	15	µs	A
4.13	Sink output switch on delay [1)]	V_{VS} = 13 V, R_{Load} =30 Ω		t_{don}		15	25	µs	A
4.14	Source output switch off delay [1)]	V_{VS} =13V, R_{Load} = 30 Ω		t_{doff}		5	15	µs	A
4.15	Sink output switch off delay [1)]	V_{VS} =13V, R_{Load} = 30 Ω		t_{doff}		1	2	µs	A
*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter									

Electrical Characteristics

7.5 V < V_S < 40 V; 4.75 V < V_{CC} < 5.25 V; INH = High; -40°C < Tj < 150°C; unless otherwise specified, all values refer to GND pins.

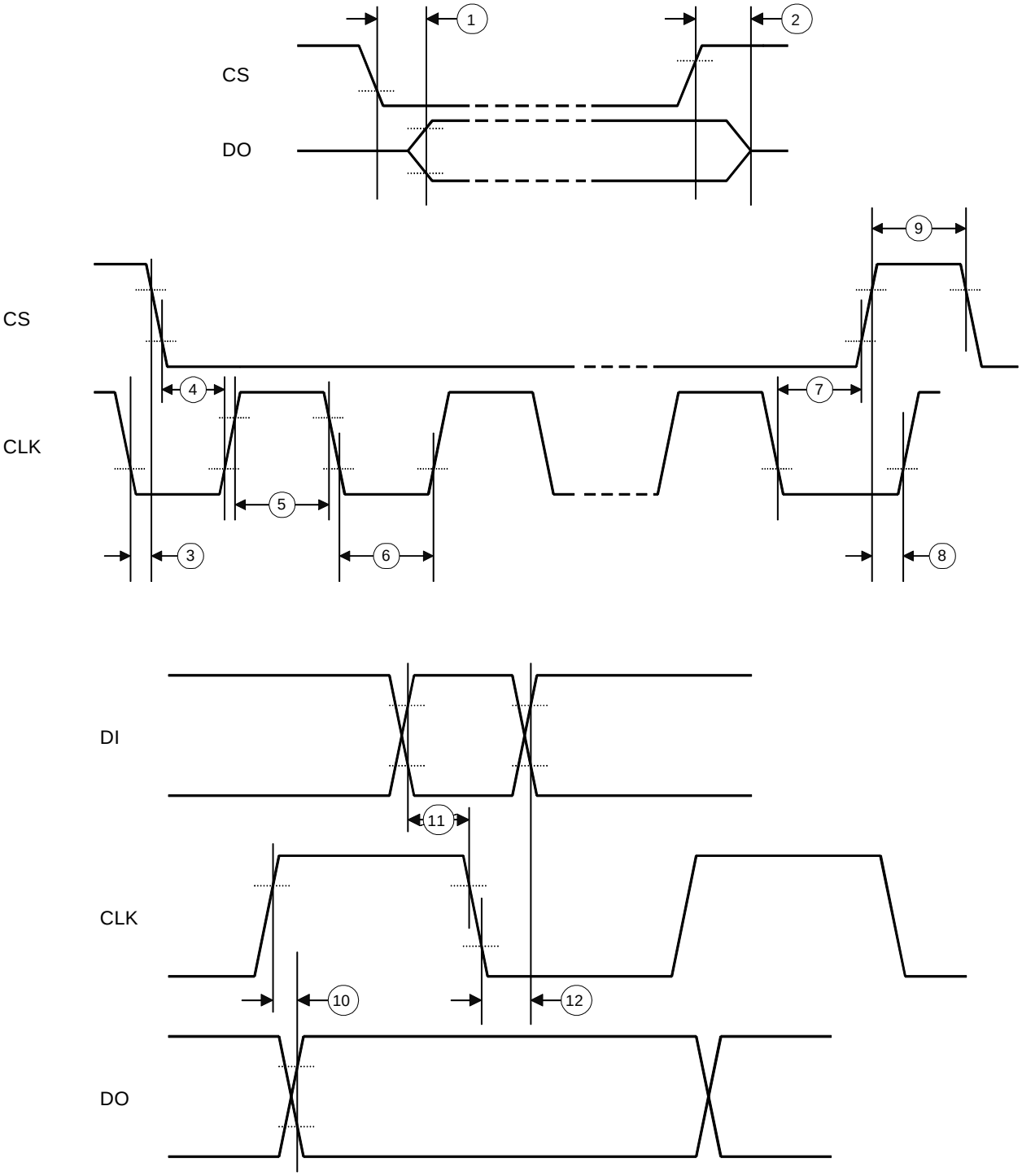
No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
4.16	Dead time between corresponding high- and low-side switches	V_{VS}=13V, R_{Load} = 30 Ω		t_{don} -t_{doff}	1			µs	A
5	**Logic Inputs DI, CLK, CS, PWM**								
5.1	Input voltage low - evel threshold		5-8	V_{IL}	0.3 × V_{VCC}			V	A
5.2	Input voltage high-level threshold		5-8	V_{IH}			0.7 × V_{VCC}	V	A
5.3	Hysteresis of input voltage		5-7	ΔV_I	50		500	mV	A
5.4	Pull-down current Pins DI, CLK, PWM	V_{DI}, $V_{CLK,}$ V_{PWM} = V_{CC}	6, 7,8	I_{PD}	10		60	µA	A
5.5	Pull-up current Pin CS	V_{CS} = 0 V	5	I_{PU}	-50		-10	µA	A
5.6	Hysteresis of input voltage		8	ΔV_I	50		700	mV	A
6	**Serial Interface – Logic Output DO**								
6.1	Output-voltage low level	I_{OL} = 2mA	Pin 10	V_{DOL}			0.4	V	A
6.2	Output-voltage high level	I_{OL} = -2mA	Pin 10	V_{DOH}	V_{VCC}- 0.7V			V	A
6.3	Leakage current (tristate)	V_{CS}= V_{CC} 0V < V_{DO} < V_{VCC}	Pin 10	I_{DO}	-10		10	µA	A
7	**Inhibit Input – Timing**								
7.1	Stand-by setup time			$t_{INHSethl}$			100	µs	A
8.2	Stand-by setup time			$t_{INHSetlh}$			100	µs	A
*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter									

Note: 1. Delay time between rising edge of CS after data transmission and switch on output stages to 90% of final level. Device not in stand-by for t >1ms

Serial Interface – Timing

Parameters	Test Conditions	Timing Chart No.	Symbol	Min.	Typ.	Max.	Unit
DO enable after CS falling edge	C_{DO} = 100 pF	1	t_{ENDO}			200	ns
DO disable after CS rising edge	C_{DO} = 100 pF	2	t_{DISDO}			200	ns
DO fall time	C_{DO} = 100 pF	-	t_{DOf}			100	ns
DO rise time	C_{DO} = 100 pF	-	t_{DOr}			100	ns
DO valid time	C_{DO} = 100 pF	10	t_{DOVal}			200	ns
CS setup time		4	$t_{CSSethl}$	225			ns
CS setup time		8	$t_{CSSetlh}$	225			ns
CS high time		9	t_{CSh}	500			ns
CLK high time		5	t_{CLKh}	225			ns
CLK low time		6	t_{CLKl}	225			ns
CLK period time		-	t_{CLKp}	500			ns
CLK setup time		7	$t_{CLKSethl}$	225			ns
CLK setup time		3	$t_{CLKSetlh}$	225			ns
DI setup time		11	t_{DIset}	40			ns
DI hold time		12	t_{DIHold}	40			ns

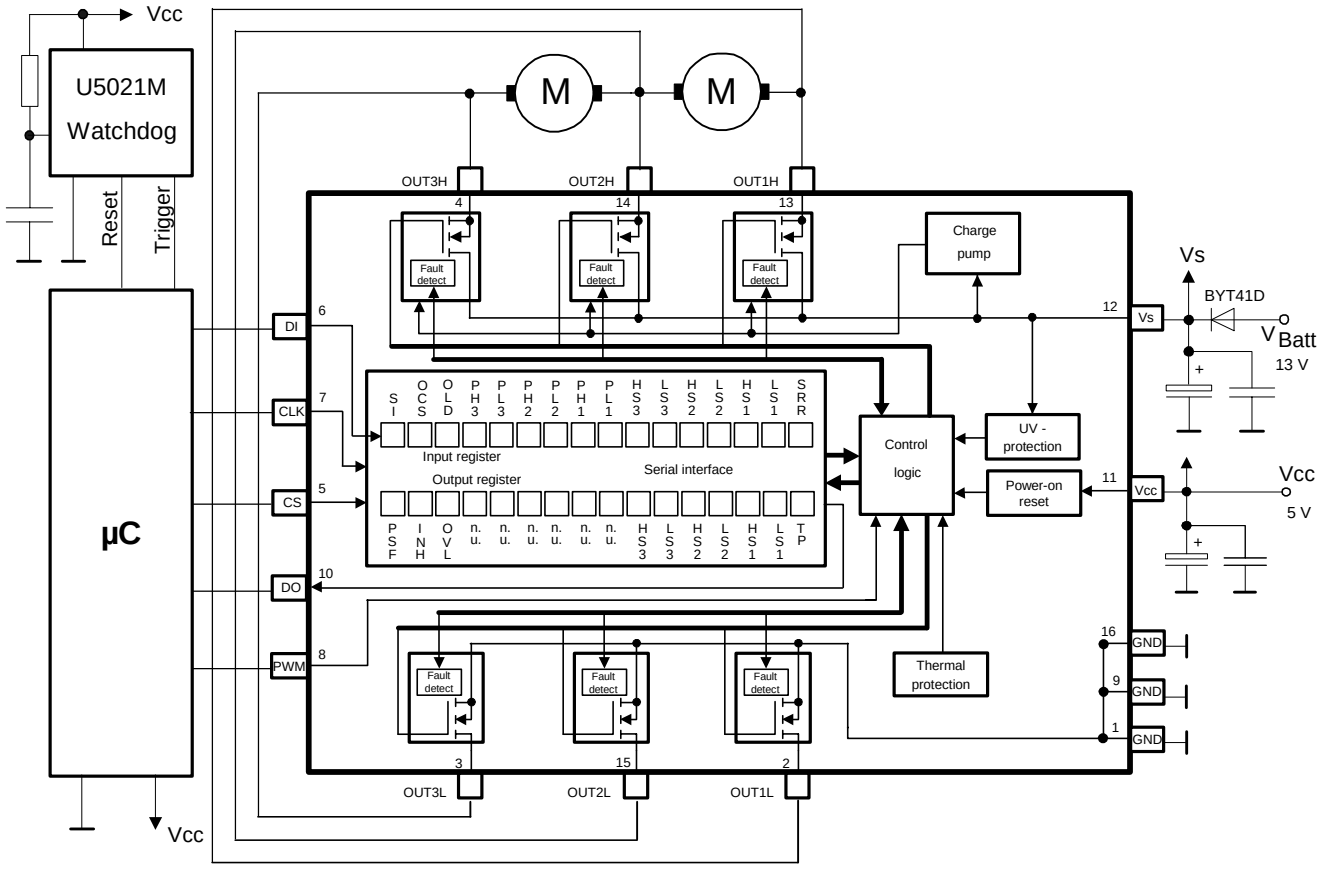
Figure 4. Serial interface timing with chart number



Inputs DI, CLK, CS: High level = 0.7 x $V_{CC,}$ low level = 0.3 x V_{CC}
Output DO: High level = 0.8 x V_{CC}, low level = 0.2 x V_{CC}

Application Circuit

Figure 5.



Application Notes

It is strongly recommended to connect the blocking capacitors at V_{CC} and V_S as close as possible to the power supply and GND pins.

Recommended value for capacitors at V_S:

Electrolytic capacitor C > 22 µF in parallel with a ceramic capacitor C = 100 nF. Value for electrolytic capacitor depends on external loads, conducted interferences and reverse conducting current I_{Outzx} (see Absolute Maximum Ratings).

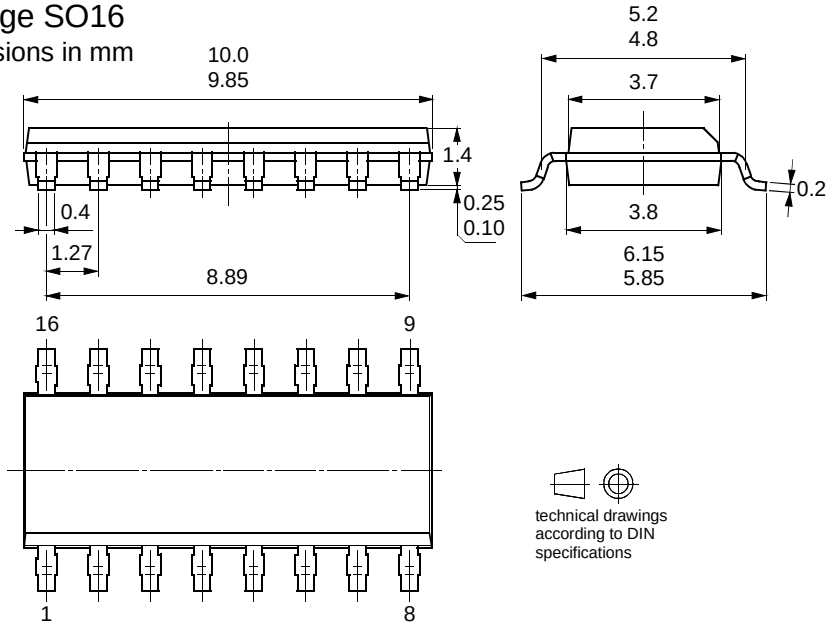
Recommended value for capacitors at V_{CC}:

Electrolytic capacitor C > 10 µF in parallel with a ceramic capacitor C = 100 nF.

To reduce thermal resistance it is recommended to place cooling areas on the PCB as close as possible to GND pins.

Package Information

Package SO16
Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **Atmel Germany GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Atmel Germany GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Atmel Germany GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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