ULTRA-PRECISION DIFFERENTIAL CML LINE DRIVER/RECEIVER WITH INTERNAL TERMINATION

Precision Edge™
SY58600U

FEATURES

- **Guaranteed AC performance over temperature and voltage:**
  - **DC-to >10.7Gbps data rate throughput**
  - **DC-to >7GHz clock f_{MAX}**
  - **<220ps in-to-out t_{pd}**
  - **t_r / t_f <60ps**
- **Ultra low-jitter design:**
  - **<1ps$_{rms}$ random jitter**
  - **<10ps$_{pp}$ deterministic jitter**
  - **<10ps$_{pp}$ total jitter (clock)**
- **Minimum input swing 200mV (|IN–/IN|)**
- **Unique, patent-pending input termination and VT pin accepts DC-coupled and AC-coupled inputs (CML, PECL, LVDS)**
- **Internal 50Ω output source termination**
- **Typical 400mV CML output swing**
- **Power supply 2.5V ±5% or 3.3V ±10%**
- **–40°C to 85°C industrial temperature range**
- **Available in an ultra-small (2mm × 2mm) 8-pin MLF™ package**

APPLICATIONS

- **Backplane buffering**
- **OC-12 to OC-192 SONET/SDN clock/data distribution**
- **All Gigabit Ethernet distribution**
- **Fibre Channel distribution**

Precision Edge™

DESCRIPTION

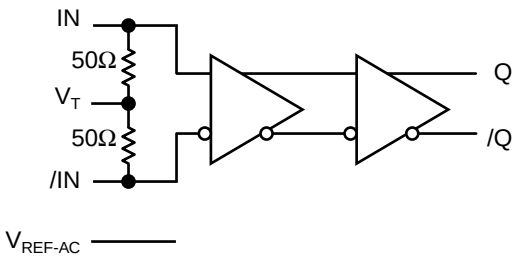
The SY58600U is a 2.5V/3.3V precision, high-speed, differential receiver capable of handling clocks up to 7GHz and data streams up to 10.7Gbps.

The differential input includes Micrel's unique, 3-pin input termination architecture that allows users to interface to any differential signal (AC or DC-coupled) as small as 200mV$_{pp}$ without any level shifting or termination resistor networks in the signal path. The outputs are 400mV CML, with extremely fast rise/fall times guaranteed to be less than 60ps.

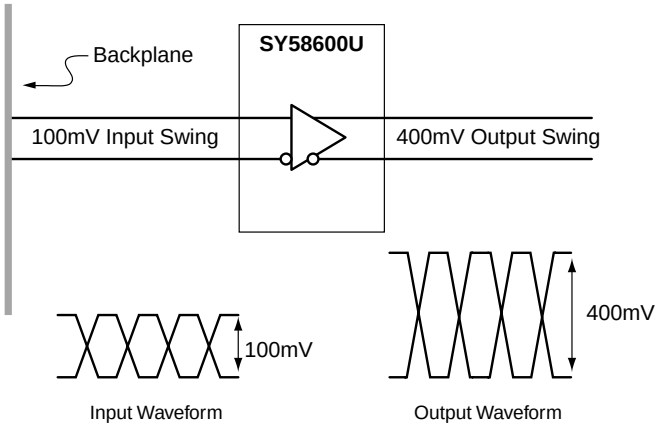
The SY58600U operates from a 2.5V ±5% supply or a 3.3V ±10% supply and is guaranteed over the full industrial temperature range of –40°C to +85°C. For applications that require 800mV LVPECL outputs, consider the SY58601U or for 400mV LVPECL outputs the SY58602U. The SY58600U is part of Micrel's high-speed, Precision Edge™ product line.

All support documentation can be found on Micrel's web site at www.micrel.com.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATION



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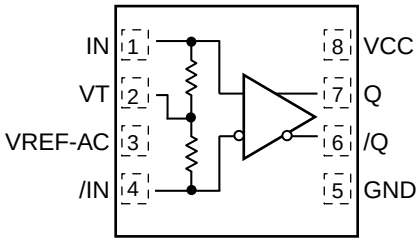
*Micro*LeadFrame and MLF are trademarks of Amkor Technology, Inc.

PACKAGE/ORDERING INFORMATION



8-Pin MLF™ (MLF-8)

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking
SY58600UMITR[2]	MLF-8	Industrial	600

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.
2. Tape and Reel.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
1, 4	IN, /IN	Differential Input: This input pair is the signal to be buffered. These inputs accept AC or DC-coupled signals as small as 100mV. Each pin of this pair internally terminates to a VT pin through 50Ω. Note that this input will default to an indeterminate state if left open. Please refer to the “Input Interface Applications” section for more details.
2	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to this pin. The VT pin provides a center-tap to a termination network for maximum interface flexibility. See “Input Interface Applications” section for more details.
3	VREF-AC	Reference Output Voltage: This output biases to V_{CC} –1.2V. Connect to VT pin when AC-coupling the input. Bypass with 0.01µF low ESR capacitor to V_{CC}. Maximum current source or sink is 0.5mA. See “Input Interface Applications” section.
8	VCC	Positive Power Supply. Bypass with 0.1µF||0.01µF low ESR capacitors as close to the VCC pin as possible.
7, 6	Q, /Q	Differential CML Output: Differential buffered output copy of the input signal. The differential output swing is typically 800mV into a 50Ω load, or 100Ω across the pair. See “Output Interface Applications” section.
5	GND, Exposed	Ground. Ground pin and exposed pad must be connected to the same ground plane.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
CML Output Voltage (V_{OUT}) ..... V_{CC} –1.0V to V_{CC} +0.5V
Termination Current[3]
  Source or Sink Current on V_T ..... ±100mA
Input Current
  Source or Sink Current on IN, /IN ..... ±50mA
Current (V_{REF})
  Source or Sink Current on V_{REF}–AC ..... ±1.5mA
Lead Temperature (soldering, 10 sec.) ..... +265°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +2.375V to +2.625V or
..... +3.0V to +3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[4]
  MLF™ (θ_{JA})
    Still-Air ..... 93°C/W
  MLF™ (ψ_{JB})
    Junction-to-Board ..... 32°C/W

DC ELECTRICAL CHARACTERISTICS[5]

T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply	V_{CC} = 2.5V V_{CC} = 3.3V	2.375 3.0	2.5 3.3	2.625 3.6	V V
I_{CC}	Power Supply Current	No Load, max. V_{CC}, **Note 6**		45	65	mA
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		80	100	120	Ω
R_{IN}	Input Resistance (IN-to-V_T, /IN-to-V_T)		40	50	60	Ω
V_{IH}	Input HIGH Voltage (IN, /IN)	**Note 7**	V_{CC} –1.6		V_{CC}	V
V_{IL}	Input LOW Voltage (IN, /IN)		0		V_{IH} –0.1	V
V_{IN}	Input Voltage Swing (IN, /IN)	See Figure 1a.	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing |IN–, /IN|	See Figure 1b.	0.2		3.4	V
V_{T_IN}	In-to-V_T (IN, /IN)				1.28	V
$V_{REF–AC}$	Output Reference Voltage		V_{CC} –1.3	V_{CC} –1.2	V_{CC} –1.1	V

Notes:

1. Permanent device damage may occur if the ratings in “Absolute Maximum Ratings” section are exceeded. This is a stress rating only and functional operation is not implied for conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability use for input of the same package only.
4. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device’s most negative potential on the PCB. ψ_{JB} uses 4-layer θ_{JA} in still-air, unless otherwise stated.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. Includes current through internal 50Ω pull-ups.
7. V_{IH} (min) not lower than 1.2V.

CML OUTPUTS DC ELECTRICAL CHARACTERISTICS[8]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = –40°C to +85°C; R_L = 100Ω across output pair or equivalent, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage Q, /Q		V_{CC}–0.020	V_{CC}–0.010	V_{CC}	V
V_{OUT}	Output Voltage Swing Q, /Q	See Figure 1a.	325	400		mV
V_{DIFF_OUT}	Differential Output Voltage Swing Q, /Q	See Figure 1b.	650	800		mV
R_{OUT}	Output Source Impedance Q, /Q		40	50	60	Ω

AC ELECTRICAL CHARACTERISTICS[9]

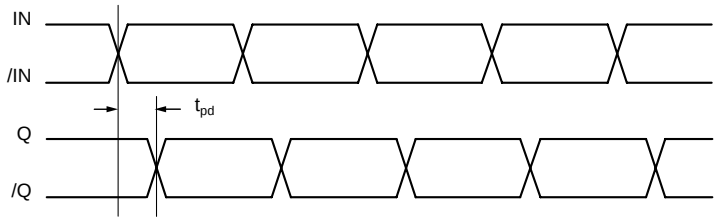
V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = –40°C to +85°C; R_L = 100Ω across output pair or equivalent, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	NRZ Data	10.7			Gbps
		$V_{OUT} \geq$ 200mV Clock	7			GHz
t_{pd}	Propagation Delay	IN-to-Q	70	125	220	ps
t_{pd} Tempco	Differential Propagation Delay Temperature Coefficient			115		fs/°C
t_{JITTER}	Data Random Jitter (RJ)	**Note 10**			1	ps_{rms}
	Deterministic Jitter (DJ)	**Note 11**			10	ps_{pp}
	Clock Cycle-to-Cycle Jitter	**Note 12**			1	ps_{rms}
	Total Jitter (TJ)	**Note 13**			10	ps_{pp}
t_r, t_f	Output Rise/Fall Times Q, /Q	(20% to 80%) At full output swing.	20	40	60	ps

Notes:

8. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
9. High frequency AC electricals are guaranteed by design and characterization.
10. Random jitter is measured with a K28.7 comma detect character pattern, measured at 2.5Gbps/3.2Gbps.
11. Deterministic jitter is measured at 2.5Gbps/3.2Gbps with both K28.5 and 2^{23}–1 PRBS pattern.
12. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, T_n–T_{n-1} where T is the time between rising edges of the output signal.
13. Total jitter definition: with an ideal clock input of frequency ≤ f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

TIMING DIAGRAM



DEFINITION OF SINGLE-ENDED AND DIFFERENTIAL SWINGS

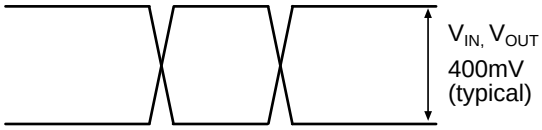


Figure 1a. Single-Ended Swing

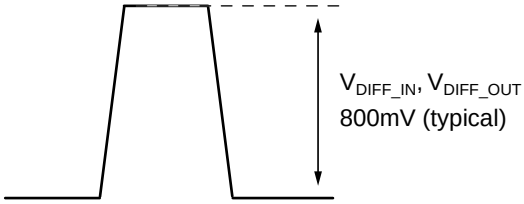


Figure 1b. Differential Swing

INPUT AND OUTPUT STAGE INTERNAL TERMINATION

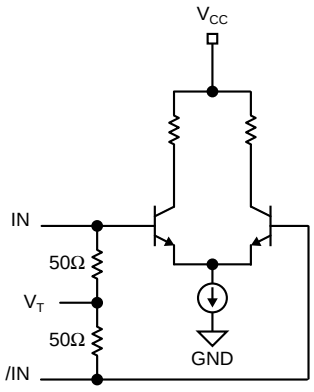


Figure 2a. Simplified Differential Input Stage

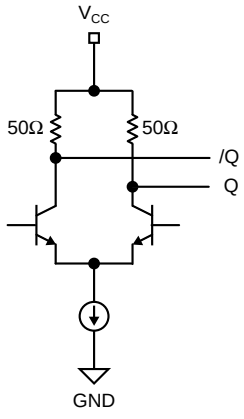
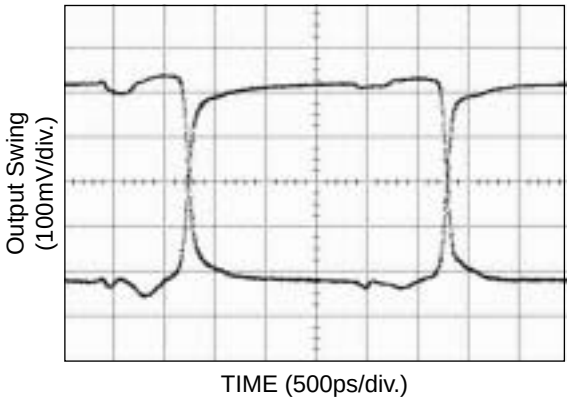


Figure 2b. Simplified Differential Output Stage

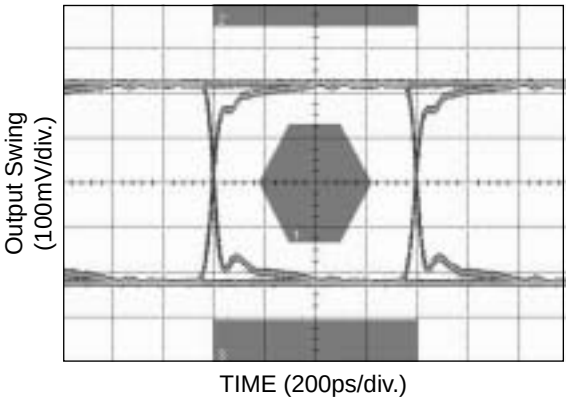
TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 3.3V, GND = 0, V_{IN} = 800mV.

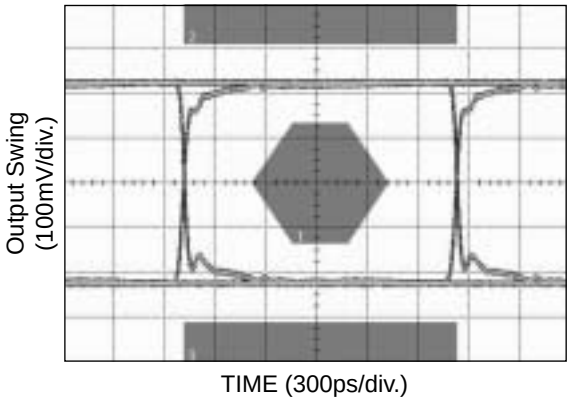
200MHz Clock



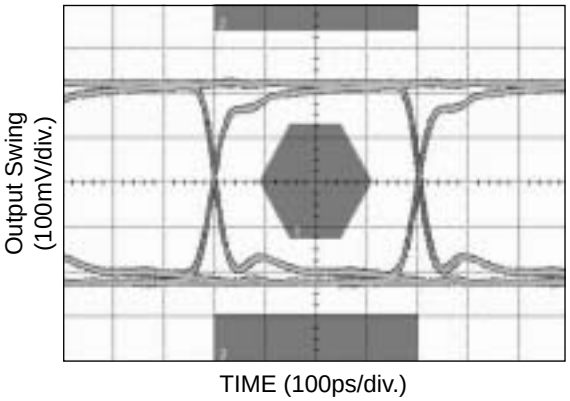
1xGBE Mask 2^{23}–1



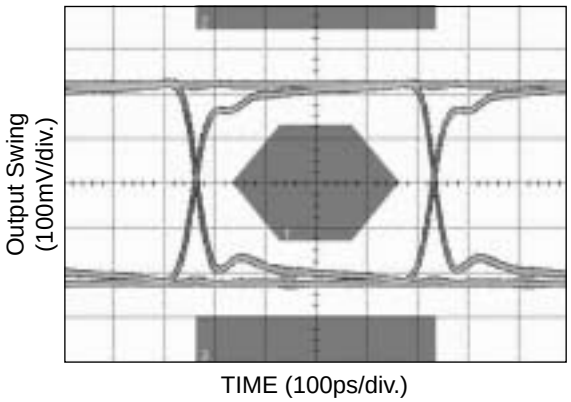
OC-12 Mask 2^{23}–1 PRBS



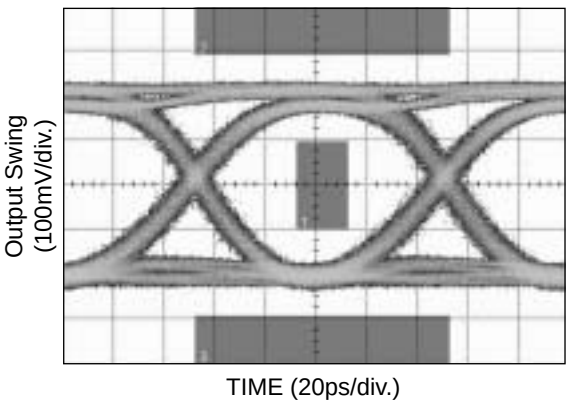
2xGBE Mask 2^{23}–1 PRBS



2xFC Mask 2^{23}–1 PRBS



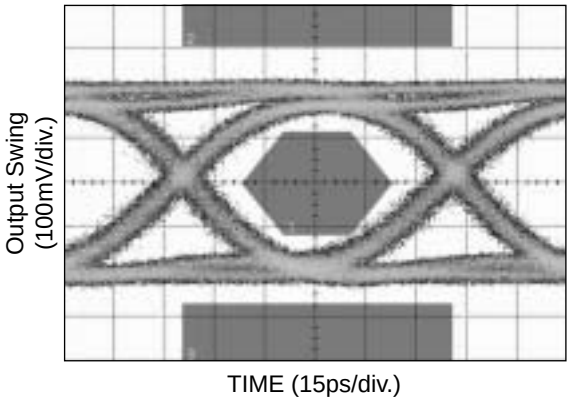
OC-192 Mask 2^{23}–1 PRBS



TYPICAL OPERATING CHARACTERISTICS CONT'D

V_{CC} = 3.3V, GND = 0, V_{IN} = 800mV.

10xGBE Mask 2^{23}–1 PRBS



INPUT INTERFACE APPLICATIONS

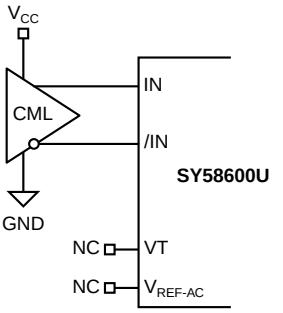


Figure 3a. CML Interface (DC-Coupled)

Option: V_T may be connected to V_{CC}

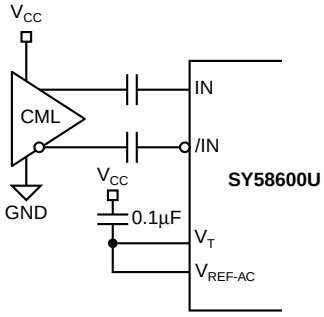


Figure 3b. CML Interface (AC-Coupled)

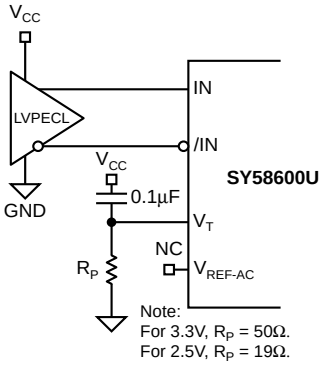


Figure 3c. LVPECL Interface (DC-Coupled)

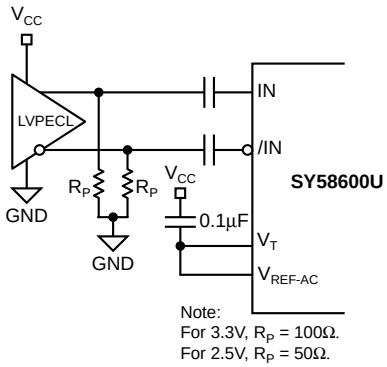


Figure 3d. LVPECL Interface (AC-Coupled)

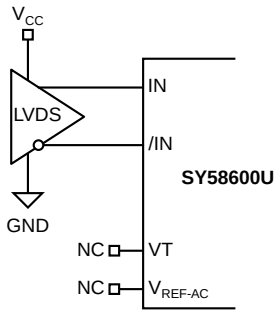


Figure 3e. LVDS Interface

OUTPUT INTERFACE APPLICATIONS

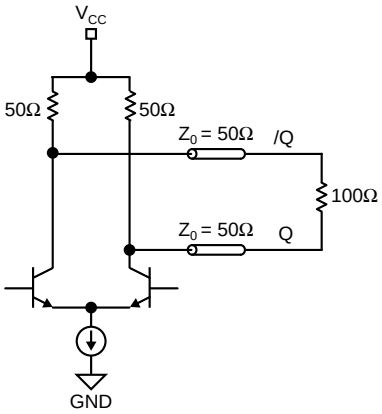


Figure 4a. CML DC-Coupled Termination

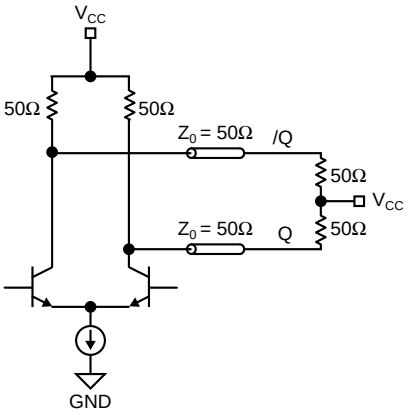


Figure 4b. CML DC-Coupled Termination

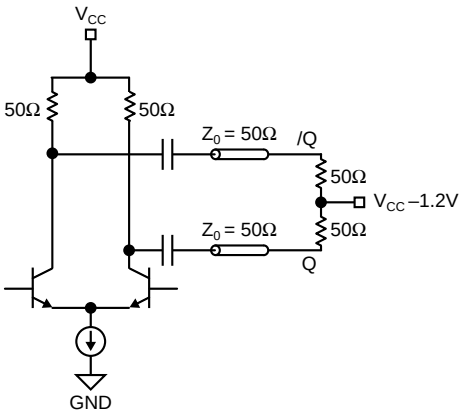
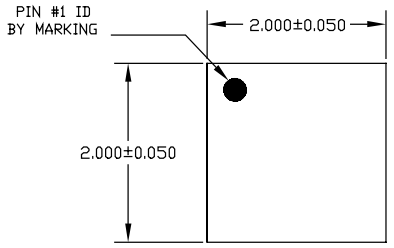


Figure 4c. CML AC-Coupled Termination

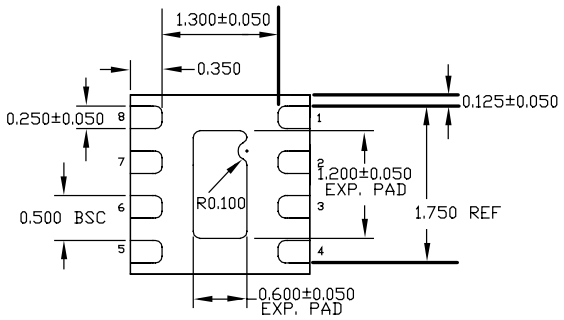
RELATED PRODUCT AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
SY58601U	2.5V/3.3V 5Gbps Differential 800mV LVPECL Line Driver/Receiver with Internal Termination	www.micrel.com/product-info/products/sy58601u.shtml
SY58602U	2.5V/3.3V 10.7Gbps Differential 400mV LVPECL Line Driver/Receiver with Internal Termination	www.micrel.com/product-info/products/sy58602u.shtml
	MLF™ Application Note	www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

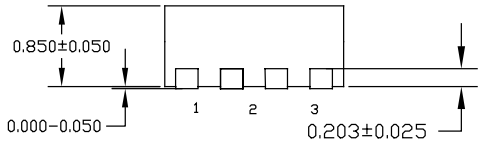
8 LEAD ULTRA-SMALL EPAD *Micro*LeadFrame™ (MLF-8)



TOP VIEW

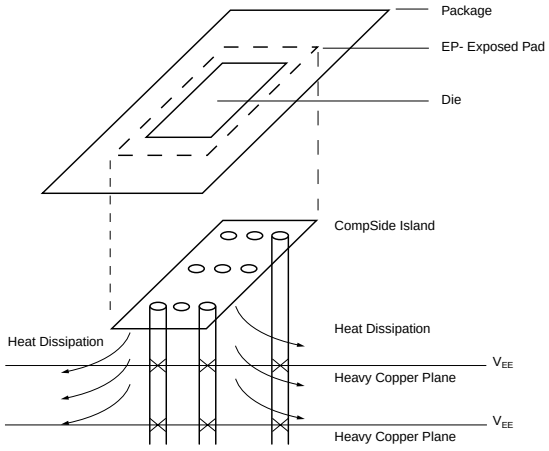


BOTTOM VIEW



SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



PCB Thermal Consideration for 8-Pin MLF™ Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

1. Package meets Level 2 qualification.
2. All parts dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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