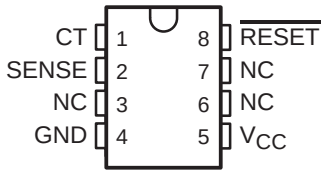
SLVS220B – JULY 1999 – REVISED AUGUST 2000

- **Adjustable Sense Voltage With Two External Resistors**
- **Adjustable Hysteresis of Sense Voltage**
- **Wide Operating Supply-Voltage Range . . . 1.8 V to 40 V**
- **Wide Operating-Temperature Range . . . –40°C to 85°C**
- **Low Power Consumption (I_{CC} = 0.6 mA TYP, V_{CC} = 40 V)**
- **Minimum External Components**
- **Package Options Include Plastic Small-Outline (PS) and Thin Shrink Small-Outline (PW) Packages and Standard DIP (P)**

P, PS, OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TL7700 is a bipolar integrated circuit designed for use as a reset controller in microcomputer and microprocessor systems. The SENSE voltage can be set to any value greater than 0.5 V using two external resistors. The hysteresis value of the sense voltage also can be set by the same resistors. The device includes a precision voltage reference, fast comparator, timing generator, and output driver, so it can generate a power-on reset signal in a digital system.

The TL7700 has an internal 1.5-V temperature-compensated voltage reference from which all function blocks are supplied. Circuit function is very stable, with supply voltage in the 1.8-V to 40-V range. Minimum supply current allows use with ac line operation, portable battery operation, and automotive applications.

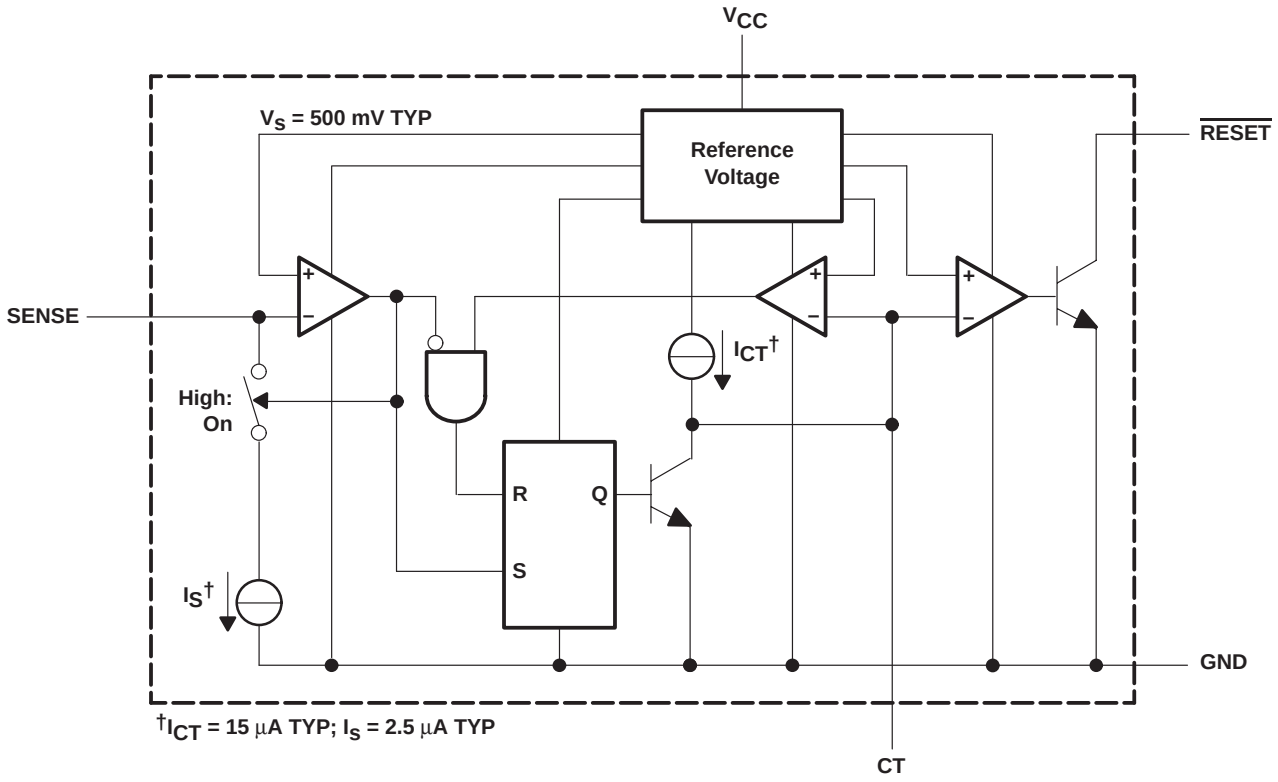
The TL7700C is characterized for operation from –40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		
	PLASTIC DIP (P)	PLASTIC SMALL OUTLINE (PS)	PLASTIC THIN SHRINK SMALL OUTLINE (PW)
–40°C to 85°C	TL7700CP	TL7700CPS	TL7700CPW

PS and PW packages are available taped and reeled. Add the suffix R to device type (e.g., TL7700CPSR).

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
CT	1	Timing capacitor connection. This terminal sets the $\overline{\text{RESET}}$ output pulse duration (t_{po}). It is connected internally to a 15-μA constant-current source. There is a limit on the switching speed of internal elements; even if CT is set to 0, response speeds remain at approximately 5 to 10 μs. If CT is open, the device can be used as an adjustable-threshold noninverting comparator. If CT is low, the internal output-stage comparator is active and the $\overline{\text{RESET}}$ output transistor is on. An external voltage must not be applied to this terminal due to the internal structure of the device. Therefore, drive the device using an open-collector transistor, FET, or 3-state buffer (in the low-level or high-impedance state).
GND	4	Ground. Keep this terminal as low impedance to reduce circuit noise.
NC	3, 6, 7	No internal connection
$\overline{\text{RESET}}$	8	Reset output. This terminal can be connected directly to a system that resets in the active-low state. A pullup resistor usually is required because the output is an npn open-collector transistor. An additional transistor should be connected when the active-high reset or higher output current is required.
SENSE	2	Voltage sense. This terminal has a threshold level of 500 mV. The sense voltage and hysteresis can be set at the same time when the two voltage-dividing resistors are connected. The reference voltage is temperature compensated to inhibit temperature drift in the threshold voltage within the operating temperature range.
V_{CC}	5	Power supply. This terminal is used in an operating-voltage range of 1.8 V to 40 V.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 41 V
Sense input voltage range, V_S . . . . . –0.3 V to 41 V
Output voltage, V_{OH} (off state) . . . . . 41 V
Output current, I_{OL} (on state) . . . . . 5 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3): P package . . . . . 85°C/W
PS package . . . . . 95°C/W
PW package . . . . . 149°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	1.8		40	V
Low-level output current, I_{OL}			3	mA
Operating free-air temperature, T_A	–40		85	°C

electrical characteristics, V_{CC} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_S	SENSE input voltage			495	500	505	mV
		T_A = –40°C to 85°C		490		510	
I_S	SENSE input current	V_S = 0.4 V		2	2.5	3	µA
			T_A = –40°C to 85°C	1.5		3.5	
I_{CC}	Supply current	V_{CC} = 40 V, V_S = 0.6 V, No load			0.6	1	mA
V_{OL}	Low-level output voltage	I_{OL} = 1.5 mA				0.4	V
		I_{OL} = 3 mA				0.8	
I_{OH}	High-level output current	V_{OH} = 40 V, V_S = 0.6 V, T_A = –40°C to 85°C				1	µA
I_{CT}	Timing-capacitor charge current	V_S = 0.6 V		11	15	19	µA

switching characteristics, V_{CC} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pi}	SENSE pulse duration	C_T = 0.01 µF	2			µs
t_{po}	Output pulse duration	C_T = 0.01 µF	0.5	1	1.5	ms
t_r	Output rise time	C_T = 0.01 µF, R_L = 2.2 kΩ, C_L = 100 pF			15	µs
t_f	Output fall time	C_T = 0.01 µF, R_L = 2.2 kΩ, C_L = 100 pF			0.5	µs
t_{pd}	Propagation delay time, SENSE to output	C_T = 0.01 µF			10	µs

PARAMETER MEASUREMENT INFORMATION

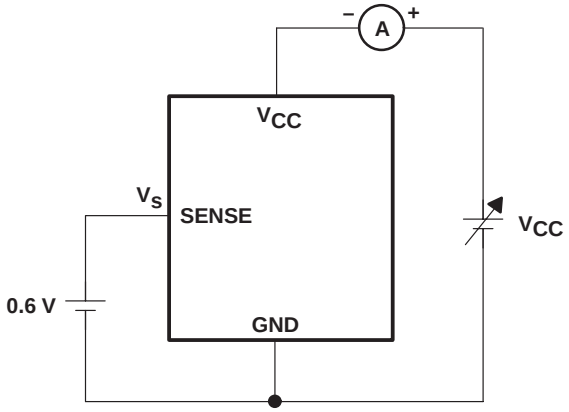


Figure 1. V_{CC} vs I_{CC} Measurement Circuit

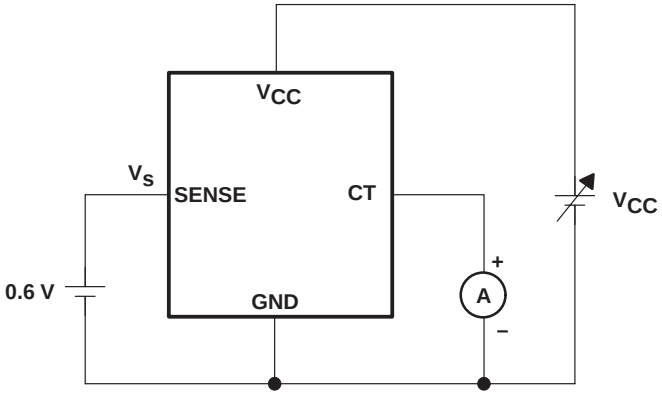


Figure 2. V_{CC} vs I_{CT}

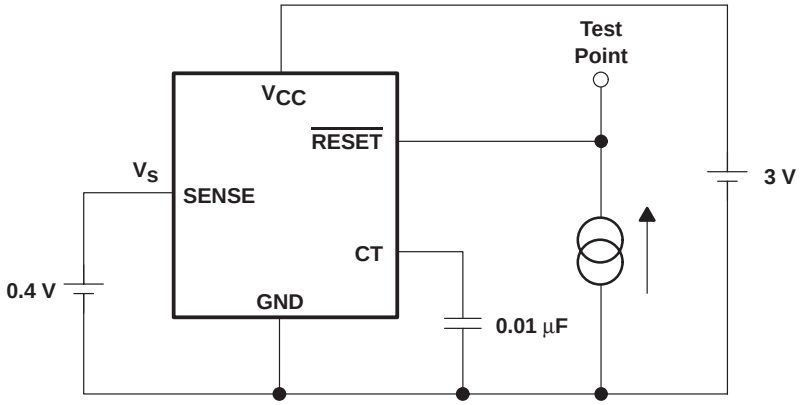


Figure 3. I_{OL} vs V_{OL}

PARAMETER MEASUREMENT INFORMATION

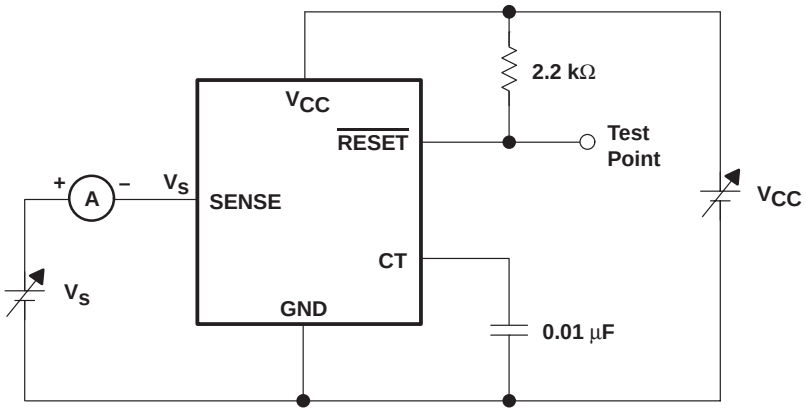


Figure 4. V_S, I_S Characteristics

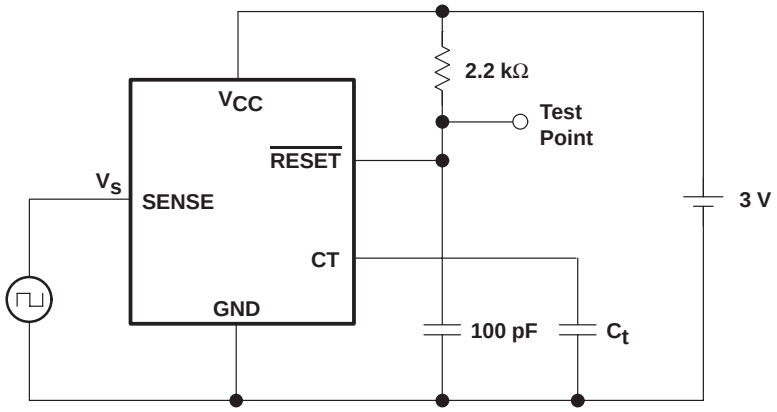


Figure 5. Switching Characteristics

TYPICAL CHARACTERISTICS†

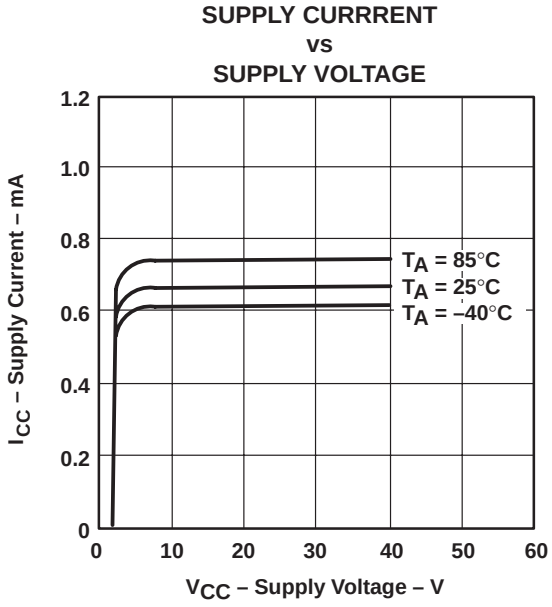


Figure 6

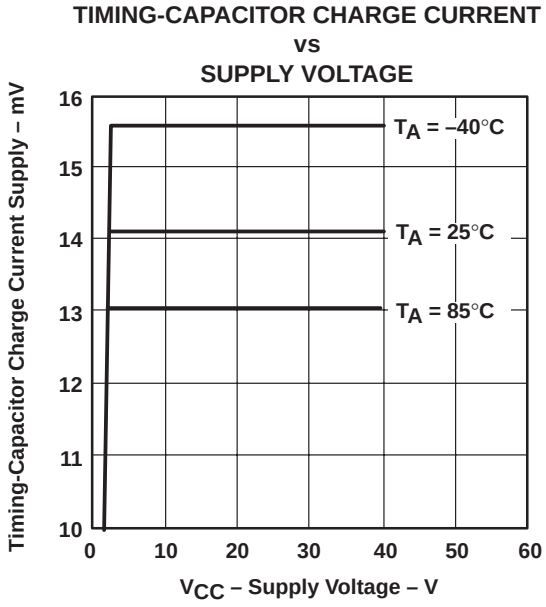


Figure 7

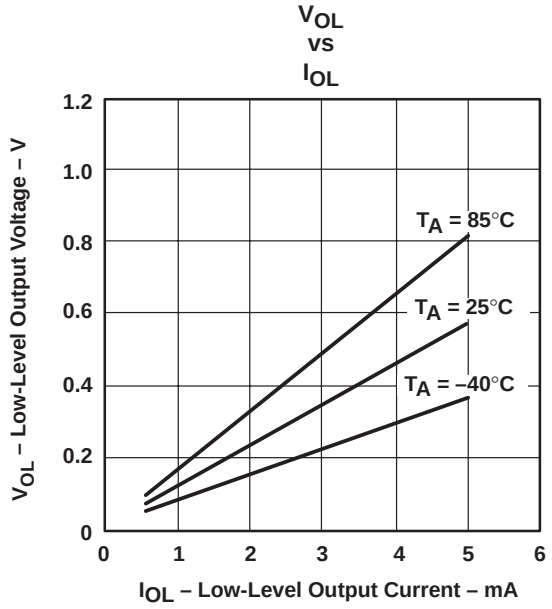


Figure 8

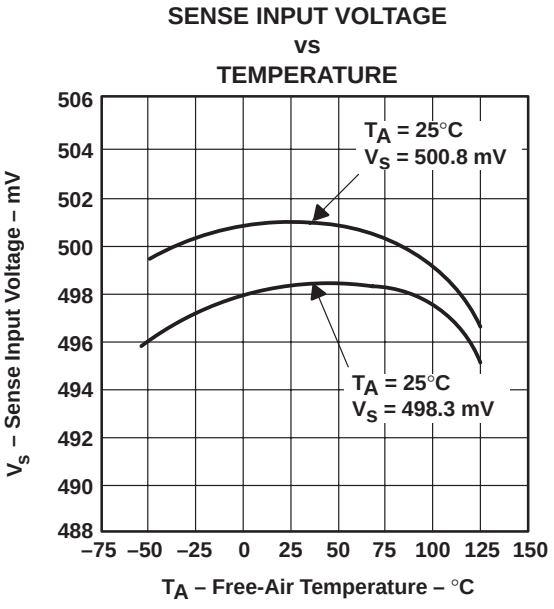


Figure 9

† Data at high and low temperatures are applicable only within the recommended operating conditions.

TYPICAL CHARACTERISTICS†

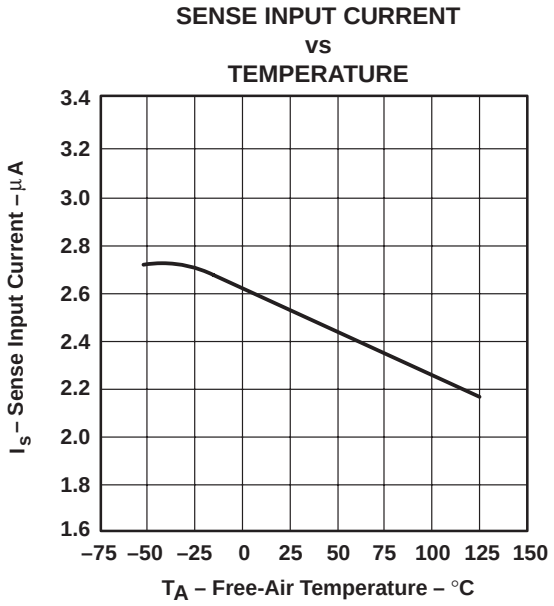


Figure 10

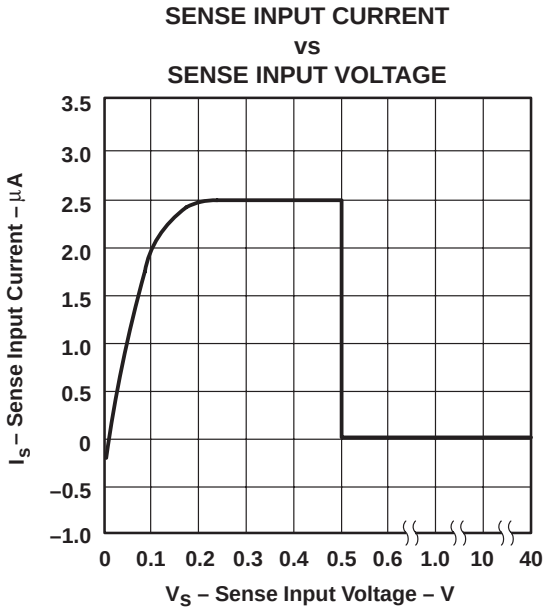


Figure 11

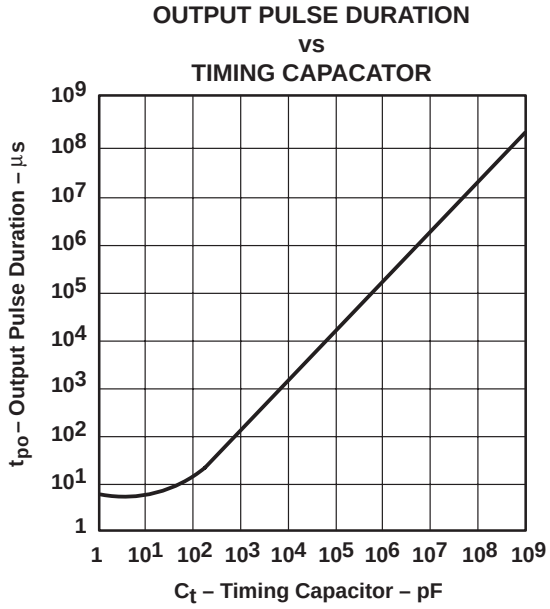


Figure 12

† Data at high and low temperatures are applicable only within the recommended operating conditions.

TYPICAL CHARACTERISTICS

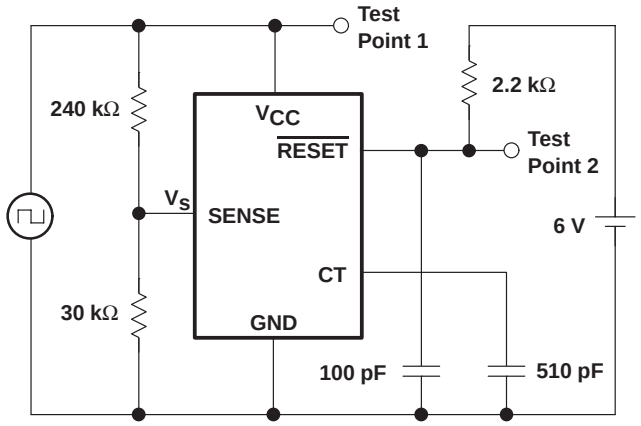


Figure 13. V_{CC} vs Output Test Circuit 1

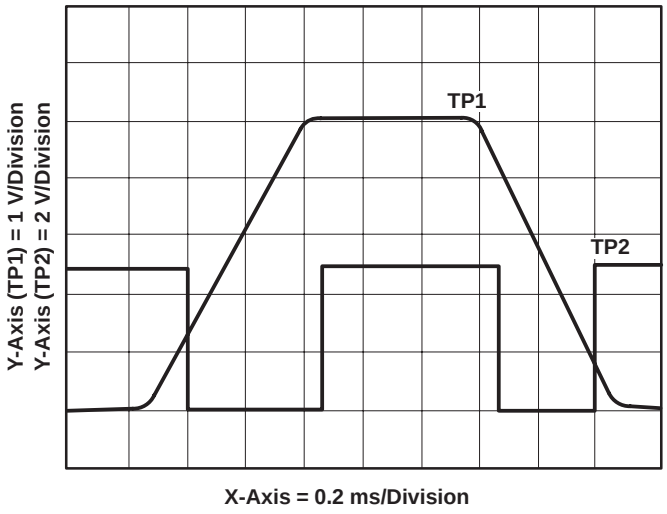


Figure 14. V_{CC} vs Output Waveform 1

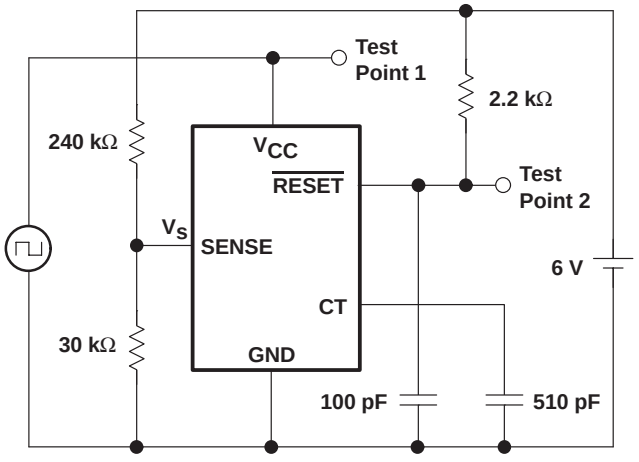


Figure 15. V_{CC} vs Output Test Circuit 2

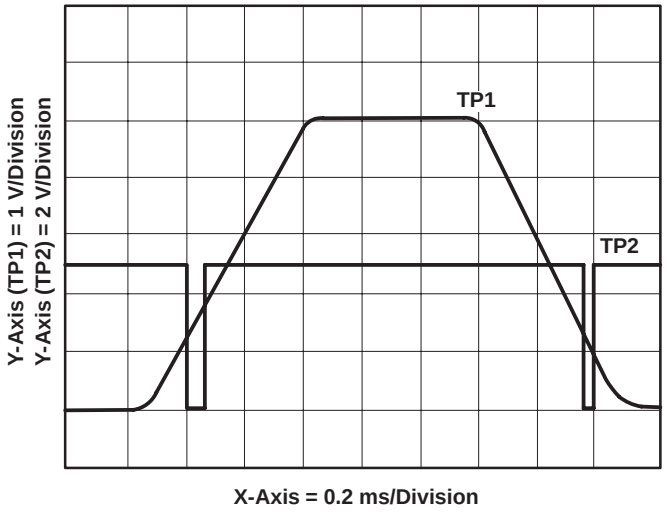


Figure 16. V_{CC} vs Output Waveform 2

TYPICAL CHARACTERISTICS

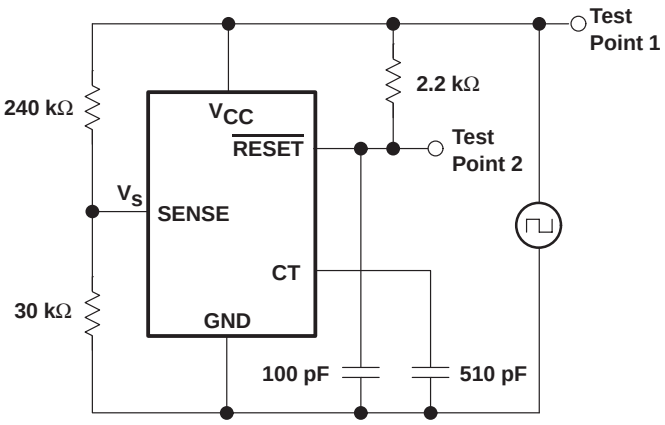


Figure 17. V_{CC} vc Output Test Circuit 3

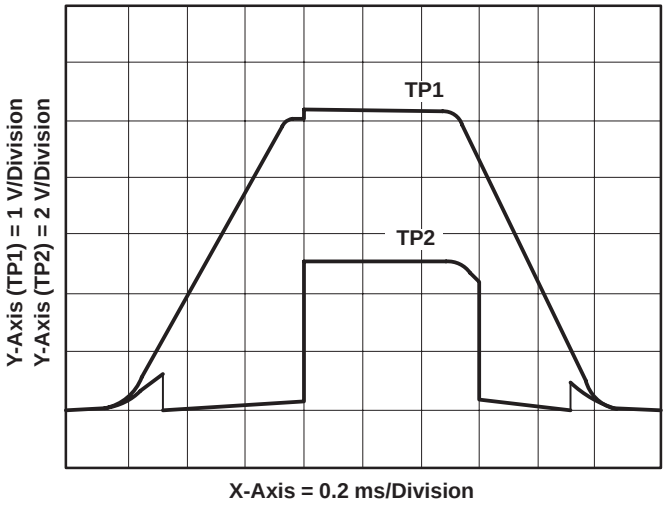


Figure 18. V_{CC} vs Output Waveform 3

detailed description

sense-voltage setting

The SENSE terminal input voltage, V_S, of the TL7700 typically is 500 mV. By using two external resistors, the circuit designer can obtain any sense voltage over 500 mV. In Figure 19, the sensing voltage, $V_{S'}$, is calculated as:

$V_{S'} = V_S \times (R1 + R2)/R2$

Where:

V_S = 500 mV, typically at T_A = 25°C

At room temperature, V_S has a variation of 500 mV ± 5 mV. In the basic circuit shown in Figure 19, variations of [±5 × (R1 + R2)/R2] mV are superimposed on V_S.

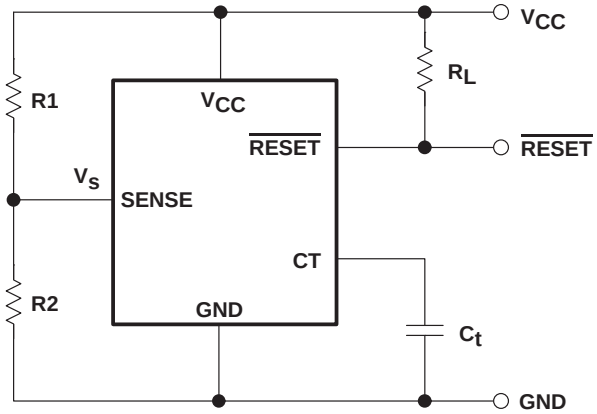


Figure 19

sense-voltage hysteresis setting

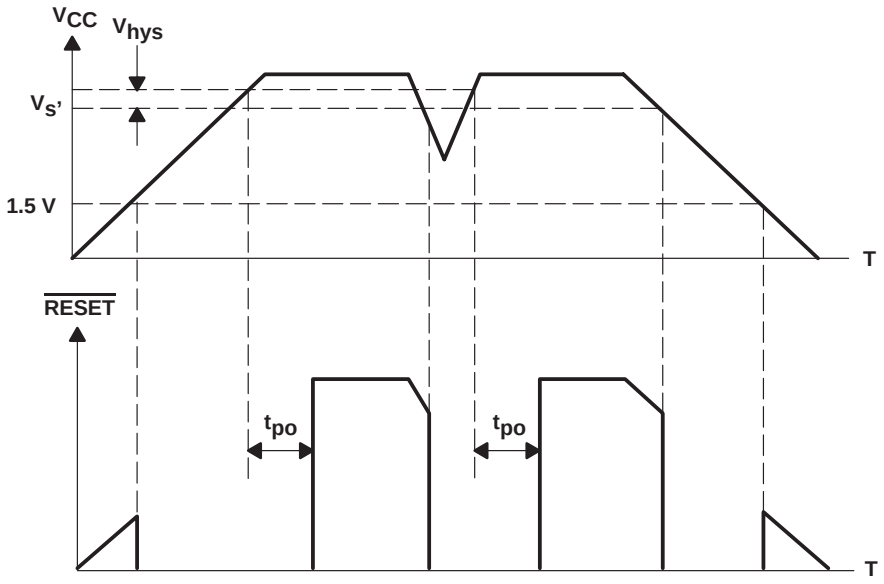
If the sense voltage, $V_{S'}$, does not have hysteresis in it and the voltage on the sensing line contains ripples, the resetting of TL7700 will be unstable. Hysteresis is added to the sense voltage to prevent such problems. As shown in Figure 20, the hysteresis, V_{hys}, is added, and the value is determined as:

$V_{hys} = I_S \times R1$

Where:

I_S = 2.5 μA, typically at T_A = 25°C

At room temperature, I_S has variations of 2.5 μA ± 0.5 μA. Therefore, in the circuit shown in Figure 19, V_{hys} has variations of (±0.5 × R1) μV. In circuit design, it is necessary to consider the voltage-dividing resistor tolerance and temperature coefficient in addition to variations in V_S and V_{hys}.



NOTE A: The sense voltage, $V_{S'}$, is different from the SENSE terminal input voltage, V_S. V_S is normally 500 mV for triggering.

Figure 20. V_{CC}-RESET Timing Chart

output pulse-duration setting

Constant-current charging starts on the timing capacitor when the sensing-line voltage reaches the TL7700 sense voltage. When the capacitor voltage exceeds the threshold level of the output drive comparator, $\overline{\text{RESET}}$ changes from a low to a high level. The output pulse duration is the time between the point when the sense-pin voltage exceeds the threshold level and the point when the $\overline{\text{RESET}}$ output changes from a low level to a high level. When the TL7700 is used for system power-on reset, the output pulse duration, t_{po}, must be set longer than the power rise time. The value of t_{po} is:

$t_{po} = C_t \times 10^5$ seconds

Where:

C_t is the timing capacitor in farads

There is a limit on the device response speed. Even if C_t = 0, t_{po} is not 0, but approximately 5 μs to 10 μs. Therefore, when the TL7700 is used as a comparator with hysteresis, without connecting C_t, switching speeds (t_r/t_f, t_{po}/t_{pd}, etc.) must be considered.

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.