= Preliminary = AK2571

Single-Chip Automatic Power/Temperature Control for WDM Laser Diodes

Features

- Single Chip LSI that integrates APC (Auto Power Control) and ATC (Auto Temperature Control) functions for WDM Laser Module
- A controlling TEC (Thermal Electrical Cooler) stabilizes the temperature of LD module in the range of +/-0.1°C by PID algorithm.
- Parameters controlling Laser Diode are user programmable and stored in EEPROM
- Internal Temperature Sensor detects on-chip temperature, enabling compensation internal and external components that may be affected by changing ambient temperature.
- Autonomous operation (internal oscillator and logic).
- Pin-selectable wavelength data for tunable laser diodes (four options).
- Single 3.3V operation
- 64-pin LQFP or Bare chip

Description

The AK2571 is a single-chip solution for WDM Laser Diode Module applications. It integrates both ATC (Auto Temperature Control) and APC (Auto Power Control) functions in a small 64-pin LQFP or bare die package..

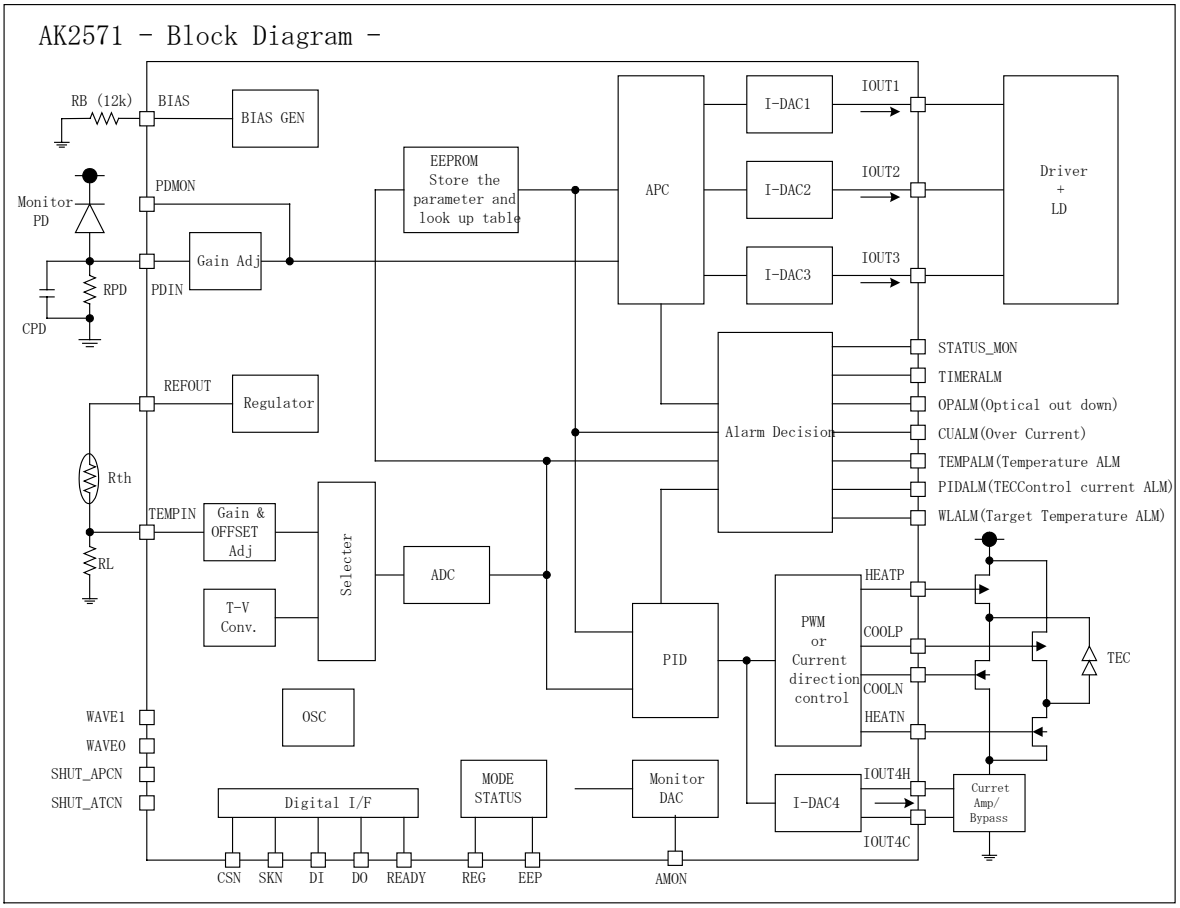
The ATC function of the AK2571 detects the LD module temperature via an external thermister and uses the PID algorithm to control the Thermo-Electric Cooler (TEC). This provides +/- 0.1°C stabilization.. A customer can program the appropriate PID parameters into the internal EEPROM , thereby providing compensation characteristics for each Laser Diode. TEC control is handled through either PWM or Analog current control through I-DAC4. These are easily selected by an EEPROM (Register) setting.

The APC has two functions. The first function is to compensate for Laser Diode power decreases caused by aging. The other function is to compensate for temperature variations of AK2571 and external components (current amplifier or driver circuits) which may be affected by ambient temperature within the LDM. The AK2571 does this by controlling BIAS and modulation current according to the look up table in EEPROM .

The AK2571 has every alarm needed for WDM modules (Loss of power, Over current, Temperature etc.). There is a dithering function for modulation current that improves the extinction ratio for long distance transmissions.

Also, parameter and compensation data can be stored for four wavelengths. If a customer uses a tunable laser diode, it is very easy to change the wavelength by pin control.

Block Diagram



Circuit Description

1. Over view

The AK2571 has two primary functions. The first function is APC (Automatic Temperature Control) which supplies adequate modulation /BIAS current to a Laser diode and the other is ATC (Automatic Temperature control) which controls the TEC (Thermo Electric Cooler) to stabilize the temperature of the Laser diode.

1. 1 APC

There are three Digital to Analog Converters (I-DAC1, 2, 3) that output the current for modulation, BIAS and EA (Electrical Absorption) Modulation.

Maximum output currents :

I-DAC1: 120mA (typ.),

I-DAC2 and I-DAC3: 20mA (typ.)

Each DAC has a current limit function whose value is stored in the internal EEPROM. This is especially important for I-DAC1, which has the modulation function for dithering.

In WDM systems, there is no need for discrete laser diode temperature compensation. However the outer current amplifier or LD drivers may be affected by ambient temperature changes. In order to compensate for these the AK2571 has a feed-forward APC that can supply adequate current corresponding to the ambient temperature change detected by the internal T_V converter.

Please refer the part "**3. APC**" **for** details.

1.2 ATC

The AK2571 controls TEC to stabilize the input voltage from the temperature sensor of the LD module (Thermistor). The control algorithm is PID (Proportion Integration Differential) which has user-programmable parameters that are stored in EEPROM. There are two ways for driving TEC, one is PWM (more energy effective than DC drive), the other is DC current drive through I-DAC, which has lower noise.

Please refer the part "**4. ATC**" **for** details.

1.3 Control Sequence

There are three functional modes in AK2571 below.

1) Self-operation mode: The AK2571 operates ATC and APC independently. When self-operating mode starts, , ATC Lock (detects when the target temperature is reached), APC Count up (prevents jumps in BIAS and Modulation currents) and Timer (counts the time from device start to beginning of operation) are available.

2) Register Access Mode: AK2571 permits writing registers through the digital interface. Customers can adjust any parameters or tables in this mode.

3) EEPROM mode: AK2571 permits EEPROM writes. Customers can store the parameters or table data in EEPROM.

Please refer the part "**5. Sequencer**" for details.

2. Reference

2.1 Definition

All values are expressed in the order shown below

Tab_(Function Block_)Main name(Function_).Sub name[Bit]

Setting way	Tab	Main name	Sub name	Bits	Example
Register	R	REGISTER NAME (Capital letter)	Sub register name	[x,x]	R_PDGAIN R_DAC_SET.Dac1 R_DAC_SET[2:0]
EEPROM	E	EEPROM NAME (Capital letter)	Sub eeprom name	[x,x]	E_PDGAIN E_DAC_SET.Dac1
PIN	P	PIN NAME (Capital letter)			P_WAVE0

Register and EEPROM names may include additional tags as described below

Classify	Additional Tag	Contents	Example
Function Block	APC	APC relate	E_APC_FF_SET
	DAC	I-DAC relate	E_DAC1_FIX
	ATC	ATC relate	E_ATC_OFFSET
	ALM	Alarm relate	E_ALM_POL
	PID	PID relate	E_PID_P
	LK	ATC Lock counter relate	E_LK_CNT_SET
	TMPRT	Temperature decode value	R_TMPRT_TRNT
Function	SET	Settled value (ALM or Counter etc.)	E_DAC1_SET
	WIN	Hysteresis (ALM or counter etc.)	E_TMPRTALM_WIN
	CTRL	Hysteresis (ALM or counter etc.)	E_INI_CTRL_USR
	FIX	Fixed data for APC	E_DAC1_FIX
	TV	APC compensation data	E_DAC1_TV
	CMPNST	LD aging compensation data	R_APC_CMPNST
	TRGT	Target value (Temperature or Voltage etc.)	E_APC_TRGT
	CRNT	Current value	R_TMPRT_CRNT
	BFR	Before value	R_TMPRT_BFR

All circuit blocks and internal nodes are noted as below

	Main name	Example
Circuit Block	BLOCK NAME (Capital letter)	I-DAC1 PID
Internal Node	Signal name (Small letter)	vout

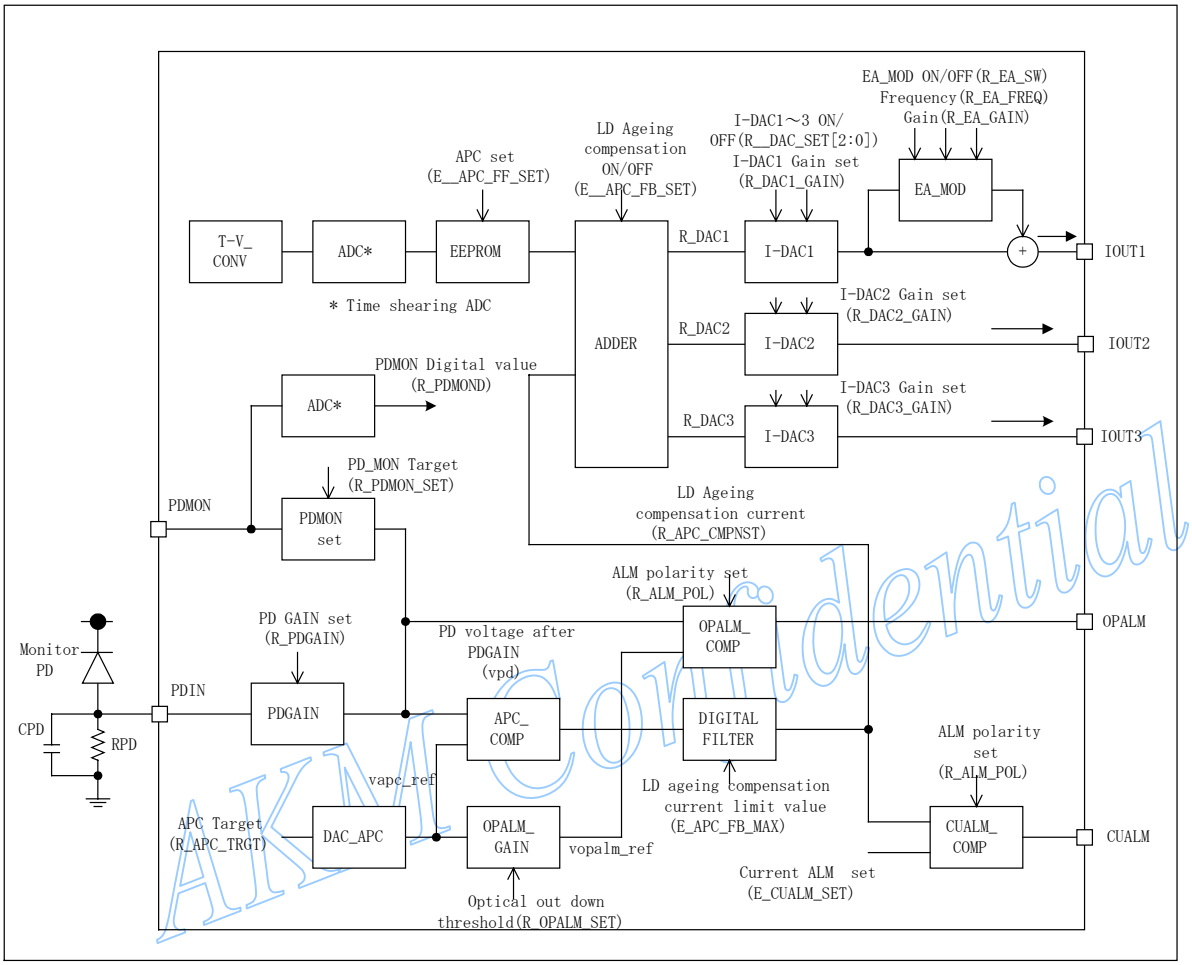
2.2 Functional explanation

Some values are stored in both register and EEPROM to simplify user programming. Explanations of these values are in the register description tables.

For EEPROM details, refer to Section **7. EEPROM**

For Register details, refer to Section **8. Registers**

3. APC (Automatic Power Control)



3.1 Functional description

Block	Function	Note
T_V CONV	Internal Temperature Sensor. Outputs a voltage that corresponds to the surface temperature of the AK2571. This function controls temperature compensation of an external current amplifier, driver IC, etc. By activating the E_APC_FF_SET (=1), the ADC outputs the digital data of T_V CONV as the address of EEPROM stores the lookup table of temperature compensation data for external components every 5.6degree. This data is output through I-DAC and supplies the Laser Diode modulation and BIAS currents. If this function is not required set E_APC_FF_SET to a fixed value and set the current value in E_DACx_FIX.	
ADC	8-bits A-to-D converter for temperature detection. (5-bit MSB is used for temperature compensation)	
EEPROM	E_APC_FF_SET=0 (Default): APC is not activated. Fixed data (E_DACx_FIX, x=1-3) is sent to I-DACs. E_APC_FF_SET=1: APC activation. 5-bits MSB of ADC sent to E_DACxTV[A/D], x=1-3 and work the APC sequence.	
ADDER	E_APC__FB_SET.Dacx(x=1-3)=0 (default): Do not add aging compensation current to I-DACs. E_APC_FB_SET.Dacx(x=1-3)=1: Add aging compensation (R_APC_CMPNST) current to I-DACs.	
I-DAC1	8-bit current output DAC (120mA max.). Output current corresponds to R_DAC1 data. When R_DAC_SET=1, this outputs is enabled.	
I-DAC2	8-bit current output DAC (20mA max.). Output current corresponding to R_DAC1 data. When R_DAC_SET=1, this outputs is enabled.	
I-DAC3	8 bit current output DAC (20mA max.). Output current corresponding to R_DAC1 data. When R_DAC_SET=1, this outputs is enabled.	
EA_MOD	Dithering function. R_EA_SW=0: Non-Active/ 1: Active. R_EA_FREQ: Modulation frequency selection: 16kHz(000), 32kHz(001), 64kHz(010), 128kHz(011) and 256kHz(100). R_EA_GAIN: Additional level to I=DAC1 out selection:16%(00), 8%(01), 10.4%(10) and 2%(11).	
PDGAIN	Amplifies the input signal from the monitoring Photo Diode. (vpd). Customers can set the gain from 0dB to 21dB(Typ.) by 0.7dB steps, using values stored in the EEPROM. Input range: 0.2V - 1.5V Full-scale output through PDMON can be set from 0.4V to1.1V in 0.1V steps. Internal attenuator adjusts the full scale per E_PDMON_SET..	
DACAPC	Generates the target APC (R_APC_TRGT) voltage (vact_ref) in proportion to PDGAIN.	
APC_COMP	Compares the PD monitoring voltage (vpd) with APC target voltage (vapc_ref), if vpd < vapc_ref, outputs UP signals to digital filter. And if vpd > vapc_ref, outputs DOWN signals to digital filter. The sampling rate is 512kHz.	
DIGITAL FILTER	Receives signals from APC_COMP, calculates the value to make vpd and vapc_ref equal. Its value is the LD aging error (R_APC_CMPNST), and is limited by the value of E_APC_FB_MAX. There is no need to supply negative current for aging error.	
CUALM_COMP	LD aging error current (R_APC_CMPNST) over Alarm value (E_CUALM_SET), output CUALM. Its polarity is selected by register R_ALM_POL.	
OPALM_GAIN	OPALM (light sparkle fail) output level (vopalm_ref) setting by register R_OPALM_SET. 000: 1/2, 001: 1/3, 010: 1/4, 011: 1/5, 100: 1/6, 101:1/8	
OPALM_COMP	Compares the PD monitoring voltage (vpd) with OPALM voltage (vpalm), if vpd < vpalm, outputs OPALM (light power down alarm). Its polarity is selected by register R_ALM_POL.	

3.2 Feed forward APC Function

The AK2571 compensates for ambient temperature variations caused by the current amplifier or driver chip located outside of the LD module. If this function is not required, a fixed-current source for the LD can be used instead..

The Feed-forward process is described below:

1) The internal T_V converter (please refer to "**3.6 Internal T-V converter**") senses the ambient temperature. The integrated ADC converts the signal to a digital value.

2) 5-bit MSB data address for the EEPROM stores the temperature compensation data, which is sent to I-DACx.

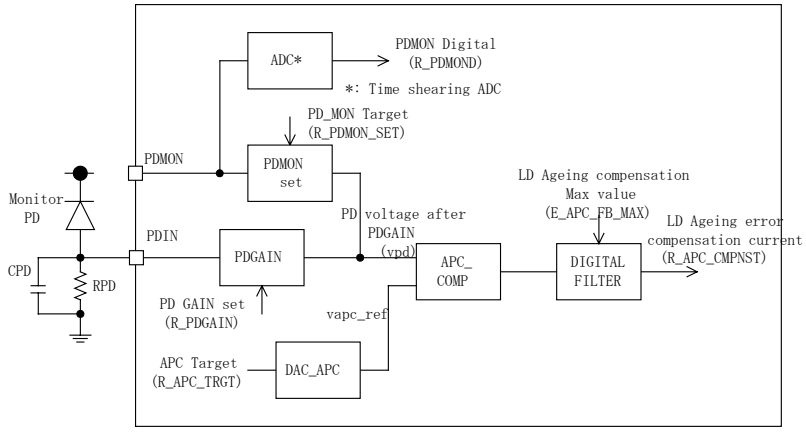
3) Compensation current is output from I-DACx.

To execute feed forward APC, temperature compensation data must be stored in the internal EEPROM as a look-up table that is programmed during the customer assembly process.

In Self-operation mode, all compensation operations (sensing T_V converter, access to EEPROM and compensation current output through I-DACs) are automatically executed.

3.3 LD aging error compensation

Compensation current outputs are available for LD light power deterioration. APC_COMP compares the feedback voltage from PDIN (vpd) with the output voltage of DACAPC (vapc_ref, R_APC_TRGT). Based on this result a compensation current (R_APC_CMPNST) is added to the output current of I-DAC set by E_APC_FB_SET after averaging through a digital filter.



3.3.1 PDMON / PDGAIN setting

Selects the output range from PDMON pin by R_PDMON_SET in the range from0.4 to 1.1V. Adjust the input signal level using R_PD_GAIN (E_PD_GAIN) to make the initial input level equal the value of R_PDMON_SET. Table 3-2 indicates the function of R_PDMON_SET and output voltages, Table 3-3 indicates the function of R_PDGAIN and Gain. After this adjustment, the internal PD input voltage (vpd) is set at 1.8V(typ) in Self-operation mode.

Table 3-2 R_PDMON_SET setting

R_PDMON_SET (E_PDMON_SET)[2:0]	PDMON Full Scale
111	1.1V
-	0.1V / step
000	0.4V

Table 3-3 R_PDGAIN setting

R_PDGAIN_SET (E_PDGAIN_SET)[4:0]	Gain
11111	21.7dB
-	0.7dB / step
00000	0dB

Make sure the PDMON voltage equals the value of R(E)_PDMON_SET.

Conversion expression: Gain = 20*log (1.8 / PDIN voltage)

3.3.2 DACAPC

Generates the reference voltage for aging compensation. Table 3-4 indicates the function of R(E)_APC_TRGT and vapc_ref

R_APC_TRGT (E_APC_TRGT)[6:0]	Reference voltage for Aging compensation (vapc_ref)
1111111	2.1V
|	4.8mV / step
0000000	1.5V

Refer to "**5.3.1 Process - ATC and APC Adjustment Example" for further instructions** regarding the adjustment process, .

3.4 Gain setting of I-DAC1,2,3

See the table below for a description on how to set the three I-DACs full-scale voltages. The resolution is set in proportion with the gain.

I-DAC1 gain setting

R_DAC1_GAIN (E_DAC1_GAIN)	Gain set value	Max output current (typ)	Setting range of output current (typ)	Non missing code warranty range (typ)	Current resolution (typ)
00	1	121.8mA	30mA-121.8mA	30mA over	0.36mA
01	1/2	60.9mA	15mA-60.9mA	15mA over	0.18mA
10	1/4	30.45mA	7.5mA-30.45mA	7.5mA over	0.09mA
11	1/12	10.15mA	2.5mA-10.15mA	2.5mA over	0.03mA

I-DAC2 Gain setting

R_DAC1_GAIN (E_DAC1_GAIN)	Gain set value	Max output current (typ)	Setting range of output current (typ)	Non missing code warranty range (typ)	Current resolution (typ)
00(11)	1	20.42mA	0mA-21.42mA	2.5mA over	0.084mA
10	1/2	10.71mA	0mA-10.71mA	1.25mA over	0.042mA
11	1/4	5.36mA	0mA-5.36mA	0.625mA over	0.021mA

I-DAC3 Gain setting

R_DAC1_GAIN (E_DAC1_GAIN)	Gain set value	Max output current (typ)	Setting range of output current (typ)	Non missing code warranty range (typ)	Current resolution (typ)
00(11)	1	21.42mA	0mA-20.42mA	2.5mA over	0.084mA
10	1/2	10.71mA	0mA-10.71mA	1.25mA over	0.042mA
11	1/4	5.36mA	0mA-5.36mA	0.625mA over	0.021mA

3.5 Modulation for dithering through I-DAC1

I-DAC1 has a modulation function for dithering. It's added to the current of I-DAC1 and output through IOUT1. Its function is available to set R_EA_SW.

Figure 3-3 shows the block diagram and Table 3-8 / 3-9 explains the setting

Figure 3-3 EA Block diagram

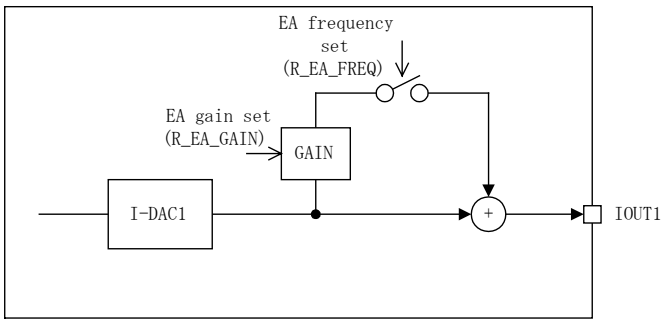


Table 3-8 EA Dithering frequency

R_EA_FREQ (E_EA_FREQ)	Setting frequency (Typ)	Deviation (typ)	Remarks
000	16kHz	TBD	(Default)
001	32kHz	TBD	
010	64kHz	TBD	
011	128kHz	TBD	
100-111	256kHz	TBD	

Table 3-9 Additional gain

R_EA_GAIN (E_EA_GAIN)	Additional gain	Deviation (typ)	Remarks
00	16%	TBD	(Default)
01	8%	TBD	
10	4%	TBD	
11	2%	TBD	

3.6 Internal T_V converter

The internal temperature sensor's output voltage function is shown in Figure 3-4. This offset is different for each device, and is adjusted during factory test by AKM. If re-adjustment of the offset is necessary (for higher accuracy, etc.), it is possible to rewrite the R(E)_TV_OFFSET. Table 3-10 diagrams the offset voltage and R_TV_OFFSET. The internal T_V converter has a gain of –12.3mV / degree (typ) and the 8-bit ADC (full scale is 2.2V) is changed 0.7degree for each LSB. Actually, only 5bits MSB of ADC is valid for feed forward APC, so the compensation data is renewed every 5.6 degrees.

The internal T_V converter monitors the surface temperature of the AK2571 and detects any difference between this temperature, the ambient temperature and the temperature of external components. It is possible to increase the accuracy of this function by "training" the device beforehand and writing the compensation data trained as described below.

1) Single-point temperature adjustment

Read R_TV at one ambient temperature, and using the T_V Conv. Gain (-0.7degree/LSB), calculates the 8-bit ADC value and enter it into the look-up table address for Feed forward APC.

By performing this training, the offset error can be cancelled. Of course this training must be executed in conjunction with an APC adjustment. Please refer to **5.3.1 APC/ATC adjustment.**

2) Two-point temperature adjustment

Read R_TV at two ambient temperatures, calculate the T_V Conversion gain. From this gain, calculate the 8-bit ADC value and enter it into the look-up table address for Feed forward APC.

By performing this training, the offset error and gain variation can be cancelled. Of course this training must be executed in conjunction with an APC adjustment. Please refer to **5.3.1 APC/ATC adjustment.**

Figure 3-4 Internal Temperature Sensor

Table 3-10 R_TV_OFFSET setting

R_TV_OFFSET[4:0] E_TV_OFFSET[4:0]	Offset voltage [mV] (Reference value)
11111	+375
11110	+350
11101	+325
10001	+25
10000	0
01111	-25
00010	-350
00001	-375
00000	-400

Default value of E_TV_OFFSET is set by AKM.

3.7 Example schematics of connection to external components

Figures 3-5 to 3-10 illustrate typical system connections. When connecting to a negative voltage source, use a level shifter to ensure that the signal voltages stays within the specified range.. In addition to that, I-DAC1 can't be forced negative voltage supply.

Figure 3-5
Direct Modulation with Positive Power Supply

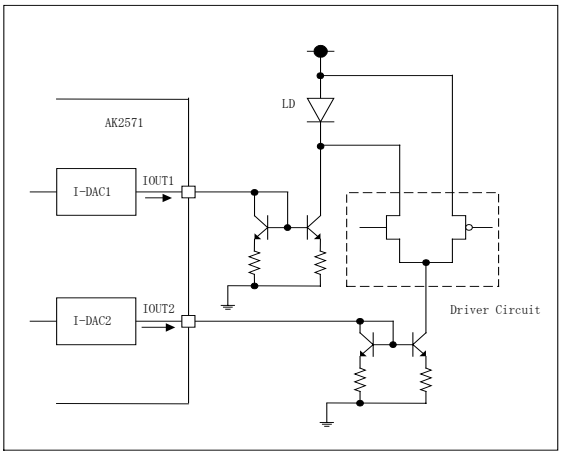


Figure-3-6
Direct Modulation with Negative Power Supply

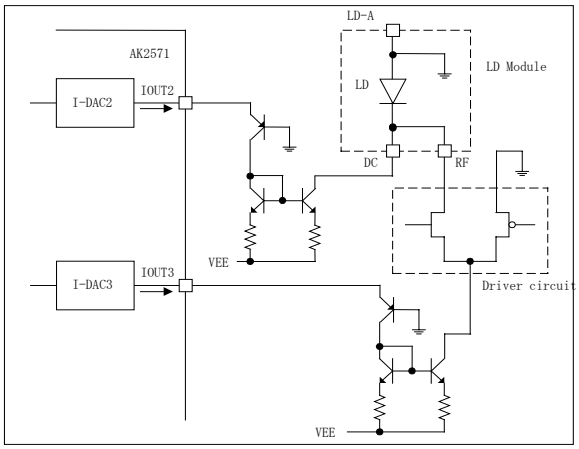


Figure 3-7
Direct Modulation with Voltage Controlled LD Driver

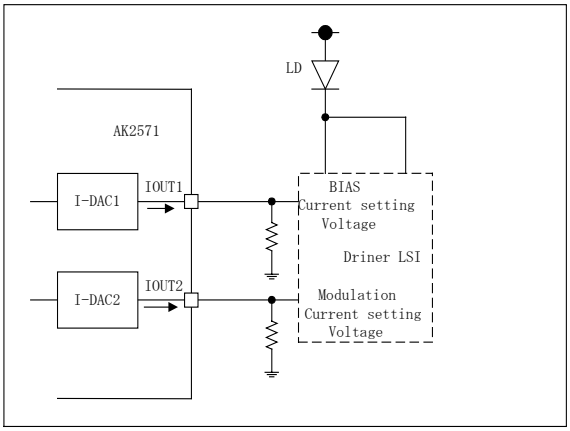


Figure 3-8
Direct Modulation with Voltage Controlled LD Driver

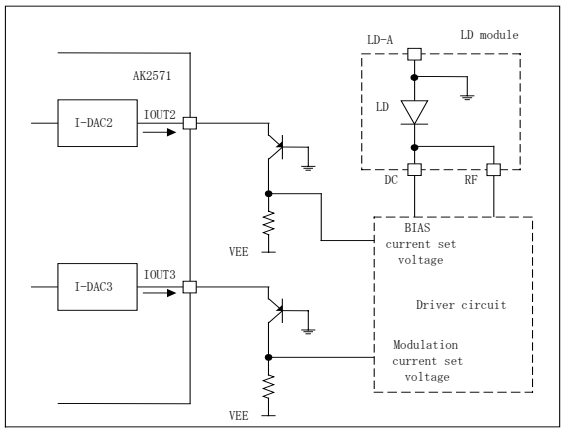


Figure 3-9
EA Modulation

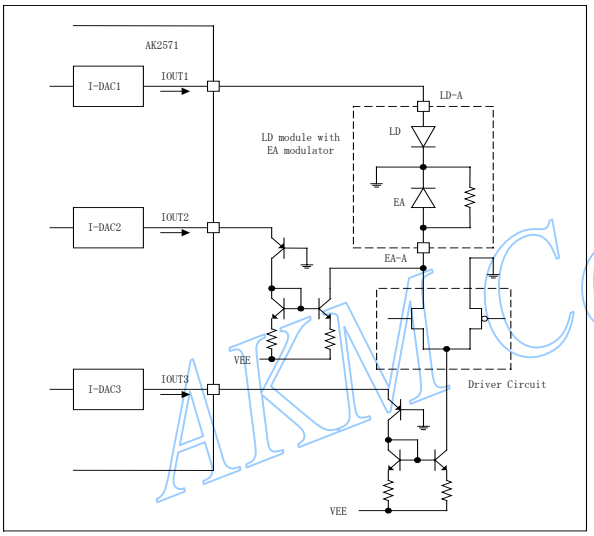
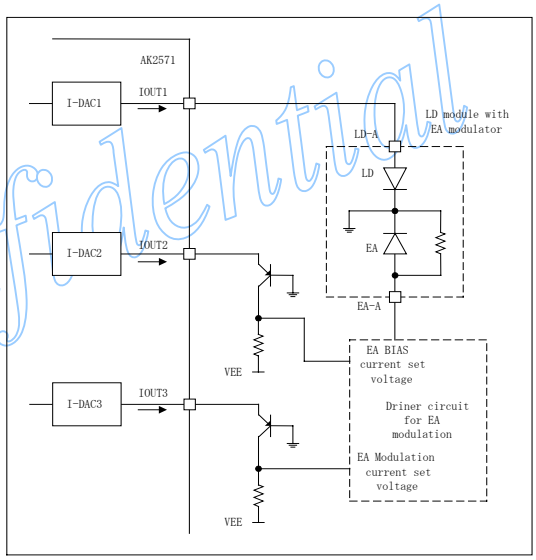
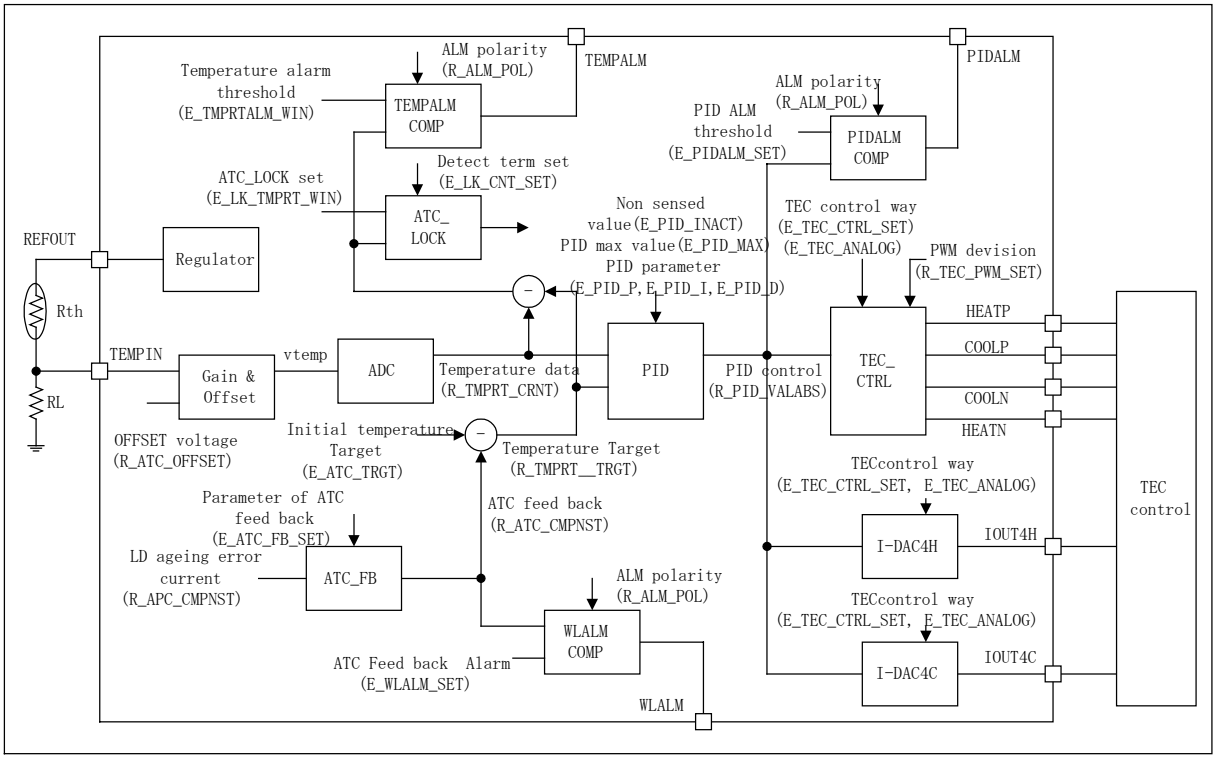


Figure 3-10
EA with Voltage Controlled LD Drive



4. ATC (Automatic Temperature Compensation)

Figure 4-1 ATC Block diagram



4.1 ATC Block Explanation

Table 4-1 indicates the functions of the ATC block

Block	Function	Remarks
Regulator	Supplies voltage to thermister included in the LD module. REFOUT=2.3V (typ). Thermister output voltage (TEMPIN) error tracks the varying voltage supply temperature characteristics of REFOUT and automatically calculates and cancels this in the AK2571.	
Gain & Offset	AK2571 amplifies (x13 typically) the input signal to enable higher resolution from the 8-bit ADC. The input signal should be set to the midpoint of its full scale to meet the target temperature of the offset setting function. For example, when thermister R0=10kohm.@25 degree, B=3900, load resistance 6.8kohm., its sensitivity is about 0.03degree/LSB.	
ADC	8b-it A-to-D converter. Reference voltage is 2.2V (typ). Temperature signal from Gain & OFFSET is converted to digital and transferred to PID calculator.	
PID	Executes a PID (Proportion, Integration and differential) calculation to meet the temperature signal (R_TMPRT_CRNT) at the target temperature (R_TMPRT_TRGT). Output data (R_PID_VALABS) is composed of 13-bits absolute value and a positive/negative bit. Each PID parameter can be set in the EEPROM. The cycle time for this calculation is 8mS (typ) and is set by the internal oscillator.	
TEC_CTRL	Using the PID data (R_PID_VALABS), the TEC (Thermo Electric Cooler) is controlled by PWM or Analog control. When PWM control is selected, the FET switch is controlled through the PWM division set register (R_TEC_PWM_SET).	
I-DAC4H I-DAC4C	10b-it current D-to-A converter. When analog control for TEC is selected, the IDAC outputs current following 10bits MSB data from PID. Its full-scale output current is 50mA (typ). When Analog-1 is selected (Control the current direction by FET: refer to figure 4-4), it is possible for I-DAC4H to output both cooling and heating current, depending on current direction. On the other hand, when Analog-2 is selected, heating current is output through I-DAC4H (I-DAC4C output is GND) and cooling current is output through I-DAC4C (I-DAC4H output is GND).	
ATC_FB	Change the target temperature according to LD aging error from PD monitor voltage. Its value (R_ATC_CMPNST) is calculated from the parameter (E_ATC_FB_SET). This function assumes that there is first order function between the LD aging error and moving the wavelength to the longer, can compensate wavelength shift cause from aging. When use this function, please note this assumption carefully.	
ATC_LOCK	Detect the stabilization of LD temperature from start or reset of AK2571. The stabilization judge range (E_LK_TMPRT_WIN) and its decision term (E_LK_CNT_SET) are set in EEPROM. If the LD temperature data (R_TMPRT_CRNT) stays within the stabilization judge range for a period that is longer than the decision term, the AK2571 moves to the next operation.	
TEMPALMCOMP	If the difference between LD temperature data (R_TMPRT_CRNT) and target temperature (R_TMPRT_TRGT) exceeds the temperature alarm threshold (E_TEMPALM_WIN), TEMPALM is triggered. RegisterI R_ALM_POL sets the polarity of this signal.	
PIDALMCOMP	When the PID control value (R_PID_VALUE) exceeds the PID alarm threshold (E_PIDALM_SET), PID alarm is triggered. RegisterI R_ALM_POL sets the polarity of this signal	
WLALMCOMP	When the aging target temperature aging (R_ATC_CMPNST) is exceeds the threshold of the wavelength aging error alarm (E_WLALM_SET), WLALM is output. Its polarity is selectable by the R_ALM_POL register.	

4.2 PID control

Figure 4-2 explains the block diagram for PID control and table 4-3 indicates the parameter setting range

Figure 4-2 PID control

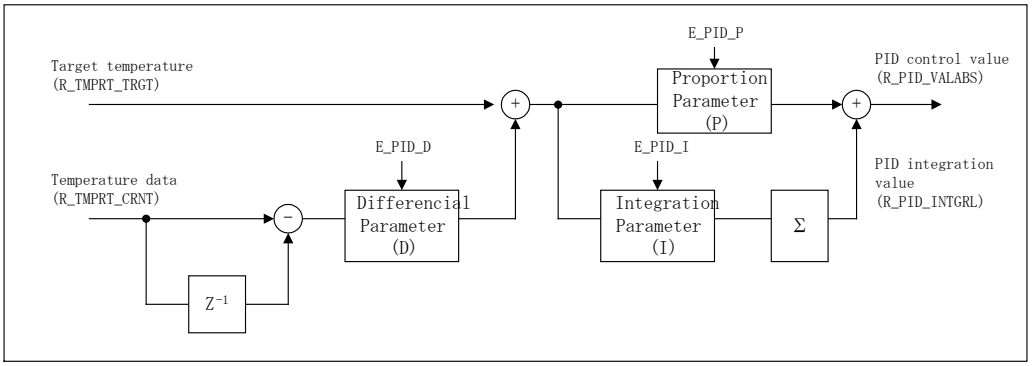


Table 4-3: PID parameter setting range

Parameter	EEPROM	Min.	Default	Max.
Proportion	E_PID_P	0	8	255
Integration	E_PID_I	0	7/256	255/256
Differential	E_PID_D	0	6/256	255/256

4.3 TEC control

The TEC control process is illustrated in table 4-4. Figures 4-3 to 4-6 explain the circuit that drives TEC and table 4-5 indicate the pin strapping for different control modes.

Figure 4-3 PWM control

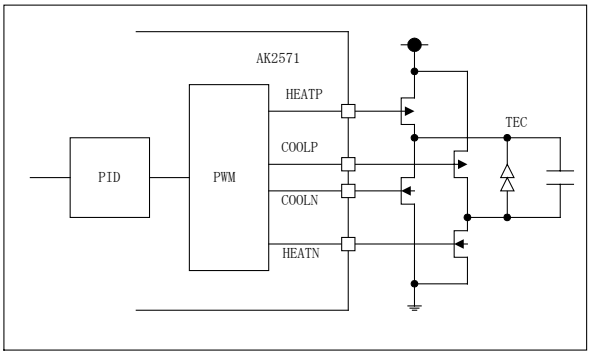


Figure 4-4 Analog control-1

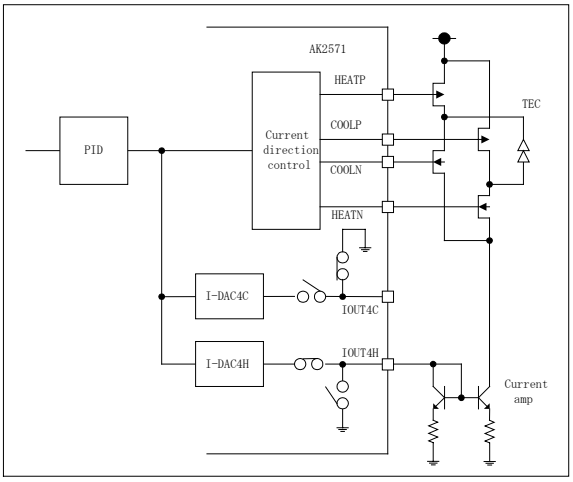


Figure 4-5 Analog control 2-1

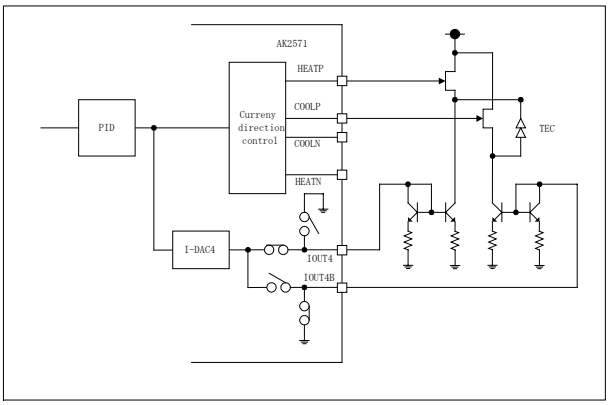


Figure 4-6 Analog control 2-2

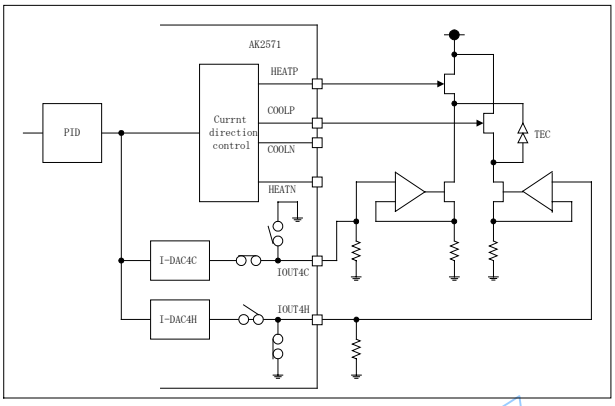
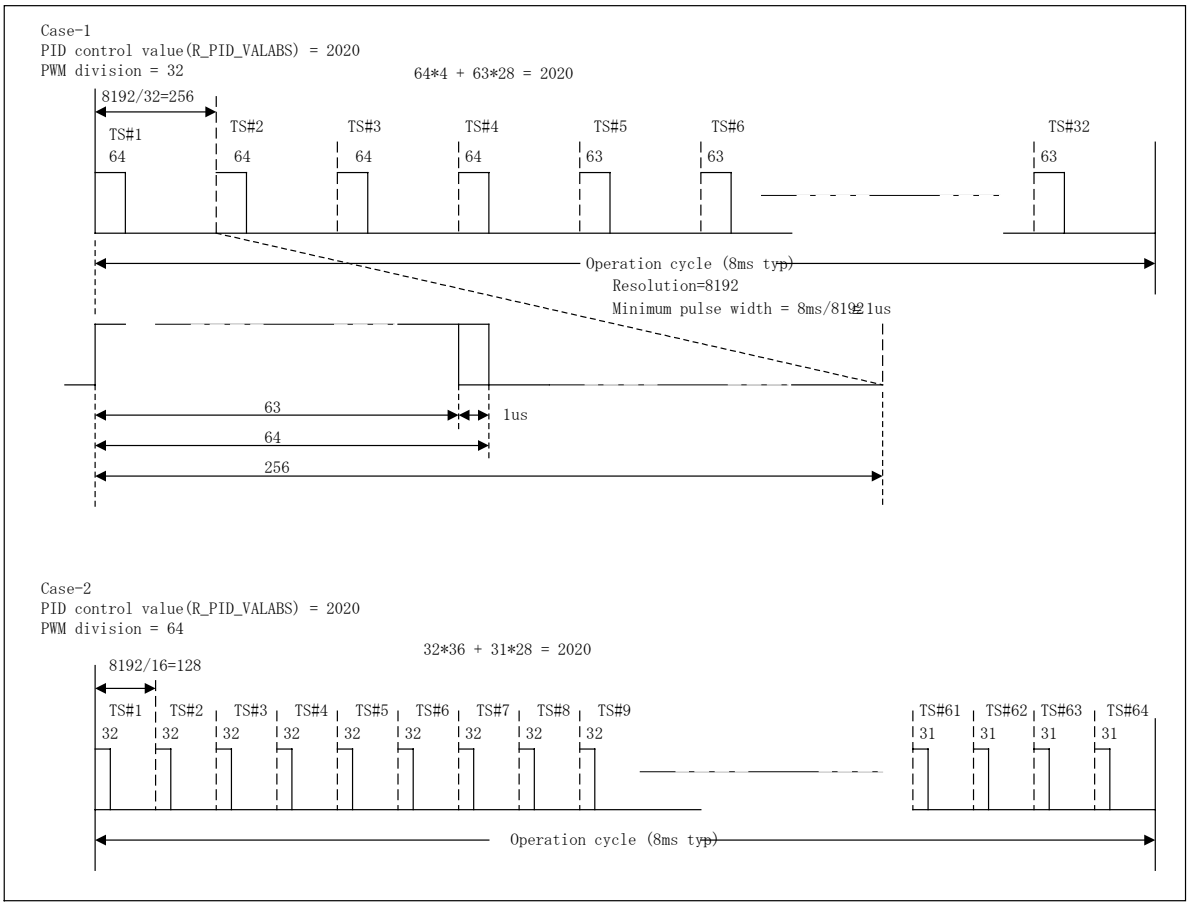


Table 4-5 pin status

PID data	TEC	Control way	IOUT4H	IOUT4C	HEAT_P	HEAT_N	COOL_P	COOL_N
PID=0	OFF	PWM	GND	GND	1	0	1	0
		Analog-1	GND	GND	1	0	1	0
		Analog-2	GND	GND	1	0	1	0
PID>0	Heating	PWM	GND	GND	0	PWM	1	0
		Analog-1	Current out	GND	0	1	1	0
		Analog-2	Current out	GND	0	0	1	0
PID<0	Cooling	PWM	GND	GND	1	0	0	PWM
		Analog-1	Current out	GND	1	0	0	1
		Analog-2	GND	Current out	1	0	0	0

Figure 4-7 PWM division



4.4 Gain & Offset

The AK2571 amplifies (typically x13) the input signal from the thermister to provide higher resolution for the 8-bit ADC. It also adds an offset voltage to meet the middle of full scale at target temperature. Table 4-6 indicates temperature levels that correspond to ADC values when using a thermister R0=10kohm@25degree, B=3900 and Table 4-7 indicates a thermister R0=10kohm@25degree, B=3450. Both load resistances RL) are 6.8kohm, REFOUT is 2.3V. When adjusting Offset voltage (R_ATC_OFFSET), target temperature must be a value between 96 (60h) and 160 (A0h).

Table 4-6 Temperature corresponding to code of ADC (Thermister: R0=10kohm@25degree,B=3900)

R_ATC_OFFSET	Offset voltage [V]	Temperature [degree] (typ)				
		ADC=0	ADC=96	ADC=128	ADC=160	ADC=256
0	0.30	-7.6	-3.2	-1.9	-0.6	3.0
1	0.33	-5.6	-1.5	-0.2	1.0	4.5
2	0.36	-3.8	0.2	1.4	2.6	5.9
3	0.39	-2.0	1.8	2.9	4.1	7.3
4	0.42	-0.3	3.3	4.4	5.5	8.7
5	0.45	1.3	4.7	5.8	6.9	10.0
6	0.48	2.8	6.2	7.2	8.3	11.3
7	0.51	4.3	7.5	8.6	9.6	12.5
8	0.54	5.7	8.9	9.9	10.9	13.8
9	0.57	7.1	10.2	11.2	12.2	15.0
10	0.60	8.5	11.5	12.5	13.4	16.2
11	0.63	9.8	12.7	13.7	14.6	17.4
12	0.66	11.1	14.0	14.9	15.8	18.5
13	0.69	12.4	15.2	16.1	17.0	19.7
14	0.72	13.6	16.4	17.3	18.2	20.9
15	0.75	14.8	17.6	18.5	19.4	22.0
16	0.78	16.0	18.8	19.6	20.5	23.2
17	0.81	17.2	19.9	20.8	21.7	24.3
18	0.84	18.4	21.1	21.9	22.8	25.4
19	0.87	19.6	22.2	23.1	24.0	26.6
20	0.90	20.7	23.4	24.2	25.1	27.7
21	0.93	21.9	24.5	25.4	26.2	28.8
22	0.96	23.0	25.6	26.5	27.4	30.0
23	0.99	24.1	26.8	27.6	28.5	31.1
24	1.02	25.3	27.9	28.8	29.6	32.2
25	1.05	26.4	29.0	29.9	30.8	33.4
26	1.08	27.5	30.2	31.0	31.9	34.5
27	1.11	28.7	31.3	32.2	33.1	35.7
28	1.14	29.8	32.4	33.3	34.2	36.9
29	1.16	30.9	33.6	34.5	35.4	38.1
30	1.19	32.1	34.7	35.6	36.6	39.3
31	1.22	33.2	35.9	36.8	37.7	40.5
32	1.25	34.4	37.1	38.0	38.9	41.7
33	1.28	35.6	38.3	39.2	40.2	43.0
34	1.31	36.7	39.5	40.4	41.4	44.3
35	1.34	37.9	40.7	41.7	42.6	45.6
36	1.37	39.1	42.0	42.9	43.9	46.9
37	1.40	40.3	43.2	44.2	45.2	48.3
38	1.43	41.6	44.5	45.5	46.5	49.7
39	1.46	42.8	45.8	46.8	47.9	51.1
40	1.49	44.1	47.2	48.2	49.3	52.5
41	1.52	45.4	48.5	49.6	50.7	54.0
42	1.55	46.7	49.9	51.0	52.1	55.6
43	1.58	48.1	51.3	52.5	53.6	57.2
44	1.61	49.5	52.8	54.0	55.1	58.8
45	1.64	50.9	54.3	55.5	56.7	60.6
46	1.67	52.3	55.9	57.1	58.4	62.3
47	1.70	53.8	57.5	58.7	60.1	64.2

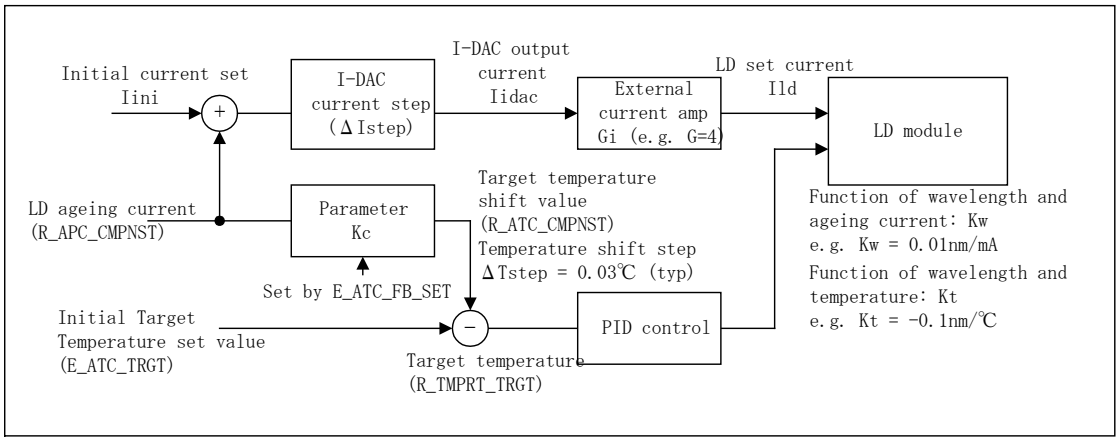
Table 4-6 Temperature levels corresponding to ADC values (Thermister: R0=10kohm@25degree,B=3450)

R_ATC_OFFSET	Offset voltage [V]	Temperature [degree] (typ)				
		ADC=0	ADC=96	ADC=128	ADC=160	ADC=256
0	0.30	-11.3	-6.3	-4.7	-3.3	0.9
1	0.33	-9.2	-4.4	-2.9	-1.5	2.5
2	0.36	-7.1	-2.6	-1.2	0.2	4.0
3	0.39	-5.2	-0.8	0.5	1.8	5.6
4	0.42	-3.3	0.9	2.2	3.4	7.1
5	0.45	-1.5	2.5	3.7	5.0	8.5
6	0.48	0.2	4.0	5.3	6.5	10.0
7	0.51	1.8	5.6	6.8	8.0	11.4
8	0.54	3.4	7.1	8.2	9.4	12.7
9	0.57	4.9	8.5	9.7	10.8	14.1
10	0.60	6.5	10.0	11.1	12.2	15.4
11	0.63	7.9	11.4	12.5	13.6	16.8
12	0.66	9.4	12.7	13.8	14.9	18.1
13	0.69	10.8	14.1	15.2	16.3	19.4
14	0.72	12.2	15.4	16.5	17.6	20.7
15	0.75	13.5	16.8	17.8	18.9	22.0
16	0.78	14.9	18.1	19.1	20.2	23.3
17	0.81	16.2	19.4	20.4	21.5	24.6
18	0.84	17.5	20.7	21.7	22.8	25.8
19	0.87	18.9	22.0	23.0	24.1	27.1
20	0.90	20.2	23.3	24.3	25.3	28.4
21	0.93	21.5	24.6	25.6	26.6	29.7
22	0.96	22.7	25.8	26.9	27.9	31.0
23	0.99	24.0	27.1	28.1	29.2	32.3
24	1.02	25.3	28.4	29.4	30.5	33.6
25	1.05	26.6	29.7	30.7	31.8	34.9
26	1.08	27.9	31.0	32.0	33.1	36.2
27	1.11	29.1	32.3	33.3	34.4	37.5
28	1.14	30.4	33.6	34.6	35.7	38.9
29	1.16	31.7	34.9	35.9	37.0	40.3
30	1.19	33.0	36.2	37.3	38.4	41.6
31	1.22	34.3	37.5	38.6	39.7	43.0
32	1.25	35.7	38.9	40.0	41.1	44.5
33	1.28	37.0	40.3	41.4	42.5	45.9
34	1.31	38.3	41.6	42.8	43.9	47.4
35	1.34	39.7	43.0	44.2	45.4	48.9
36	1.37	41.1	44.5	45.6	46.8	50.4
37	1.40	42.5	45.9	47.1	48.3	52.0
38	1.43	43.9	47.4	48.6	49.8	53.6
39	1.46	45.3	48.9	50.1	51.4	55.3
40	1.49	46.8	50.4	51.7	53.0	57.0
41	1.52	48.3	52.0	53.3	54.6	58.8
42	1.55	49.8	53.6	55.0	56.3	60.6
43	1.58	51.4	55.3	56.7	58.1	62.4
44	1.61	53.0	57.0	58.4	59.9	64.4
45	1.64	54.6	58.8	60.2	61.7	66.4
46	1.67	56.3	60.6	62.1	63.6	68.5
47	1.70	58.0	62.4	64.0	65.6	70.7

4.5 ATC Feedback function

The ATC Feedback function compensates for wavelength shifts caused by aging. R_CTRL_USER.Atc_fb = "1" enables the function, "0" disables it. Turning on this function changes the target temperature according to LD aging error from the PD monitor voltage. Its value (R_ATC_CMPNST) is calculated from (E_ATC_FB_SET). This function assumes that there is a first order function between the LD aging error and wavelength increases and uses this function to compensate for this shift caused by aging. When using this function, please note this assumption carefully. Figure 4-8 indicates the block diagram for this function.

Figure 4-8 ATC Feedback Block



Its operation is described below

1) With LD aging error engaged, initiate the APC compensation circuit. LD compensation current (Digital) is added to the I-DACs selected by R_APC_CMPNST.
2) Calculate the shift value of the target temperature (R_ATC_CMPNST) from the compensation current and the parameter stored in E_ATC_FB_SET (=Kc).
3) Shift the target temperature (R_TMPRT_TARGET) which is the initial target temperature (E_ATC_TRGT) minus the shift value of target temperature (R_ATC_CMPNST).

Kc as above is calculated by the expression below.

If the shift value of wavelength is $\Delta\lambda 1$, Compensation current (Analog) is ΔIld,

$\Delta\lambda 1 = Kw * \Delta Ild$ ..... (1)

If the rate of analog output current per one step of I-DACs is $\Delta Istep$, the gain of external current amplifier is Gi,

The value of compensation current (Digital)

$R\_APC\_CMPNST = \Delta Ild / Gi / \Delta Istep$ ..... (2)

The shift value of target temperature

$R\_ATC\_CMPNST = Kc * R\_APC\_CMPNST$ ..... (3)

If the rate of temperature shift per one step of R_ATC_CMPNST is $\Delta Tstep$, the value of wavelength shift by the shift of target temperature is $\Delta\lambda 2$,

$\Delta\lambda 2 = Kt * R\_ATC\_CMPNST * \Delta Tstep$ ..... (4)

In that sense the value of Kc to make $\Delta\lambda 1 = \Delta\lambda 2$, for compensation of the wavelength shift.

$Kc = Kw * Gi / Kt * \Delta Istep / \Delta Tstep$ ..... (5)

For example: If Kw=0.01nm/mA, Gi=4, Kt=0.1nm/°C, $\Delta Istep$=0.08mA/step, $\Delta Tstep$=0.03°C/step, Kc=1.07.

Since this function does not actually watch the wavelength, care must be exercised when setting these values.

Parameter values of Kc can be selected from 0.125, 0.25, 0.375, 0.5, 0.625, 0.75, 1.0, 1.125, 1.25 and 1.5.

5. Sequencer

5.1 Operation mode

The AK2571 has three operation modes shown below. Use the serial interface to change from one mode to another. Figure 5-1 shows the operating flowchart and table 5-1 indicates the circuit block capabilities.

1) Self-operation mode: Operates ATC and APC automatically according to the data stored in EEPROM.
2) Register access mode: Adjust the data to set the characteristics of LD. Read and write registers are accessed by writing commands to the Digital interface.
3) EEPROM access mode: Fix the adjusted data and parameters in EEPROM. Data in register are written in EEPROM and reset. All ATC and APC functions are disabled in this mode.

Figure 5-1

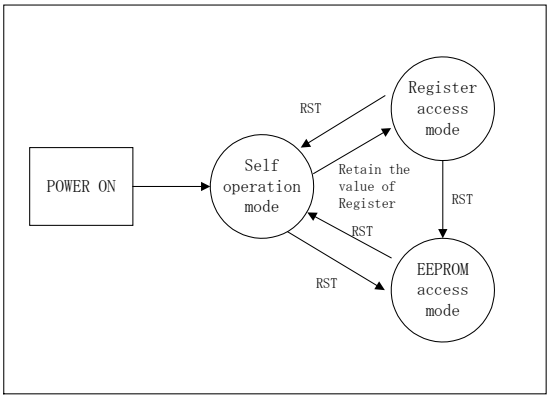


Table 5-1

		Self operation mode	Register access	EEPROM access
Register	Read	O.K.	O.K.	Non
	Write	Non	O.K.	Non
EEPROM	Read	Non	Non	O.K.
	Write	Non	Non	O.K.
Status	P_EEP	0	0	1
APC		Auto operation by EEPROM data	Operation by register data	Shut Down
ATC		Auto operation by EEPROM data	Auto operation by register data	Shut Down

5.2 Self operation mode

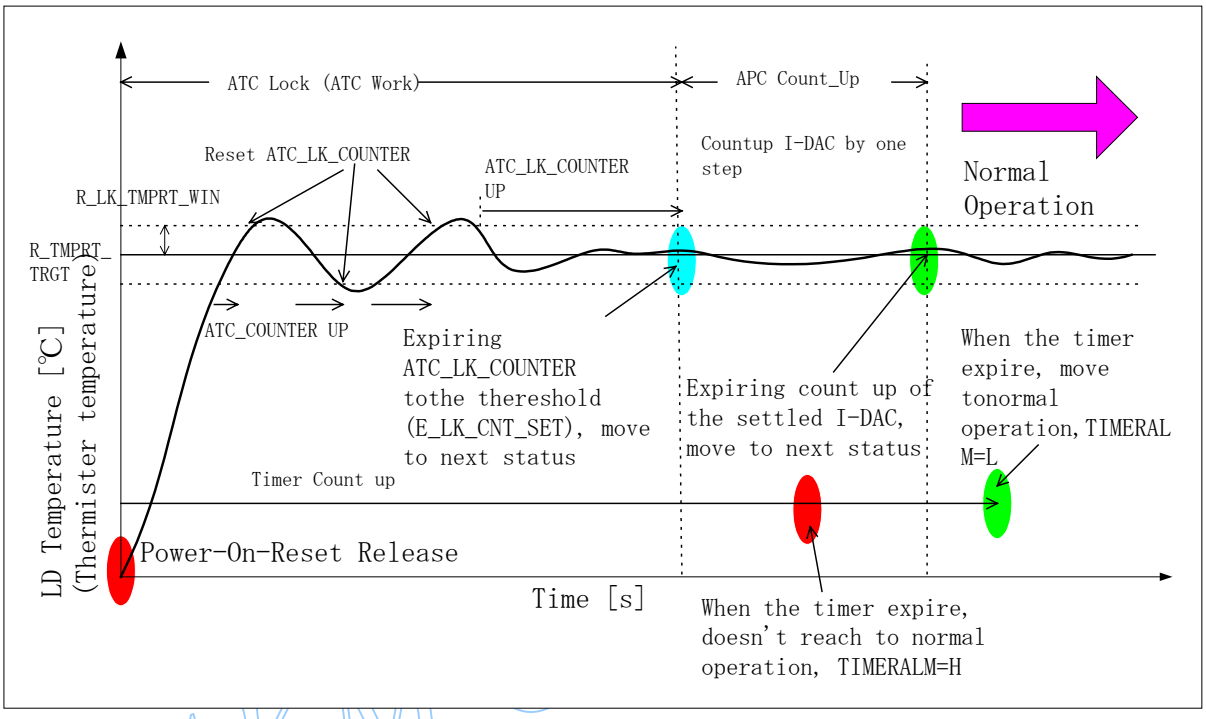
5.2.1 Start up sequence

The AK2571 has various start-up sequence patterns that set the control register (R_CTRL_AKM / R_CTRL_USER). The AK2571 automatically executes the start up sequence stored in EEPROM when it is started or re-start. Table 5-2 and Figure 5-2explains each sequence.

Table 5-2

	Condition of finish	ATC status	APC status	APC_FB	ATC_FB	APCALM	ATCALM
Power ON							
⇩							
Status-1 (Only ATC work)	ATC Lock	ATC Lock	Disable	Disable	Disable	User setting	User setting
⇩							
Status-2 (APC Count up work)	APC Count up	Normal operation	Count up or Disable (User setting)	Disable	Disable	User setting	User setting
⇩							
Status-3 (Normal operation)		Normal operation	Normal operation	User setting	User setting	User setting	User setting

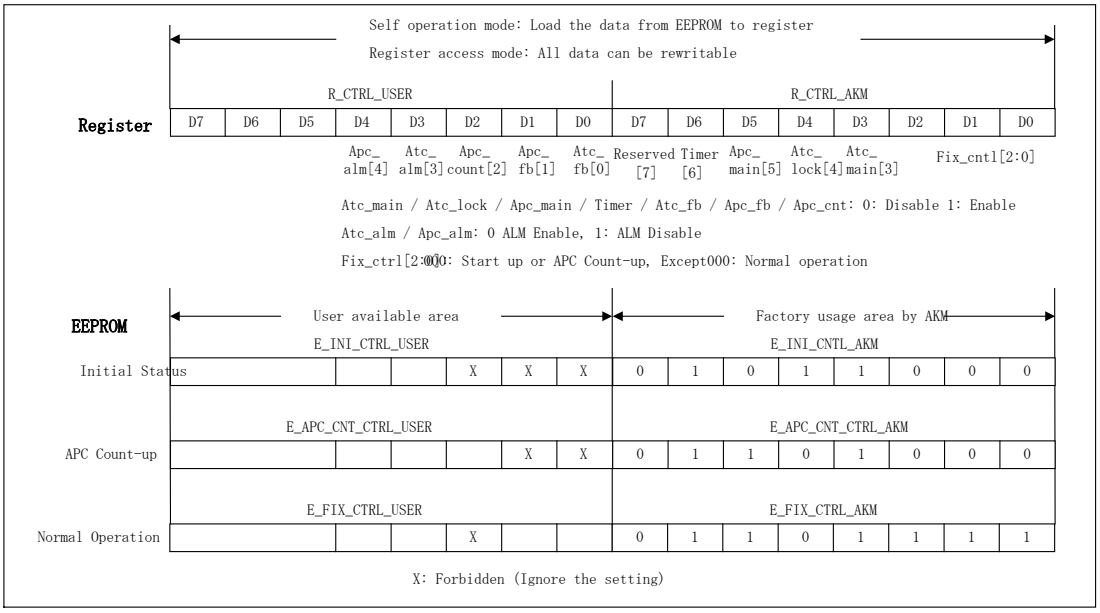
Figure 5-2 Start up sequence



5.2.2 Control registers

Figure 5-3 illustrates the register format. There are two areas in these registers, one is for AKM factory use and the other is for user customization. Even though both areas are re-writable, the AKM values SHOULD NOT BE OVERWRITTEN. If the AKM values are modified product functionality cannot be guaranteed.

Figure 5-3 Control Register



5.2.3 ATC Lock

1) When temperature data (R_TMPRT_CRNT) enters the target temperature range (R_TMPRT_TRGT) +/- hysteresis (E_LK_TMPRT_WIN) ATC_LOCK_COUNTER starts to count up every 8mS.
2) Once temperature data is out of the range, ATC_LOCK_COUNTER is reset.
3) LD temperature is stabilized when ATC_LOCK_COUNTER reaches the settled value (E_LK_CNT_SET),. When this happens, the AK2571 completes the ATC Lock sequence and moves to Status-2.

5.2.4 APC Count up

1) Increment the selected I -DAC value by one step (each 8mS) to prevent abrupt heat increases from affecting ATC.
2) Count up ends when the I-DACx selected by E_APC_CNT_SET (Count up DAC) reaches the target value (E_APC_CNT_CTRL_USER[7:0]).
3) The unselected I-DAC retains the feed forward APC value if the Count up DAC doesn't reach settled value.
4) Although the unselected DAC doesn't reach its feed forward APC (or fixed) value, if count up DAC reaches to the settled value, the AK2571 moves to Status-3

5.2.5 Timer

1) Counts the time from power on reset or release of shut down.
2) If the AK2571 does not reach normal operation within the period set by the settling time register (E_TIMER_SET), , TIMERALM is output.

5.2.6 Normal operation

After theAK2571 has been properly configured and is in "normal" operating mode, continuous temperature compensation is performed every 8 milliseconds using the data in EEPROM.

5.3 Register access mode

Register access mode is used to for adjust the characteristics of the Laser Diode Module. Any characteristics can be adjusted while monitoring by writing to the appropriate register. Please refer to "**8. Registers**" for details.

5.3.1 ATC and APC Adjustment Example

The following adjustment process example is based on the assumption that polarity of ALM, threshold level of ALM, PID, Max current of APC feedback, etc. are already fixed and every parameter is written in the EEPROM continuously.

1) Change the operation mode from self-operation to register access by sending the appropriate command through the Digital interface.
2) Common settings
   2-1) Write zero ("0") to all registers R_CTRL_AKM .to stop the AK2571 working.
   2-2) Select I-DACx for APC by using the R_DAC_SET register.
   2-3) If the temperature corresponding to wave length is known (either exactly or approximately), set the input temperature offset by using the R_ATC_OFFSET register. (Please refer to "4.4 Gain & Offset"). In this process, the target temperature must be set at the midpoint of the ADC (80h).
   2-4) Write 80h to the target temperature register (R_TMPRT_TRGT)
   2-5) Use register R_TEC_CTRL_SET to select a way to control the TEC.. When using Analog control use register R_TEC_ANALOG to select Analog-1 or Analog –2.. If using Digital control, use register lR_TEC_PWM_SET to set the PWM division.
3) ATC adjustment
   3-1) Temperature Adjustment
   When a "1" is written to the R_CTRL_AKM Atc_main(R_CTRL=08h), the ATC begins control of the TEC to meet target the temperature. 10 to 30 seconds are required before the LD temperature is fully stabilized. This time depends on the difference between ambient temperature and target temperature. Stabilization is detected from the ATC Lock completion signal through the STATUS_MON pin moving from Low to High. To detect this signal, E_LK_CNT_SET and E_LK_TMPRT_WIN must be set to the appropriate values, STATUS_MON pin must be set to ATC_LK (R_STATUS_SET=000), and a "1" must be written R_CTRL_AKM.Atc_lk (R_CTRL_AKM=18h) prior to ATC adjustment.
   To complete the ATC adjustment by monitoring the temperature, a preliminary rough adjustment is made using the offset (R_ATC_OFFSET) and secondary fine adjustment using the target temperature register(R_TMPRT_TRGT) should be executed to match the temperature required.

   3-2) Wavelength Adjustment
   It is also possible to adjust the ATC monitoring wavelength. When doing this, the APC be adjusted to work to maintain consistent light power. Writing "1" in R_CTRL_AKM.Apc_main (R_CTRL_AKM=28h) starts APC. Follow the APC adjustment instructions in the next section and roughly set R_DACx_GAIN and R_DACx corresponding to I-DAC for use.
   A preliminary rough adjustment is made using the offset (R_ATC_OFFSET) and secondary fine adjustment using the target temperature register(R_TMPRT_TRGT) should be executed to match the temperature required.

4) APC adjustment

4-1) I-DAC adjustment

a) Adjust R_DACx to set the light power of the LD. Firstly set register R_DACx_GAIN for the full code of I-DAC being over 80h to get sufficient accuracy. But it is need to take the margin for LD aging compensation for the APC Feed back DAC. R_DACx_GAIN of APC Feed back must be limited to remain Feed back compensation current. For example R_DACx must not beyond 80h if aging compensation current is needed by the same amount of initial current. And not beyond C0h if aging compensation current is needed by the half amount of initial current.

b) When using the I-DAC1 dithering function, enable R_EA_SW, set the gain using register R_EA_GAIN and set the frequency using R_EA_FREQ. Monitor the total I-DAC1 current since this dithering current is added to R_DAC1 R_DAC1 must be adjusted with this in mind.

c) If the wavelength moves after the APC adjustment, adjust R_TMPRT_TRGT to match the wavelength or go back and readjust the ATC.

4-2) PDMON Gain setting

Set the PD voltage gain monitoring. The range is from 0.4V to 1.1V / 0.1V step. This setting must be executed after R_PDGAIN is set.

4-3) Initial aging error setting (R_APC_TRGT adjustment)

a) STATUSMON setting: Set R_STATUS_SET = "APC FB". When the aging compensation current is added to the I-DAC output, STATUS_MON becomes High.

b) R_CTRL_USER.Apc_fb = 1 executes the APC Feedback function. In this register access mode, actually the APC Feedback function doesn't add current to the R_DACx to make sure this adjustment.

c) Moving R_APC_TRGT, identify the point at which STATUS_MON becomes High. This is the initial aging set point.

5) APC setting

If there are external components affected by ambient temperature changes (current amplifiers, driver IC etc.), training for cancellation of temperature characteristics is needed. To do this:

5-1) Stabilize the ambient temperature

5-2) Read the R_TV[7:0] (internal T_V converter digital output) through the serial interface.

5-3) Adjust R_DACx to output adequate current at the temperature.

5-4) Store the data 5-2) as address and 5-3) as data in the look-up table.

5-5) Change temperature and repeat this sequence.

6) Set another wavelength

The AK2571 can store the data for four wavelengths in EEPROM. To get the data for another three wavelengths, repeat the sequence from 2) to 5).

Wavelength selection is via pin control.

7) Writing the EEPROM

7-1) Compose the data to write in the EEPROM based on the adjustment above.

7-2) Change the mode to EEPROM mode.

7-3) Write the data in EEPROM through the serial interface.

8) Test

Change to Self-operation mode, and confirm all functions work. If there are problems, repeat steps1 to7 and readjust.

Caution: All the data in registers is reset when the power is removed or when the operating mode is changed.

5.3.2 Confirmation of other functions

1) OPALM confirmation

When the APC adjustments are complete, set R_OPALM_SET.

Gradually decrement the value of R_DACx OPALM is output as a current. Confirm LD light power is settled value or not by monitoring the output of PDMON.

2) Aging Error Compensation confirmation

After APC adjustments are complete, write "1" in R_CTRL.Apc_fb. decrement the value of R_DACx , but don't reduce it too much as OPALM is output. APC Feedback begins to function and will increase the value of R_APC_CMPNST. In this register access mode, APC does not add to R_DACx and the light power of the LD does not increase, actually. Eventually R_APC_CMPNST will equal E_APC_FB_MAX. If E_CUALM_SET is set to an equal value of E_APC_FB_MAX beforehand, CUALM out expresses the increment of aging compensation current.

3) Aging shift of wavelength compensation confirmation

This confirmation can be done with 2) Aging Error Compensation confirmation. R_CTRL.Atc_fb="1" enables the ATC feedback confirmation. Decrement the value of R_DACx, but do not reduce it too much as OPALM is output. APC Feedback begins to function and increases the value of R_APC_CMPNST. According to this value, R_ATC_CMPNST is increased by the E_ATC_FB_SET parameter. R_ATC_CMPNST will eventually equal E_ATC_FB_MAX. If E_WLALM_SET is set equal to E_ATC_FB_MAX and below the value of E_APC_FB_SET or E_ATC_FB_SET beforehand, WLALM output indicates the shift of target temperature.

6. Monitor function

6.1 AMON pin analog monitor

Set R_MON_SET (E_MON_SET) register, and monitor the values in the registers below through MON-DAC. Table 6-1 indicates the registers that can be monitored. Output voltage (Vmon) (typ) is expressed below.

Vmon = (2.1-0.5) / 255*K+0.5 [V] K=the decimal value of the register

Table 6-1 Monitoring Register

R_MON_SET				Monitoring Function	Remarks
0	0	0	0	Fixed voltage	R_MON_DAC_FIX
0	0	0	1	PID control absolute value	R_RID_ABS[12:5]
0	0	1	0	APC feedback value	R_APC_CMPNST[7:0]
0	0	1	1	ATC target value	R_TMPRT_CRNT[7:0]
0	1	0	0	ATC feedback value	R_ATC_CMPNST[7:0]
0	1	0	1	IDAC1 set value	R_DAC1[7:0]
0	1	1	0	IDAC2 set value	R_DAC2[7:0]
0	1	1	1	IDAC3 set value	R_DAC3[7:0]
1	0	0	0	T_V converter output	R_TV[7:0]

6.2 STATUS_MON pin output

Set R_STATUS_MON (E_STATUS_SET), and monitor the status in AK2571 through STATUS_MON pin. Table 6-2 indicates the setting

Table 6-2 STATUS_MON output

E_STATUS_SET[2:0]	STATUS_MON output	Remarks
000	ATC_LOCK ATC Lock count up	0: counting 1: count up
001	APC_END APC Count-up expiring	0: APC Count-up or Count-up disable 1: APC Count-up expiring
010	E_FIX_CTRL Move to normal operation	0: before normal operation (start up) 1: Normal Operation
011	APC_FB APC Feedback working	0: APC Feedback Compensation current=0 1: APC Feedback Compensation current>0
100	ATC_FB ATC Feedback working	0: ATC Feedback target temp. shift=0 1: ATC Feedback target temp. shift>0
101	REG Register access mode	0: Self operation or EEPROM mode 1: Register access mode
110	PID_SIGN PID control direction	0: Heating 1: Cooling
111	APC_COMP APC_COMP output	0: PDIN is higher than target 1: PDIN is lower than target

7. EEPROM

The internal 4k-bits EEPROM is composed of 16-bits*256 addresses. The memory map is shown in Table 7-1. Two MSB bits are set by WAVE0 and 1,. It is possible to change the target temperature via pin strapping if the adjustment data for each wavelength is stored in an EEPROM address.. Table 7-2 indicate the relationship between WAVE0, 1 and the EEPROM addresses. Addresses from [xx111010] to [xx111111], which contain system data, user program area and AKM factory data, are valid regardless of the settings of WAVE0,1.

Table 7-1 EEPROM Memory Map Overview

Address			D15-D8	D7-D0
00	00	0000	E_DAC1_TV[00001] Wavelength-1: I-DAC1temperature compensation value	E_DAC1_TV[00000]
		1111	E_DAC1_TV[11111]	E_DAC1_TV[11110]
	01	0000 1111	E_DAC2_TV Wavelengh-1 I-DAC2 temperature compensation value	
	10	0000 1111	E_DAC3_TV Wavelength-1 I-DAC3 temperature compensation value	
	11	0000 1001	Wavelength-1setting data for each wavelength	
		1010 1111	Common setting data-1	
01	00 11	0000 1001	Wavelength-2 data	
		1010 1111	Common setting data-2	
10	00 11	0000 1001	Wavelength-3 data	
		1010 1111	User program area	
11	00 11	0000 1001	Wavelength-4 data	
		1001 1111	Factory usage by AKM	

Table 7-2 Relation of WAVE0, 1and EEPROM [A7, A6]

WAVE1	WAVE0	Address 2bit from MSB		Remarks
		A7	A6	
0	0	0	0	Wavelength-1
0	1	0	1	Wavelength-2
1	0	1	0	Wavelength-3
1	1	1	1	Wavelength-4

7.2 Data construction

1) Temperature compensation data

Force the temperature compensation current on the output of DAC1-3 using the internal T_V converter. Digital MSB 4-bits of data from the T_V converter becomes the address of EEPROM and 5-bit (R_TV[3]) selects the 8-bits data whether D15-D8 or D7-D0. Table 7-3 indicate the temperature compensation data format.

Table 7-3 Temperature compensation data

		Address			Data	
Name	Function	A7, A6	A5, A4	A3-A0	D15-D8	D7-D0
E_DAC1_TV	I-DAC1 Temperature compensation data	xx	00	0000 | 1111	E_DAC1_TV [00001] | E_DAC1_TV [11111]	E_DAC1_TV [00000] | E_DAC1_TV [11110]
E_DAC2_TV	I-DAC2 Temperature compensation data	xx	01	0000 | 1111	E_DAC2_TV [xxxx1]	E_DAC2_TV [xxxx0]
E_DAC3_TV	I-DAC3 Temperature compensation data	xx	10	0000 | 1111	E_DAC3_TV [xxxx1]	E_DAC3_TV [xxxx0]

(1) Setting data for each wavelength

Table 7-4 and 7-5 indicate the data construction for setting data of each wavelength.
Address is A3 toA0 ([A7:A6] is set by WAVE1, 0 and [A5, A4] is fixed [1,1])
Reg marked "1" indicate the existence of related register.

Table 7-4 setting data of each wavelength

Name	Bit	Function	Reg	A7-A4	A3-A0	Data	Setting
E_PDGAIN	5	PDGAIN set	1	xx11	0000	D4-D0	00000: 0dB 11111: 21.7dB 0.7dB Step, Refer table 3-3
E_PDMON_SET	3	PDMON output voltage set	1		0000	D7-D5	000: 0.4V 111: 1.1V 0.1V Step, Refer table 3-2
E_ATC_OFFSET	6	ATC OFFSET set	1		0000	D15-D8	Refer Table 4-6, 4-7 000000: 0.3V 101000: 1.7V 29.7mV / Step
E_MON_DAC_FIX	8	MON_DAC output fixed value	1		0001	D7-D0	Refer table 6-1
E_DAC1_GAIN	2	I-DAC1 Gain set	1		0010	D1-D0	Refer table 3-5 00: 1, 01: 1/2, 10: 1/4, 11: 1/12
E_DAC2_GAIN	2	I-DAC2 Gain set	1		0010	D3-D2	Refer table 3-6 00: 1, 01: 1/2, 10: 1/4

E_DAC3_GAIN	2	I-DAC3 Gain set	1		0010	D5-D4	Refer table 3-7 00: 1, 01: 1/2, 10: 1/4
E_EA_SW	1	EA ON/OFF set	1		0010	D8	0: OFF, 1: ON
E_EA_GAIN	2	EA Gain set	1		0010	D10-D9	Refer table 3-9 00: 16%, 01: 8% 10: 4%, 11: 2%
E_EA_FREQ	3	EA Frequency set	1		0010	D13-D11	Refer table 3-8 000: 16k, 001: 32k, 010: 64k, 011: 128k, 100: 256k
E_APC_TRGT	7	APC Feedback Reference voltage set	1		0011	D6-D0	0000000: 1.5V 1111111: 2.1V 4.8mV/Step, Refer Table 3-4
E_APC_FB_MAX	8	APC Feedback limit current set			0011	D15-D8	
E_DAC1_FIX	8	I-DAC1Fixed current set	2		0100	D7-D0	
E_DAC2_FIX	8	I-DAC2 Fixed current set	2		0100	D15-D8	
E_DAC3_FIX	8	I-DAC3 Fixed current set	2		0101	D7-D0	
E_ATC_FB_MAX	8	ATC Feedback target shift limit set			0110	D7-D0	
E_ATC_FB_SET	4	Parameter set for LD compensation current to target temperature			0110	D11-D8	0000: 0.125, 0001: 0.25 0010: 0.375, 0011: 0.5 0100: 0.625, 0101: 0.75 0110: 1.0, 0111: 1.125 1000: 1.25, 1001: 1.5
E_ATC_TRGT	8	ATC target temperature set	2		0111	D7-D0	0.03°C/LSB
E_TMPRT_ALM_WIN	8	TEMPALM set			0111	D15-D8	
E_CUALM_SET	8	CUALM set			1000	D7-D0	
E_WL_ALM_SET	8	WLALM (target temperature shift ALM) set			1000	D15-D8	

Table 6-5 Data and address construction for each wavelength

Address	Data															
A3-A0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0000			E_ATC_OFFSET[5:0]						E_PDMON_SET[2:0]			E_PDGAIN[4:0]				
0001									E_MON_DAC_FIX[7:0]							
0010			E_EA_								E_DACi_GAIN					
			FREQ			GAIN		SW			DAC3		DAC2		DAC1	
0011	E_APC_FB_MAX[7:0]									E_APC_TRGT [6:0]						
0100	E_DAC2_FIX[7:0]								E_DAC1_FIX[7:0]							
0101									E_DAC3_FIX[7:0]							
0110					E_ATC_FB_SET[3:0]				E_ATC_FB_MAX[7:0]							
0111	E_TMPRTALM_WIN[7:0]								E_ATC_TRGT[7:0]							
1000	E_WLALM_SET[7:0]								E_CUALM_SET[7:0]							
1001	Reserved															

(2) Common setting data

Table 7-6 and 7-7 show common data settings in the EEPROM. Registers marked "1" indicate the existence of a related register.

Table 7-6 Common setting data construction

				Address			
Name	Bits	Function	Reg	A7,A6	A5, A4	A3-A0	Setting
E_TEC_ANALOG	1	TEC Analog way select	1	00	11	1010	0: Analog-1way 1: Analog-2way
E_PID_PWM	2	PWM division set	1			1010	00: Not divide 01: 32, 10:64, 11:128
E_PID_CTRL	1	Analog / PWM set	1			1010	0: Analog control 1: PWM control
E_DAC_SET	3	I-DAC set	1			1010	0: Disable 1: Enable [0]: I-DAC1 [1]: I-DAC2 [2]: I-DAC3
E_APC_FF_SET	1	APC Feed forward set	1			1011	0: fixed current 1: compensation
E_APC_FB_SET	3	APC Feedback data add I-DAC selection	1			1011	0: not addition 1: addition [0]: I-DAC1 [1]: I-DAC2 [2]: I-DAC3
E_APC_CNT_SET	2	APC Count-up finalize I-DAC select	1			1011	00: I-DAC1 01: I-DAC2 10: I-DAC3 11: Disable
E_TV_OFFSET	5	Internal T_V conv.	1			1100	Refer Table 3-10

		OFFSET adjustment					Adjusted by AKM
E_MON_SET	4	MON-DAC output set	1			1101	Refer table 6-1
E_STATUS_SET	3	STATUS MON output set	1			1101	Refer table 6-2
E_ALM_SHUTDW	2	ALM output set	1			1110	0x: ALM enable 10: Fix not active polarity 11: Fix active polarity
E_ALM_POL	1	ALM polarity set	1			1110	0: ALM detect "H" 1: ALM detect "L"
E_OPALM_SET	3	OPALM threshold set	1			1110	000: 1/2, 001: 1/3 010: 1/4, 011: 1/5 100: 1/6, 101: 1/8
E_TIMER_SET	2	TIMER ALM count period set	1			1111	00: 8s, 01: 16s 10: 32s, 11: 64s
E_INI_CTRL_USR	8	Start up sequence set	2	01	11	1010	Refer 5.2.2
E_APC_CNT_CTRL_USR	8	APC Count-up operation set	2			1010	Refer 5.2.2
E_FIX_CTRL_USR	8	Normal operation set	2			1011	Refer 5.2.2
E_LK_TMPRT_WIN	8	Window set for ATC Lock window				1100	0.03 °C/LSB
E_LK_CNT_SET	2	ATC Lock period set				1100	00: 2s, 01: 4s, 10: 8s, 11: 16s
E_PID_D	8	PID differential parameter				1101	Refer Table 4-3
E_PID_P	8	PID proportion parameter set				1101	Refer Table 4-3
E_PID_I	8	PID integration parameter set				1101	Refer Table 4-3
E_PID_MAX	6	PID control maximum value set				1101	6bits MSB of PID absolute control value (13bits)
E_PIDALM_SET	8	PIDALM set				1111	8bits MSB of PID absolute control value (13bit)
E_PID_INACT_SET	8	PID not sense window set				1111	8bits LSB of PID absolute control value (13bits)
USER program area	96			10	11	1010 | 1111	
AKM adjust area	96	Start up sequence operation set		11	11	1010 | 1111	Don't touch the data.

Table 7-7 Common data addresses

Address			Data															
[7:6]	[5:4]	[3:0]	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	11	1010						E_DAC_SET[2:0]							Ctrl	PWM[1:0]		Ana
		1011											CNT_SET		APC_FB_SET			FF
		1100												E_TV_OFFSET[4:0]				
		1101										E_STATUS_SET			E_MON_SET[3:0]			
		1110						E_OPALM_SET								POL	ALM_SH	
		1111															TIMER_SET	
01	11	1010	E_APC_CNT_CTRL_USR[7:0]								E_INI_CTRL_USR[7:0]							
		1011									E_FIX_CTRL_USR[7:0]							
		1100							E_LK_CNT_SET		E_LK_TMPRT_WIN[7:0]							
		1101	E_PID_P[7:0]								E_PID_D[7:0]							
		1110			E_PID_MAX[5:0]						E_PID_I[7:0]							
		1111	E_PID_INACT_SET[7:0]								E_PIDALM_SET[7:0]							

8 Register

Table 8-1 and 8-2 show register contents and formats.

The EEP column indicates:

1: existence of same function in EEPROM

2: existence of related function in EEPROM.

Table 8-1 Construction of Registers

Register Name	Bits	Function	EEP	Address A5-A0	Setting
R_PDGAIN[4:0]	5	PDGAIN Set	1	000000	00000: 0dB 11111: 21.7dB 0.7dB Step, refer table3-3
R_PDMON_SET[7:5]	3	PDMON output voltage set	1	000000	000: 0.4V 111: 1.1V 0.1V Step, refer table 3-2
R_ATC_OFFSET[13:8]	6	ATC OFFSET set	1	000000	Refer table 4-6, 4-7 000000: 0.3V 101000: 1.7V 29.7mV / Step
R_MON_DAC_FIX[7:0]	8	MON_DAC fixed value set	1	000001	Refer table 6-1
R_DAC1_GAIN[1:0]	2	I-DAC1 Gain set	1	000010	Refer table 3-5 00: 1, 01: 1/2, 10: 1/4, 11: 1/12
R_DAC2_GAIN[3:2]	2	I-DAC2 Gain set	1	000010	Refer table 3-6 00: 1, 01: 1/2, 10: 1/4
R_DAC3_GAIN[5:4]	2	I-DAC3 Gain set	1	000010	Refer table 3-7 00: 1, 01: 1/2, 10: 1/4
R_EA_SW[8]	1	EA ON/OFF set	1	000010	0: OFF, 1: ON
R_EA_GAIN[10:9]	2	EA Gain set	1	000010	Refer table 3-9

					00: 16%, 01: 8% 10: 4%, 11: 2%
R_EA_FREQ[13:11]	3	EA frequency set	1	000010	Refer table 3-8 000: 16k, 001: 32k, 010: 64k, 011: 128k, 100: 256k
R_APC_TRGT[6:0]	7	APC Feedback Reference voltage set	1	000011	0000000: 1.5V 1111111: 2.1V 4.8mV/step, refer table3-4
R_TEC_ANALOG[0]	1	TEC Analog control select	1	000100	0: Analog-1way 1: Analog-2way
R_PID_PWM[2:1]	2	PWM division set	1	000100	00: not divide 01: 32, 10:64, 11:128
R_PID_CTRL[5:4]	1	Analog / PWM select	1	000100	0: Analog way 1: PWM way
R_DAC_SET[10:8]	3	I-DAC enable	1	000100	0: disable 1: enable [0]: I-DAC1 [1]: I-DAC2 [2]: I-DAC3
R_APC_FF_SET[0]	1	APC Feed forward select	1	000101	0: fixed value 1: compensation data
R_APC_FB_SET[3:1]	3	APC Feedback added I-DAC select	1	000101	0: not addition 1: addition [0]: I-DAC1 [1]: I-DAC2 [2]: I-DAC3
R_APC_CNT_SET[5:4]	2	APC Count-up finalize I-DAC select	1	000101	00: I-DAC1 01: I-DAC2 10: I-DAC3 11: disable
R_TV_OFFSET[4:0]	5	Internal T_V conv. Offset adjustment	1	000110	Refer table 3-10 AKM factory usage
R_MON_SET[3:0]	4	MON-DAC output set	1	000111	Refer table 6-1
R_STATUS_SET[6:4]	3	STATUS MON output set	1	000111	Refer table 6-2
R_ALM_SHUTDW[1:0]	2	ALM output set	1	001000	0x: ALM enable 10: Fix not active polarity 11: Fix active polarity
R_ALM_POL[2]	1	ALM output polarity set	1	001000	0: ALM detect "H" 1: ALM detect "L"
E_OPALM_SET[10:8]	3	OPALM threshold set	1	001000	000: 1/2, 001: 1/3 010: 1/4, 011: 1/5 100: 1/6, 101: 1/8
R_TIMER_SET[1:0]	2	TIMER ALM count period set	1	001001	00: 8s, 01: 16s 10: 32s, 11: 64s
R_TMPRT_TRGT[7:0]	8	ATC target temperature set	2	001010	E_ATC_TRGT – R_ATC_CMPNST
R_CTRL_USR[7:0]	8	Control register set	2	001011	Refer 5.2.2
R_DAC1[7:0]	8	I-DAC1 set	2	001100	
R_DAC2[7:0]	8	I-DAC2 set	2	001101	

R_DAC3[7:0]	8	I-DAC3 set	2	001110	
R_STATUS[7:0]	8	Status register		010000	
R_ALM_ST[3:0]	4			010001	
R_TMPRT_CRNT[7:0]	8	Theremistor temperature data		010010	
R_TV[7:0]	8	Internal T_V conv. Temperature data		010011	
R_APC_CMPNST[7:0]	8	LD aging error current		010100	
R_ATC_CMPNST[7:0]	8	Target temperature shift value		010101	
R_MON_DAC[7:0]	8	Monitor DAC set		010110	
R_PDMOND[7:0]	8	PDMON output digital value		010111	
R_PID_INTGRL[7:0]	8	PID Integration value (under decimal)		011000	
R_PID_INTGRL[13:0]	14	PID Integration value (integral number 2's)		011001	
R_PID_VALABS[14:0]	15	PID control value		011010	
R_CTRL_AKM[7:0]	8	Control register	2	111011	

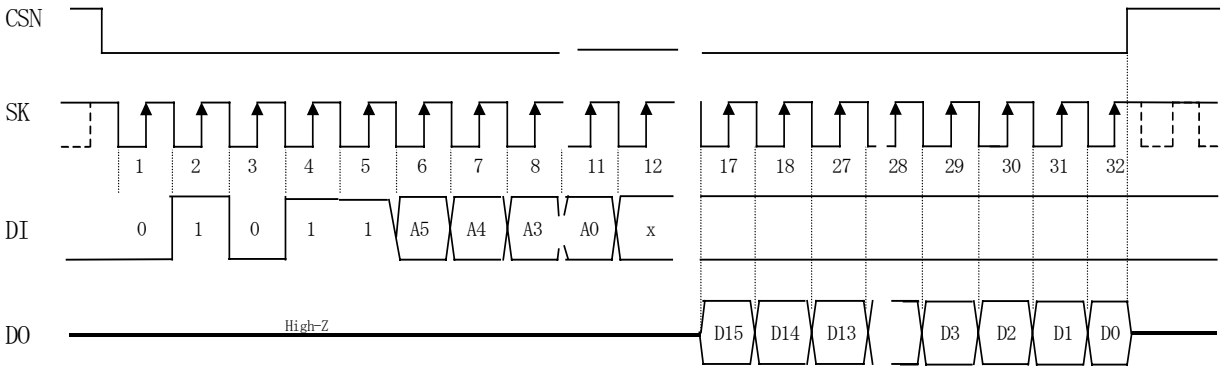
Table 8-2 Register Map

Address		Data																R/W
[5:4]	[3:0]	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
00	0000	R_ATC_OFFSET[5:0]								R_PDMON_SET[2:0]			R_PDGAIN[4:0]					R/W
	0001	R_MON_DAC_FIX[7:0]																R/W
	0010	R_EA_										R_DACi_GAIN						R/W
		FREQ					GAIN		SW			DAC3		DAC2		DAC1		
	0011	R_APC_TRGT [6:0]																R/W
	0100	R_DAC_SET[2:0]												Ctrl	PWM[1:0]		Ana	R/W
	0101	R_CNT_SET												APC_FB_SET			FF	R/W
	0110	R_TV_OFFSET[4:0]																R/W
	0111	R_STATUS_SET												R_MON_SET[3:0]				R/W
	1000	R_OPALM_SET													POL	ALM_SH		R/W
	1001	R_TIMER_SET																R/W
	1010	R_TMPRT_TRGT[7:0]																R/W
	1011	R_CTRL_USR[7:0]																R/W
	1100	R_DAC1[7:0]																R/W
	1101	R_DAC2[7:0]																R/W
	1110	R_DAC3[7:0]																R/W
	1111																	
01	0000	R_STATUS[7:0]																R
	0001	R_ALM_ST[3:0]																R
	0010	R_TMPRT_CRNT[7:0]																R
	0011	R_TV[7:0]																R
	0100	R_APC_CMPNST[7:0]																R
	0101	R_ATC_CMPNST[7:0]																R
	0110	R_MON_DAC[7:0]																R
	0111	R_PDMOND[7:0]																R
	1000	R_PID_INTGRL[7:0]																R
	1001	R_PID_INTGRL[21:8]																R
	1010	R_PID_VALABS[14:0]																R
11	1011	R_CTRL_AKM[7:0]																R/W

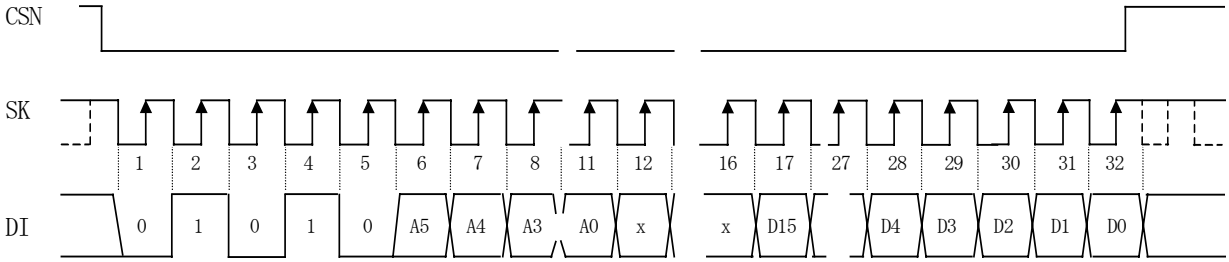
1. Digital I/F

CSN must be set for each instruction. It cannot be used continuously.
Digital I/F can connect directly to a SPI interface In this case, set (CPOL, CPHA) = (0, 0) or (1, 1).
(CPOL, CPHA) = (0, 0) : Status output through DO pin
(CPOL, CPHA) = (1, 1) : Status output disable

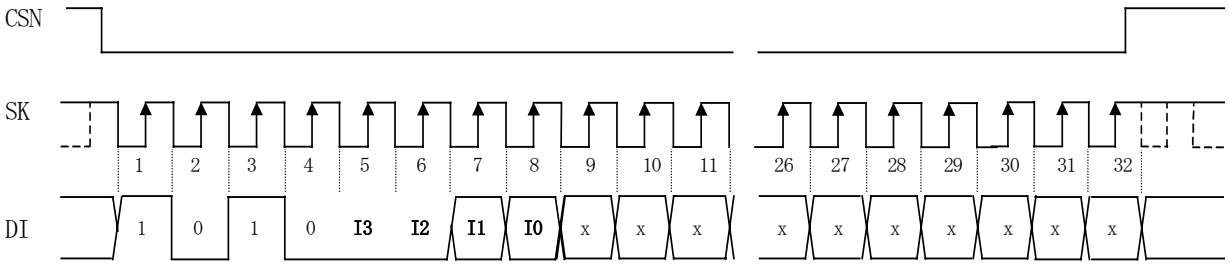
1.1 Register access [READ] mode (RDREG)



1.2 Register access [WRITE] mode (WRREG)

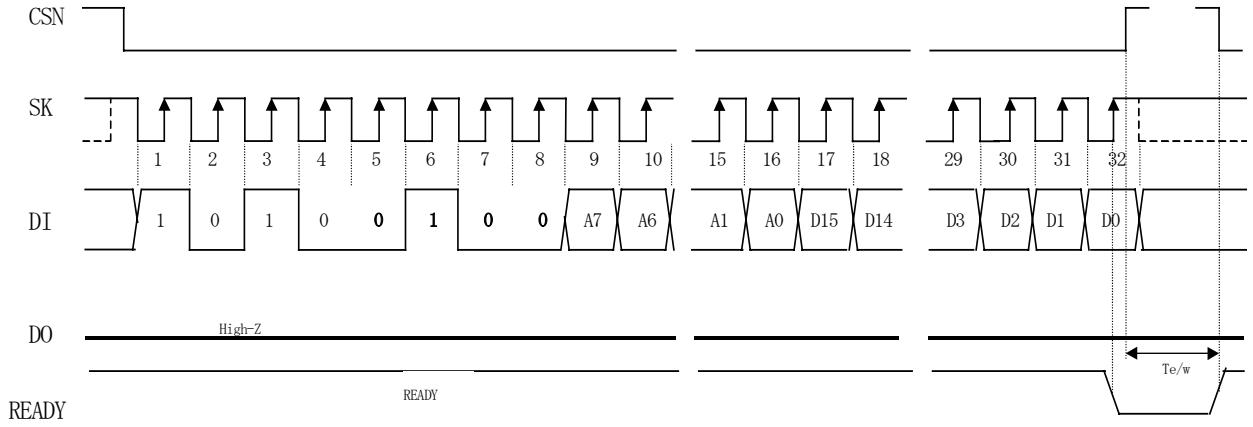


1.3 EEPROM access mode (WRDS、WREN command)

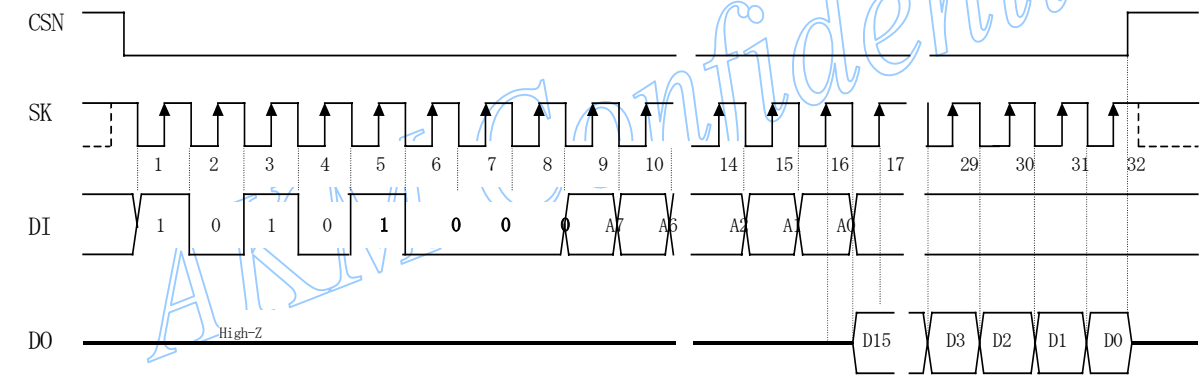


I3	I2	I1	I0	
0	0	0	0	: WRDS
0	0	1	1	: WREN

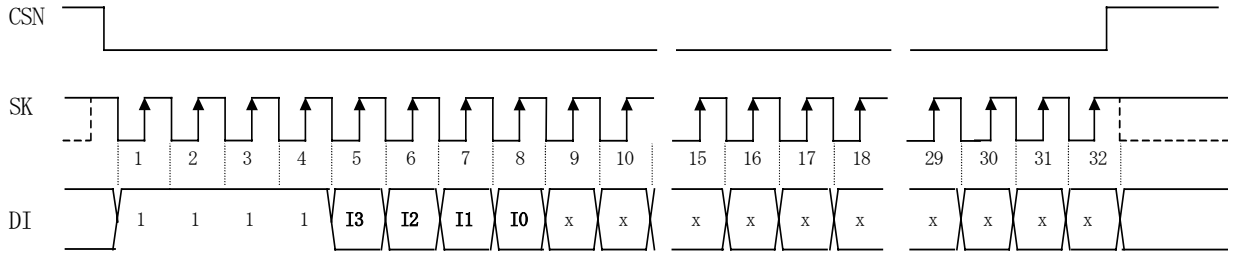
1.4 EEPROM access [WRITE] mode (WRITE)



1.5 EEPROM access [READ] mode (READ)



1.6 Move operation mode



I3	I2	I1	I0		
0	0	0	0	:	Self operation (NORMAL)
0	1	1	1	:	Register access (REGMODE)
1	1	1	0	:	EEPROM mode (EEPMODE)

2. Shut Down

2.1 Reset through RESETN pin

RESEN= "0" make same function of internal Power-On-Reset.
After its release, AK2571 begins to start up sequence same as Power ON.

2.2 Shut down control through SHUT_ATCN pin

SHUT_ATCN="0" make AK2571 all power down.
After its release, AK2571 start from reset.

2.3 Shut down control through SHUT_APCN pin

SHUT_APCN="0" make AK2571 only APC shut down which stop the current output through I-DAC1-3. After its release, AK2571 start to work by the data before shut down soon.

Electric Characteristics

(1) Absolute maximum rating

Parameter	Symbol	Min	typ	max	Unite	Remarks
Voltage supply (AVDD, L1DD, L2VDD, L3VDD, TVDD, DVDD)	VDD	-0.3	-	6.5	V	VDD=all VDD
Grand level (AVSS, BVSS, LVSS, TVSS, DVSS, DAVSS)	GND	0	-	0	V	GND=all VSS =all GND
Input voltage (Beside VDDs)	VIN	GND-0.3	-	VDD+0.3	V	
Input current (Beside VDDs)	IIN	-10	-	10	mA	
Storage temperature	Tstg	-55	-	130	°C	

(2) Recommended operating conditions

All specifications are regulated under this condition

Parameter	Symbol	Min	Typ	Max	Unite	Remarks
Voltage supply	VDD	3.1	3.3	3.5	V	3.3V+/-6%
Ambient Operating Temperature	Ta1	-20	-	+85	°C	Package version
	Ta2	+5	-	+50	°C	ATC Target temperature *)
Die surface temperature	Ta3	-20	-	+115	°C	Die version

*) Target temperature range for ATC. Not tested but design target value.

(3) Current consumption

Parameter	Symbol	Min	Typ	Max	Unite	Remarks
Current consumption (all VDD pin)	IDD	-	TBD		mA	1) 2)

*1) Exclude external load

*2) Setting code of I-DACx(x=1,2,3) is (00)、IDAC4 is h (000), all gain setting are default (Gain=" 1 ").

(4) EEPROM Characteristics

Parameter	min	max	Unite	Condition
EEPROM Re-write	10000	-	Times	*1)
EEPROM data retention	10	-	Year	at 85°C

*1) means total re-write times tolerance: All memory cells are rewrite even though only one address is re-written. In that sense average tolerance is 39 times (Total address: 256 address = 4 wavelength x 64 Address and 10000/256=39 times).

(5) Digital Input / Output DC characteristics

Parameter	Symbol	min	typ	max	Unite	Condition
High level input voltage	VIH	0.7VDD	-	-	V	
Low level input voltage	VIL	-	-	0.3VDD	V	
High level output voltage	VOH	0.9VDD	-	-	V	IOH= -0.2mA
Low level output voltage	VOL	-	-	0.4	V	IOL= 0.2mA

(6) Digital Input / Output AC characteristics (Beside Serial Interface)

Parameter	Pin	Symbol	min	typ	max	Unite	Remarks
Reset pulse width	RESETN	Tpwr	200	-	-	ns	Refer figure 1

Note) Duty Cycle : (Tpwh／(Tpwh＋Tpwl)) ×100 %

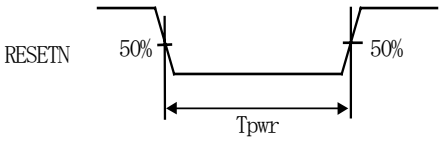


Figure 1 Reset pulse width

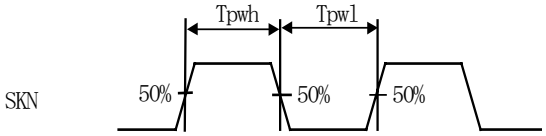


Figure 2 Input Clock Duty Cycle

(7) Digital Input / Output AC characteristics (Serial Interface)

Parameter	Pin	Symbol	min	typ	max	Unite	Remarks
SK interval	SK	Tskp	1	-	-	μs	Refer figure 3
SK Duty Cycle	SK		40	50	60	%	Refer figure 2
CSN setup time before SK fall	CSN SK	Tcss	100	-	-	ns	Refer figure 3 *1)
CSN hold time after SK rise	CSN SK	Tcsh	100	-	-	ns	Refer figure 4
SK setup time before CSN fall	CSN SK	Tsksl	100			ns	Refer figure 6
Input clock and data setup / hold time	SK DI	Tdis Tdih	200	-	-	ns	Refer figure 3, 5
SK fall to DO output latency	SK DO READY	Tpd	-	-	300	ns	Refer figure 4,6 CL=50pF
Programming time		Te/w	10	-	-	ms	Refer figure 5 *2)
CSN high level hold time after raise READY	READY CSN	Trch	100			ns	Refer figure 5 *2)
CSN high level to DO output latency	CSN DO	Toz			100	ns	Refer figure 4,6

*1) SK must be high when CSN transitions to Low.

*2) When writing in EEPROM

It is forbidden to read or write continuously by keeping CSN low.

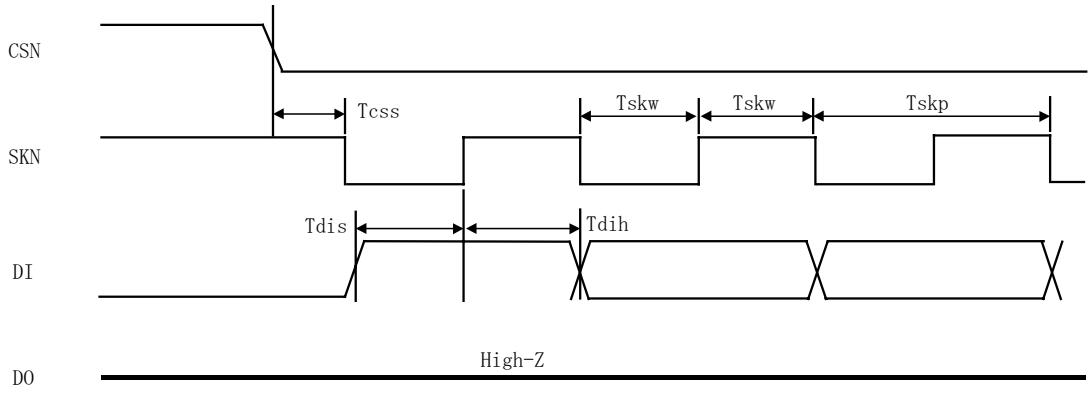


Figure 3: input command timing

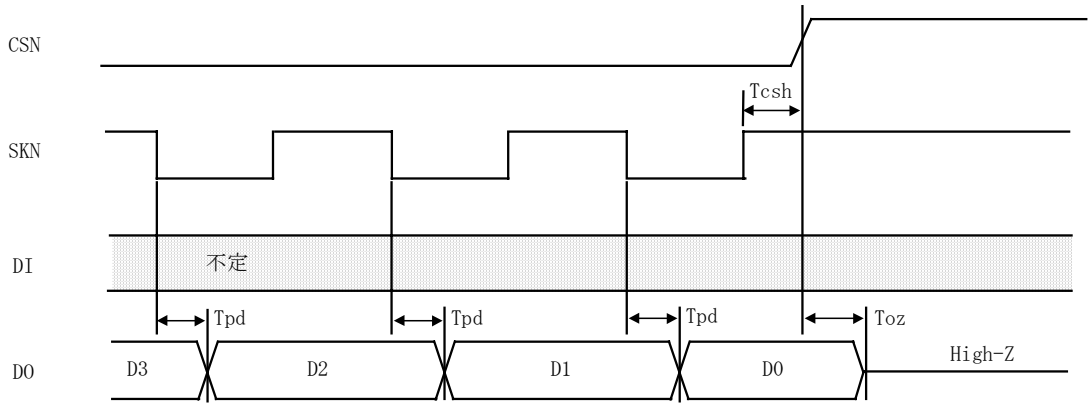


Figure 4: data output timing

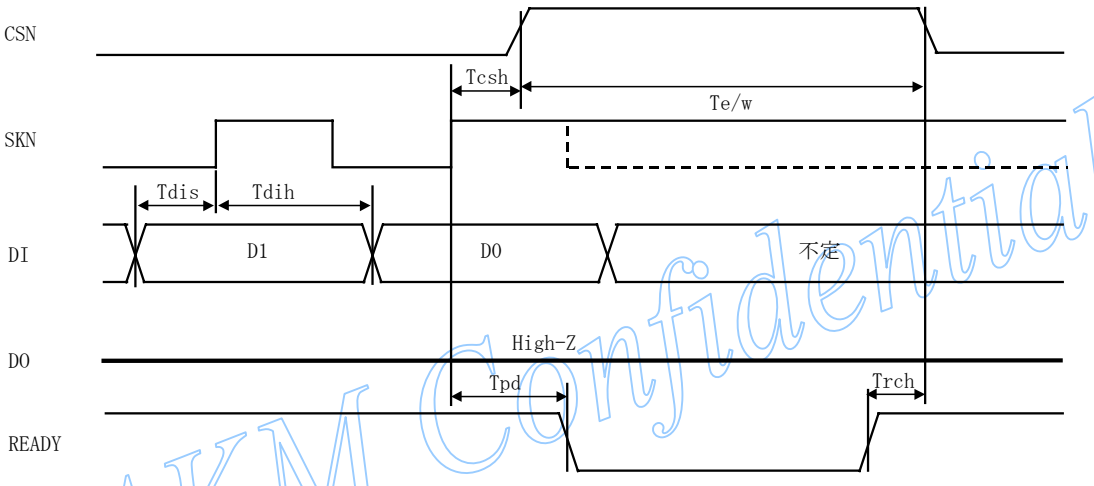


Figure 5: EEPROM write timing

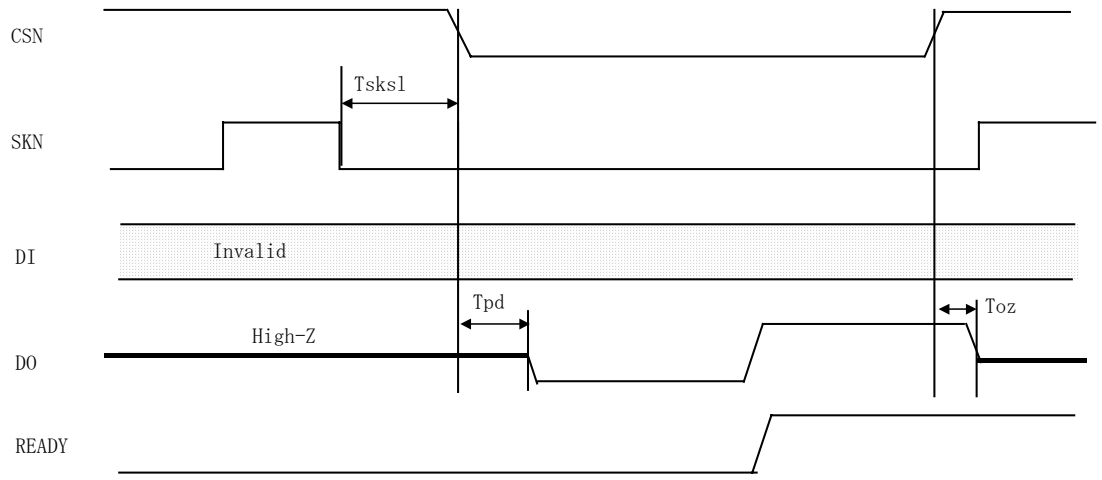


Figure 6: status output through DO pin

* Status output

Monitoring DO pin, indicates the status of READY.

After the WRITE command is executed, SK is fixed Low and CSN moves from High to Low, DO pin changes to status output mode and outputs a READY signal.

The READY signal through DO pin stops if CSN turns High or the first bit ("1") of the next command is input. When the next command is input, CSN must be set high once.

(8) ADC* (Time sharing) A to D converter Input / Output characteristics

Parameter	Condition	min	typ	max	Unite	Remark
Resolution			8		Bit	
DNL		-1		1	LSB	
INL		-2		2	LSB	
Step (=1LSB)			8.63		mV/step	
Input voltage range	Peak voltage	0.0		2.2	V	Design target
Output digital code		D[7:0] (00)h-(FF)h (straight binary) 0.0V - 2.2V				Design target

(9) MON_DAC characteristics

Parameter	Condition	Min	Typ	max	Unite	Remark
Resolution			8		Bit	
DNL	*1)	-1		1	LSB	
INL	*1)	−2		2	LSB	
Step (=1LSB)	*1)		6.27		mV/step	Remark
Output voltage range	Peak voltage	0.5		2.1	V	Design target *2)
Input digital code		D[7:0] (00)h-(FF)h(straight binary) 0.5V - 2.1V				

*1) AMON output voltage

*2) Center voltage of Output "Vmon" is indicated by the expression below, if DAC code = "K".

Vmon = (2.1 - 0.5) / 255 * K + 0.5 [V]

(10) DAC_APC characteristics

Parameter	Condition	min	Typ	max	Unite	Remark
Resolution			7		bit	
DNL		-1		1	LSB	
INL		-2		2	LSB	
Step (=1LSB)			4.8		mV/step	
Output voltage range	Peak voltage	1.5		2.1	V	Design target *1)
Output digital code		D[6:0] (00)h-(7F)h (straight binary) 1.5V ～ 2.1V				

*1) Center voltage of Output "Vapc" is indicated by the expression below, if DAC code = "K".

Vapc = (2.1 – 1.5) / 127 * K + 1.5 [V]

(11) IDAC 1 characteristics

Parameter	Condition	min	typ	max	Unite	Remark
Resolution			8		bit	
INL		-2		+2	LSB	
Maximum output current		109.6	121.8	134.0	mA	±10% *1)*4)
Minimum output current			30		mA	*2)*4)
Step (=1LSB)			0.353		mA/step	*3)*4)
Output voltage				1.8	V	*5)
DNL		-1		+1	LSB	
Input digital code		D[7:0] (00)h - (FF)h (straight binary)				

*1) at maximum (FF)h setting, gain is 1.

*2) at minimum (00)h setting, gain is 1.

*3) output current "Iidac1" is indicated by the expression below, if gain is "G", DAC setting code is "K".

Iidac1 = **(maximum output current – minimum output current)** / 255 * G * K + **minimum output current** [mA]

*4) maximum output current, minimum output current and resolution can be set by register.

E_DAC1_GAIN [1:0]	Gain	Minimum output current (Design target)	Maximum output current (Design target)	Resolution (Design target)	Remarks
00	1	30mA	121.8mA	0.36mA/step	Default
01	1/2	15mA	60.9mA	0.18mA/step	
10	1/4	7.5mA	30.45mA	0.09mA/step	
11	1/12	2.5mA	10.15mA	0.03mA/step	

*5) Construct external circuit to ensure the voltage of IOUT1 doesn't exceed this value. If it is over, output current can't be guaranteed.

(12) EA_MOD characteristics

Dithering current by EA_MOD function is added to current of I-DAC1and output through IOUT1pin. Output current through I-DAC1 shifts if this function is enabled by the register R_EA_SW(E_EA_SW).

(1) Dithering Frequency

The dither frequency is selected through register (EEPROM) R_(E_) EA_FREQ, and is derived by dividing the OSC 2.048MHz(typ) clock.

R_EA_FREQ (E_EA_FREQ) [2:0]	Division	Dithering Frequency (Design target)			Remarks
		min	Typ	max	
000	1/128		16kHz		Default
001	1/64		32kHz		
010	1/32		64kHz		
011	1/16		128kHz		
100	1/8		256kHz		

(2) Dithering current gain

R_EA_GAIN (E_EA_GAIN) [1:0]	Dithering current gain (Design target)			Remarks
	min	typ	max	
00		16%		Default
01		8%		
10		4%		
11		2%		

(13) IDAC2, IDAC3 characteristics

Parameter	Condition	Min	typ	max	Unite	Remarks
Resolution			8		bit	
INL		-2		+2	LSB	
Maximum output current		19.28	21.42	23.56	mA	±10% *1)*5)
Minimum output current			2.68		mA	*2)*5)
Step (=1LSB)			0.084		mA/step	*3)*5)
Output voltage				1.8	V	*4)
DNL		-1		+1	LSB	
Input digital code		D[7:0] (00)h - (FF)h (straight binary)				

*1) at maximum (FF)h setting, gain is 1.

*2) at minimum (20)h setting, gain is 1. Linearity from (00)h to (20)h is not guaranteed.

*3) output current "Iidac23" is indicated by the expression below, if gain is "G", DAC setting code is "K".

Iidac23 = (21.42 / 255) * G * K [mA]

*4) Construct external circuit to ensure the voltage of IOUT2 doesn't exceed this value. If it is over, output current can't be guaranteed and APC operations may not work correctly.

*5) The register below sets the maximum output current, minimum output current and resolution. . Their performance is regulated from a register value of (20)h. When the register value is below 20h, linearity is not guaranteed.

E_DAC2_GAIN E_DAC3_GAIN [1:0]	Gain	Minimum output current (Design target)	Maximum output current (Design target)	Resolution (Design target)	Remarks
00	1	0mA	21.42mA	0.084mA/step	Default
01	1/2	0mA	10.71mA	0.042mA/step	
10	1/4	0mA	5.36mA	0.021mA/step	

(14) IDAC4 characteristics

Parameter	Condition	Min	Typ	Max	Unite	Remarks
Resolution			10		bit	
Maximum output current		45.58	50.64	55.70	mA	±10% *1)
Minimum output current			3.2		mA	*2)
Step (=1LSB)			0.050		mA/step	*3)
Output voltage				1.8	V	*4)
DNL		-2		+2	LSB	
Input digital code		D[9:0] 3FF - 000 (straight binary)				

*1) Current at maximum setting (3FF)h .

*2) current of minimum setting (20)h.

Linearity from (00)h to (40)h is not guaranteed. However (00)h setting, will set an internal switch and force the output to 0V.

*3) output current "Iidac4" as indicated by the expression below, if DAC4 setting code is "K".

Iidac4= (50.64/255)*K [mA]

*4) Construct an external circuit to ensure that the IOUT4 voltage does not exceed this value. If this value is exceeded, output current cannot be guaranteed and .APC operation may not function properly.

(15) Shut down characteristics

Parameter	Conditions	min	typ	max	Unite	Remark
SHUTDOWN setup time	Time from SHUT_APCN/SHUT_ATCN = "L" to output of IDACx(1,2,3) become Hi-Z and IDAC4 becomes OFF.			10	μs	
SHUTDOWN release time	Time from SHUT_APCN = "H" to IDACx(1,2,3) output settled current.			500	μs	Only for SHUT_APCN *1)

*1) SHUT DOWN release time is regulated in SHUT_APCN.

(16) T_V conversion characteristics

Parameter	Condition	min	typ	max	Unite	Remark
T_V Conv. gain	Offset adjustment		-0.7		°C/step	±5% Design target

Regulated by the digital data after A-to-D conversion. Its offset is adjusted by AKM in testing.

(17) Other Input / Output range characteristics

Parameter	Conditions	min	typ	max	Unite	Remarks
PD input range for Monitoring	PDIN pin	0.2		1.5	V	Design target
PD monitor output range	PDMON pin PDIN voltage Gained by POMON/PDGAIN	0.4		1.1	V	*1) 0.1V/step Design target
Thermister input voltage range	TEMPIN pin	0.4		1.5	V	Design target
Regulator voltage for thermister	REFOUT pin		2.3		V	±5% Design target

*1) PDIN voltage is user programmable by register setting(Refer 3.3.1) in the range of 0.4 to1.1V by 0.1V/step.

(18) Internal oscillator (OSC) characteristics (AKM adjust in testing)

Parameter	Condition	Min	typ	max	Unite	Remark
Frequency	Adjusted by AKM in testing		2.048		MHz	±20%

Pin / Function

Pin#	Pin name	Function	Note
1	TEST1	AKM Test pin. Connect to GND .	
2	IOUT4H	I-DAC4 output(50mA max).TEC control (Heating)	
3	NC	NC pin. Connect to GND.	
4	IOUT4C	I-DAC4 output (50mA max). TEC control (Cooling)	
5	NC	NC pin. Connect to GND.	
6	IOUT3	I-DAC3 output (20mA max). LD drive	
7	L2VDD	Voltage supply for I-DAC2 and 3	
8	IOUT2	I-DAC2 output (20mA max). LD drive	
9	LVSS	I-DAC GND	
10	NC	NC pin. Connect to GND.	
11	NC	NC pin. Connect to GND.	
12	IOUT1	I-DAC1 output (120mA max). LD drive	
13 14	WAVE1 WAVE0	Wavelength select. Switch EEPROM space.	
15	SHUT_APCN	Shut down APC. "L" = Shut down.	
16	SHUT_ATCN	Shut down ATC and APC. "L" = Shut down.	
17	RESETN	Reset input. "L"= reset	
18 19	TSK TDI	AKM Test pin. Connect to GND in ordinary	
20	L1VDD	Voltage supply for I-DAC1	
21	NC	NC pin. Connect to GND.	
22	PDIN	Monitors PD voltage input. PD current is averaged by the external resistor and capacitor input.	
23	PDMON	Output gained thermister voltage	
24	TESTA	AKM Test pin. Connect to GND in ordinary	
25	TEMPIN	Input voltage from the thermister; divided by an external resistor.	
26	REFOUT	Supply reference voltage for the thermister.	
27	AVDD	Voltage supply for analog circuit.	
28	NC	NC pin. Connect to GND.	
29	AVSS	GND for analog circuit.	
30	BIAS	Set the internal BIAS currents. Connect 12kΩ±1% to GND.	
31	AMON	Outputs analog monitor signals through the DAC. Internal digital signal monitoring by analog.	
32	NC	NC pin. Connect to GND.	
33	CSN	Chip select	
34	NC	NC pin. Connect to GND.	
35	READY	Output = "L" when writing to the EEPROM .	
36	DO	Data output	
37	NC	NC pin. Connect to GND.	
38	DI	Data input	
39	SK	Serial clock input	
40	DAVSS	GND for digital substrate. Connect to GND.	
41	DVDD	Voltage supply for digital circuit	
42	NC	NC pin. Connect to GND.	

43	DVSS	GND for digital circuit	
44	EEP	"H" output when the AK2571 is in EEPROM mode.	
45	STATUS_MON	Monitors the AK2571 status.	
46	TIMERALM	Timer ALM. Outputs an alarm if the AK2571 doesn't enter normal operating mode within the settling period.	
47	OPALM	Loss of power. Outputs an alarm if the voltage from PDIN is below the threshold.	
48	CUALM	Compensation current over alarm. Outputs an alarm if the compensation current for aging is over the threshold.	
49	TEMPALM	Temperature alarm. Output alarm if voltage of TEMPIN is over the threshold.	
50	PIDALM	PID control ALM. Output alarm if current for TEC control is over the threshold.	
51	WLALM	Target temperature shift alarm. Output alarm if the value of target temperature shift is over the threshold.	
52	NC	NC pin. Connect to GND.	
53	COOLP	P-CH FET control signal for TEC. PID control directs for cooling, it becomes Low.	
54	HEATN	N-CH FET control signal for TEC. PID control directs for heating, it becomes High. PWM way selected as TEC control, switch corresponding to PID control value and PWM division value.	
55	NC	NC pin. Connect to GND.	
56	TVSS	GND for P-CH/N-CH control signal	
57	TVDD	GND for P-CH/N-CH control signal	
58	NC	NC pin. Connect to GND.	
59	COOLN	N-CH FET control signal for TEC. PID control directs for cooling, it becomes High. PWM way selected as TEC control, switch corresponding to PID control value and PWM division value.	
60	HEATP	P-CH FET control signal for TEC. PID control directs for heating, it becomes Low.	
61	BVSS	GND for substrate	
62	L3VDD	Voltage supply for I-DAC4	
63	NC	NC pin. Connect to GND.	
64	TEST2	AKM Test pin. Connect to GND in ordinary usage.	

Package Conditions

1) Package : 64-LQFP

2) Marking

a.1pin indicate: Marked ○ is 1pin

b. AKM trademark: AKM

c. AKM marking: AK2571

d. Date code: YYWWXXX

YY: Year

WW: Week(1～52)

XXX : LOT code