



STN2NE10L

N-channel 100V - 0.33Ω - 2A - SOT-223
STripFET™ Power MOSFET

General features

Type	V _{DSS} (@T _{jmax})	R _{DS(on)}	I _D
STN2NE10L	100V	<0.4Ω	1.8A

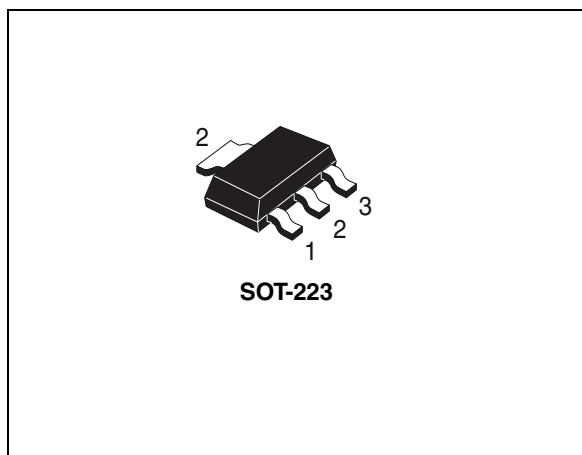
- Exceptional dv/dt capability
- Avalanche rugged technology
- 100% avalanche tested
- Low threshold drive

Description

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Applications

- Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STN2NE10L	N2NE10L	SOT-223	Tape & reel

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	100	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	1.8	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	1.3	A
$I_{DM}^{(1)}$	Drain current (pulsed)	7.2	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	2.5	W
	Derating factor	0.02	W/°C
$dv/dt^{(2)}$	Peak diode recovery voltage slope	6	V/ns
T_J	Operating junction temperature	150	°C
T_{stg}	Storage temperature	-65 to 150	°C

1. Pulse width limited by safe operating area

2. $I_{SD} \leq 7.2$ A, $di/dt \leq 200$ A/ μ s, $V_{DD} \leq (BR)DSS$, $T_J \leq T_{JMAX}$

Table 2. Thermal data

$R_{thj-pcb}$	Thermal resistance junction-PC Board max	50	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	60	°C/W
T_l	Maximum lead temperature for soldering purpose	260	°C

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J Max)	1.8	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25^\circ\text{C}$, $I_d = I_{AR}$, $V_{dd} = 25\text{V}$)	20	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	100			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating} @ 125^{\circ}C$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20V$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1	1.7	3	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 1A$ $V_{GS} = 5V, I_D = 1A$		0.33 0.38	0.4 0.45	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max},$ $I_D = 1A$	1	3		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		345 45 20		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 80V, I_D = 7A$ $V_{GS} = 5V$ (see Figure 13)		10 5 4	14	nC nC nC

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time rise time	$V_{DD} = 50 V, I_D = 3.5A,$ $R_G = 4.7 \Omega, V_{GS} = 5V$ (see Figure 14)		7 17		ns ns
$t_{d(off)}$ t_f	Turn-off-delay time fall time	$V_{DD} = 50 V, I_D = 3.5A,$ $R_G = 4.7 \Omega, V_{GS} = 5V$ (see Figure 14)		22 8		ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD} = 80 V, I_D = 7A,$ $R_G = 4.7 \Omega, V_{GS} = 5V$ (see Figure 14)		8 9 19		ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current				2	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				8	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=2A, V_{GS}=0$			1.5	V
t_{rr}	Reverse recovery time	$I_{SD}=7 A,$ $di/dt = 100A/\mu s,$ $V_{DD}=30 V, T_j=150^\circ C$		75		ns
Q_{rr}	Reverse recovery charge			190		nC
I_{RRM}	Reverse recovery current			5		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

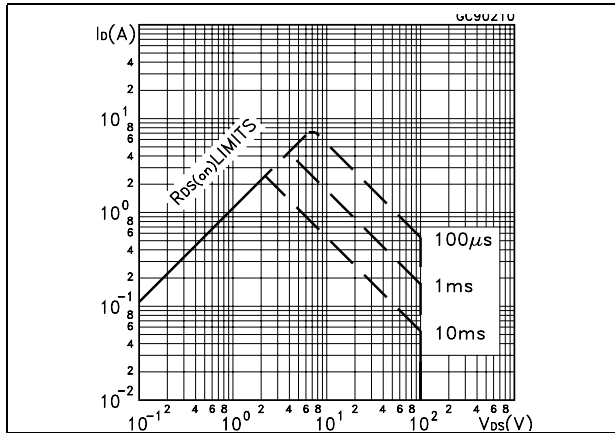


Figure 2. Thermal impedance

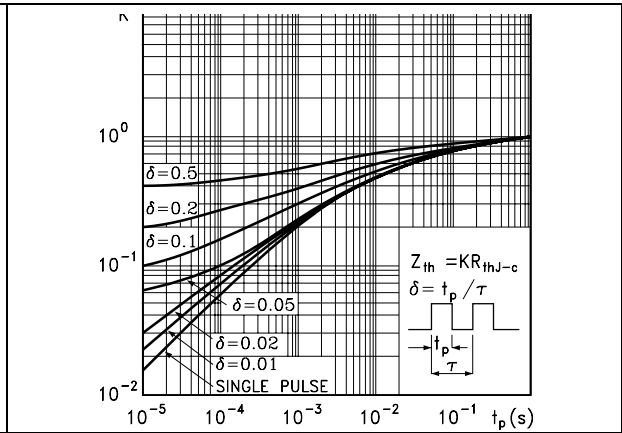


Figure 3. Output characteristics

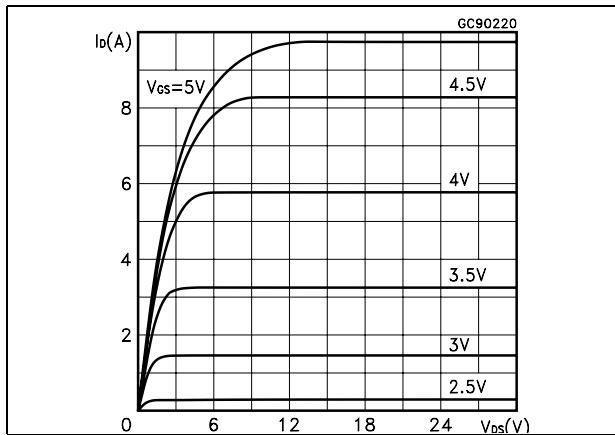


Figure 4. Transfer characteristics

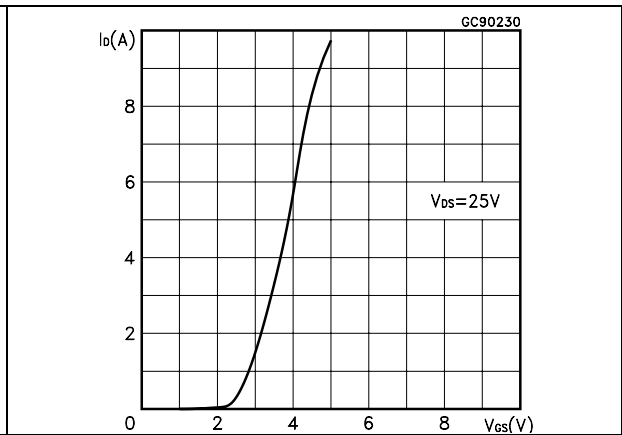


Figure 5. Transconductance

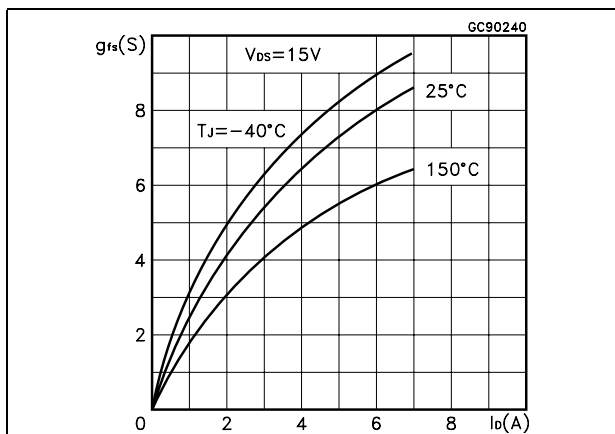


Figure 6. Static drain-source on resistance

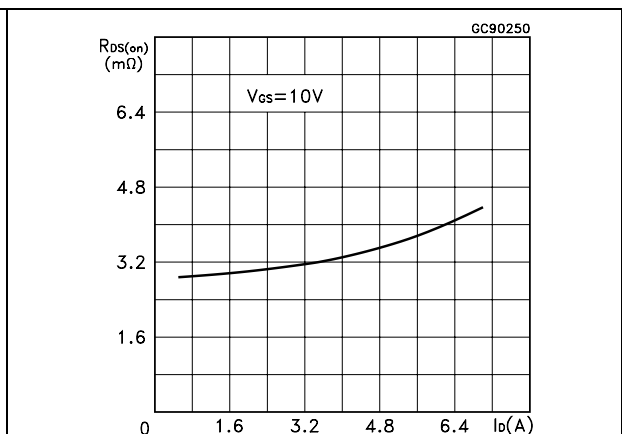


Figure 7. Gate charge vs. gate-source voltage Figure 8. Capacitance variations

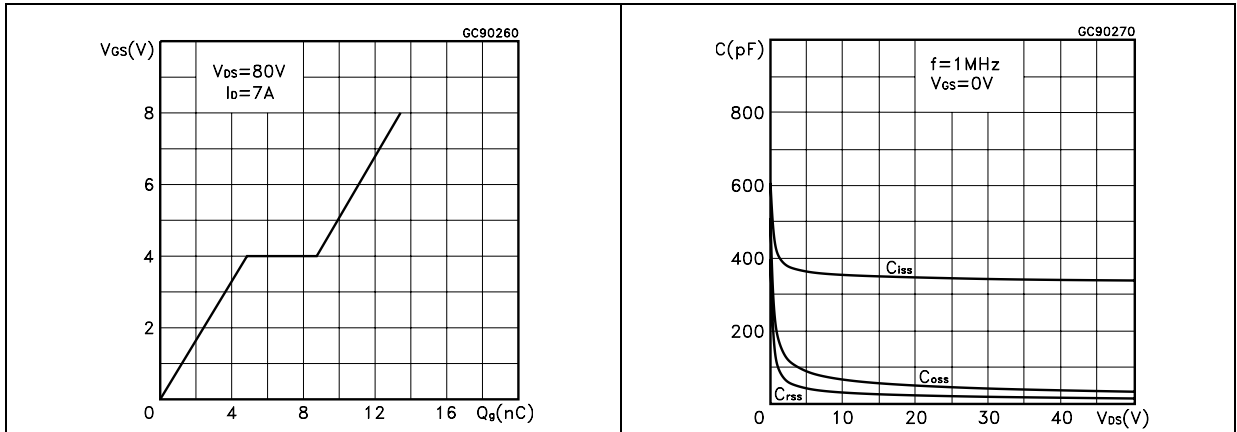


Figure 9. Normalized gate threshold voltage vs. temperature Figure 10. Normalized on resistance vs. temperature

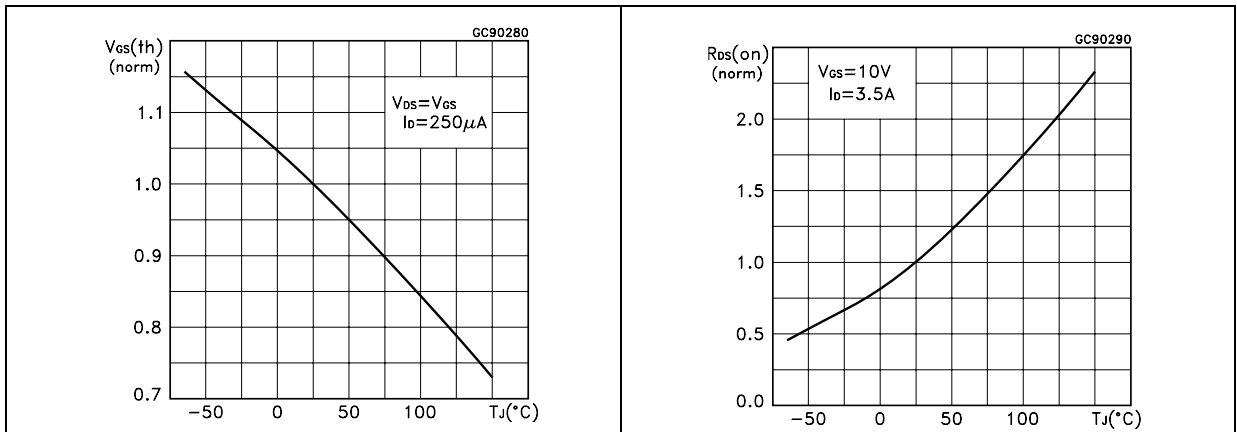
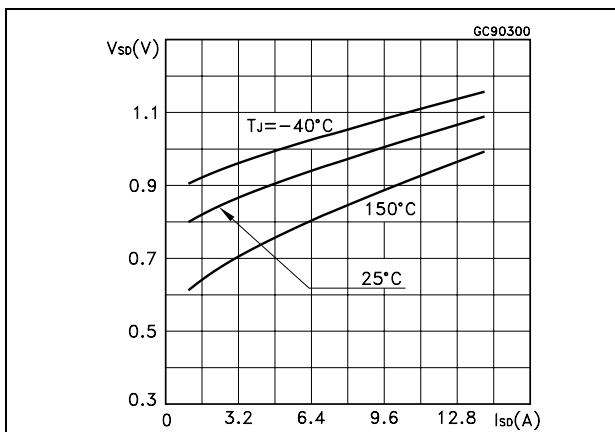


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load

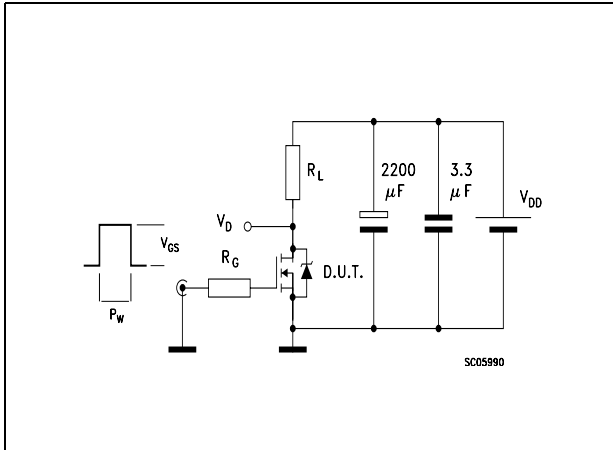


Figure 13. Gate charge test circuit

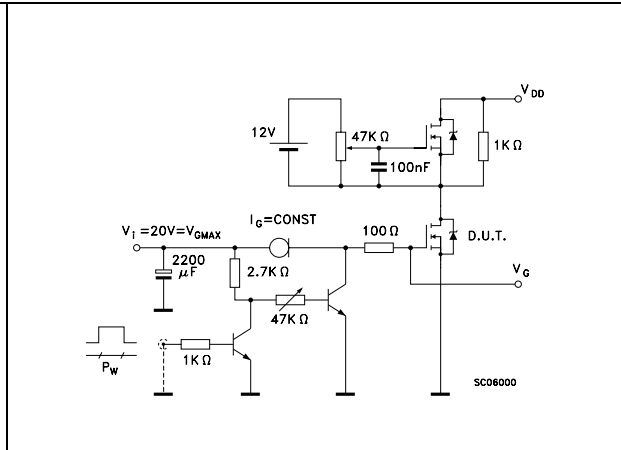


Figure 14. Test circuit for inductive load switching and diode recovery times

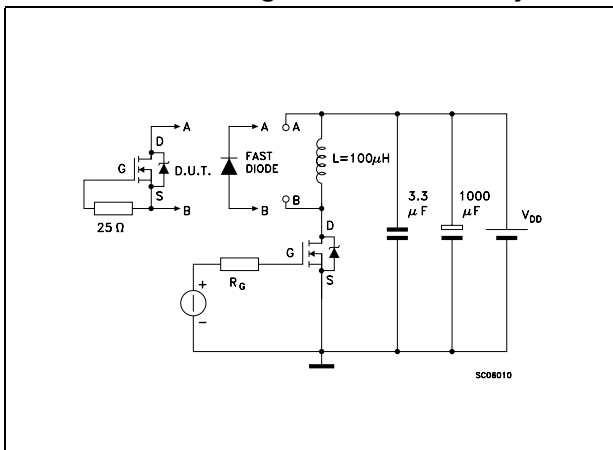


Figure 15. Unclamped Inductive load test circuit

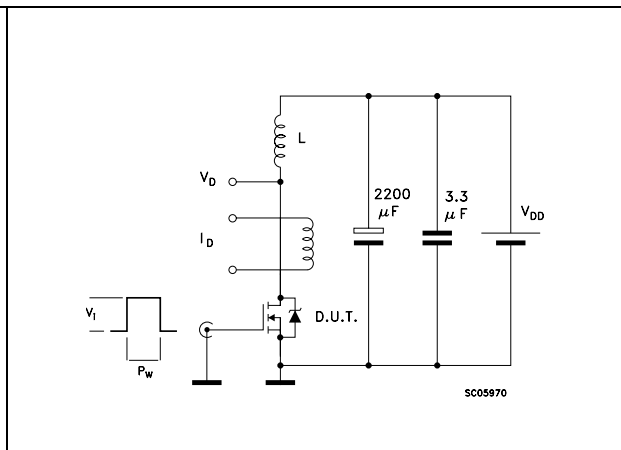


Figure 16. Unclamped inductive waveform

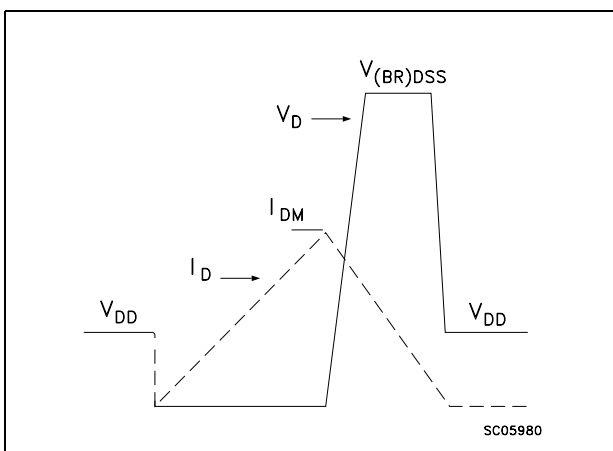
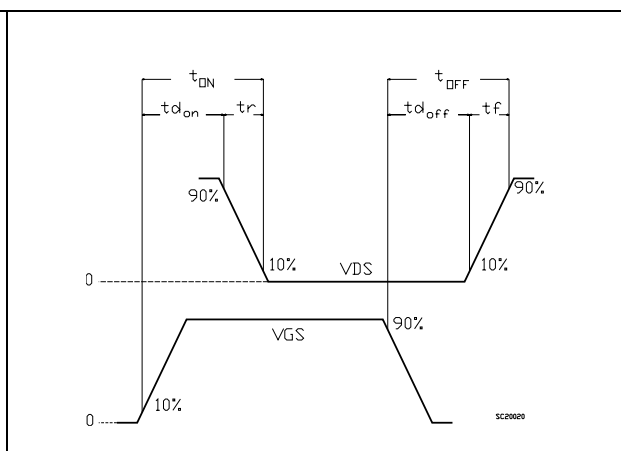


Figure 17. Switching time waveform

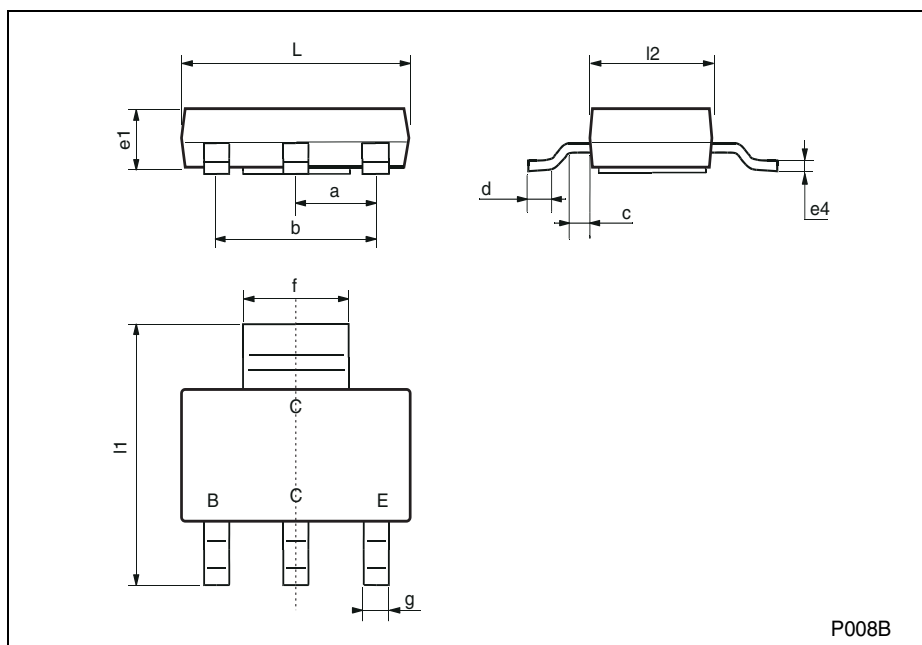


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

SOT-223 MECHANICAL DATA

DIM.	mm			mils		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a	2.27	2.3	2.33	89.4	90.6	91.7
b	4.57	4.6	4.63	179.9	181.1	182.3
c	0.2	0.4	0.6	7.9	15.7	23.6
d	0.63	0.65	0.67	24.8	25.6	26.4
e1	1.5	1.6	1.7	59.1	63	66.9
e4			0.32			12.6
f	2.9	3	3.1	114.2	118.1	122.1
g	0.67	0.7	0.73	26.4	27.6	28.7
l1	6.7	7	7.3	263.8	275.6	287.4
l2	3.5	3.5	3.7	137.8	137.8	145.7
L	6.3	6.5	6.7	248	255.9	263.8



5 Revision history

Table 8. Revision history

Date	Revision	Changes
19-Oct-2005	2	Preliminary datasheet
05-March-2006	3	Modified value on Table 4
19-Sep-2006	4	New template, no content change
01-Feb-2007	5	Typo mistake on Table 1 .

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