Discontinued Product

Preliminary

OKI Semiconductor

This version: Jan. 1998
Previous version: Mar. 1996

MSM64169

Built-in Dual-slope type A/D Converter and LCD Driver 4-Bit Microcontroller

GENERAL DESCRIPTION

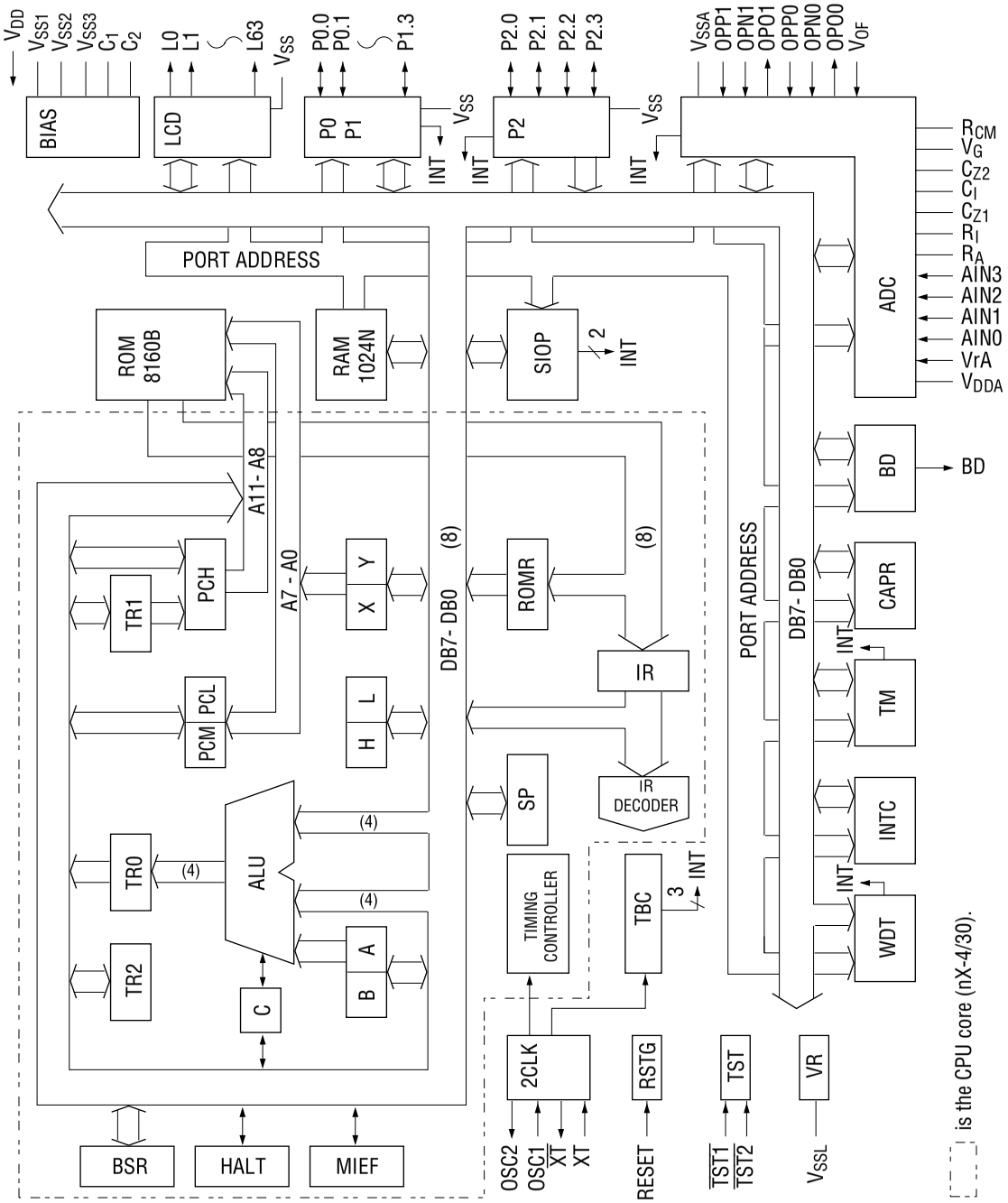
The MSM64169 is a low-power 4-bit microcontroller that incorporates OKI's nX-4/30 CPU core. The MSM64169 has a minimum instruction execution time of 4.3 µs (@ 700 kHz). The device contains 8160 bytes of program memory, a 1024-nibble data memory, a dual-slopetype A/D converter with a 4-channel input, LCD drivers that can drive up to 240 segments, a synchronous/asynchronous selectable serial port, a 16-bit timer, and a buzzer output port.
Applications include high resolution thermometers with low power consumption, barometers, and hygrometers.

FEATURES

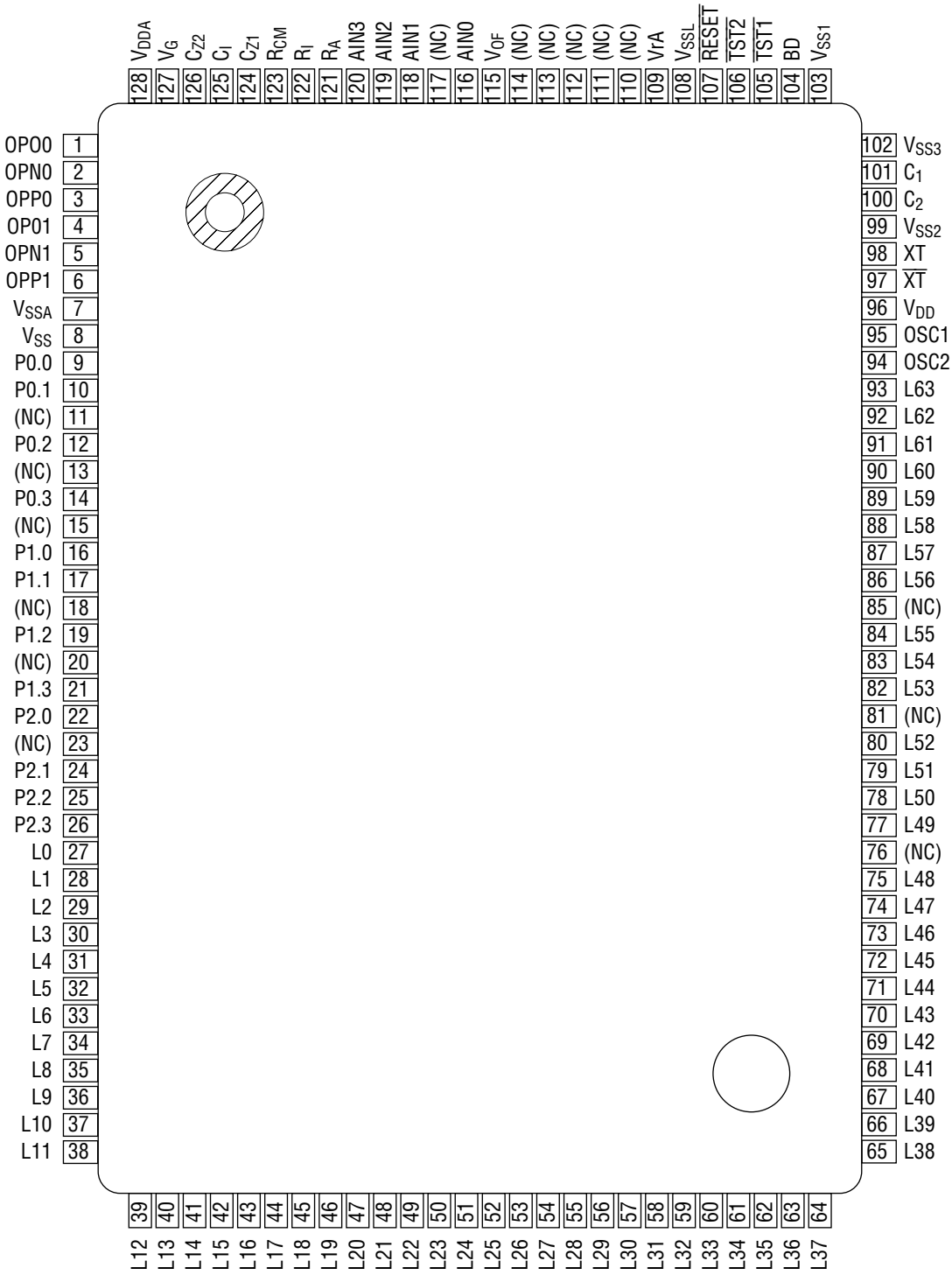
- Operating range
  - Operating frequencies (dual clock) : 32 kHz, 700 kHz
  - Operating voltage : 2.6 V to 3.6 V
  - Operating temperature : –40°C to +85°C
- Memory space
  - Internal program memory : 8160 bytes
  - Internal data memory : 1024 nibbles
- Minimum instruction execution time : 4.3 µs (@ 700 kHz)
  91.6 µs (@ 32.768 kHz)
- Dual-slope type A/D converter : 1; 4-channel input
- LCD drivers : 64; duty ratio switchable by software
  - (1) At 1/4 duty, 1/3 bias : 240 segments (max.)
  - (2) At 1/3 duty, 1/3 bias : 183 segments (max.)
  - (3) At 1/2 duty, 1/2 bias : 124 segments (max.)
- Buzzer driver : 1; four modes for controlling buzzer output ON/OFF
- Timer : 16-bit × 1
  - Auto-reload mode
  - Capture mode
  - Clock frequency measuring mode
- Watchdog timer
- Clock : 32.768 kHz quartz oscillator and 700 kHz RC oscillator (with an external resistor)
  - CPU clock : 32.768 kHz/700 kHz (selectable by software)
  - Time base clock : 32.768 kHz
- Power supply voltage : 3 V low power
- I/O port : 3 ports × 4 bits
- Output only port : 2 ports × 4 bits (8 out of 64 LCD drivers can be used as output-only ports via mask programming)
- Serial port : Synchronous/asynchronous mode support
  - Synchronous mode : 32.768 kHz/external clock
  - Asynchronous mode : 9600 bps/4800 bps/2400 bps/1200 bps
- Interrupts : 10 sources (2 external, 8 internal)

- Capture circuit : 2 channels
- Package:
  - 128-pin plastic QFP (QFP128-P-1420-0.50-K) : (Product name: MSM64169-xxxGS-K)
  - Chip : (Product name: MSM64169-xxx)
    xxx indicates the code number.
- OTP version (under development) : (Product name: MSM64P169)
  Note: The MSM64P169 is diffrent from the MSM64169 in the polarity of the power supply voltage and the operating voltage.Refer to the MSM64P169 user's manual for details.

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC: No-connection pin

128-Pin Plastic QFP

PIN DESCRIPTIONS

Basic Functions

Function	Pin	Pad	Symbol	Type	Description
Power Supply	96	86	V_{DD}	—	0V power supply
	103	93	V_{SS1}	—	Bias output for LCD drive (–1.5V)
	99	89	V_{SS2}	—	Negative power supply: bias output for LCD drive (–3.0V)
	102	92	V_{SS3}	—	Bias output for LCD drive (–4.5V)
	8	7	V_{SS}	—	Negative power supply for input/output port interface
	101	91	C_1	—	Capacitor connection for LCD-drive bias generation
	100	90	C_2	—	
	108	98	V_{SSL}	—	Negative power supply pin for internal logic (internally generated constant voltage)
	7	6	V_{SSA}	—	Negative power supply for A/D converter: externally connects to V_{SS2}.
	128	112	V_{DDA}	—	0V power supply for A/D converter: externally connects to V_{DD}.
Oscillation	98	88	XT	I	Low speed clock oscillation input pin: connects to the crystal oscillator (32.768kHz).
	97	87	$\overline{XT}$	O	
	95	85	OSC1	I	High speed clock pins: connects to the oscillation resistor (R_{OS}).
	94	84	OSC2	O	
Test	105	95	$\overline{TST1}$	I	Input pins for test: pulled up to V_{DD} internally.
	106	96	$\overline{TST2}$	I	
Reset	107	97	$\overline{RESET}$	I	System reset input: when this pin is asserted to "H" after being pulled to "L", the microcontroller's internal state is initialized and instruction execution starts from address 000H. This pin is pulled up to V_{DD} internally.

Basic Functions (Continued)

Function	Pin	Pad	Symbol	Type	Description
Ports	9	8	P0.0	I/O	4-bit I/O port (P0): each bit can be configured to be an input/output, pull-up/pull-down resistor input/high impedance input, or NMOS open drain output/CMOS output by port 0 control registers 0-3 (P00CON-P03CON). An external interrupt function is assigned to each pin.
	10	9	P0.1	I/O	
	12	10	P0.2	I/O	
	14	11	P0.3	I/O	
	16	12	P1.0	I/O	4-bit I/O port (P1): each bit can be configured to be an input/output, pull-up/pull-down resistor input/high impedance input, or NMOS open drain output/CMOS output by port 1 control registers 0-3 (P10CON-P13CON). An external interrupt function is assigned to each pin.
	17	13	P1.1	I/O	
	19	14	P1.2	I/O	
	21	15	P1.3	I/O	
	22	16	P2.0	I/O	4-bit I/O port (P2): each bit can be configured to be an input/output, pull-up/pull-down resistor input/high impedance input, or NMOS open drain output/CMOS output by port 2 control registers 0-3 (P20CON-P23CON). An external interrupt function is assigned to each pin.
	24	17	P2.1	I/O	
	25	18	P2.2	I/O	
	26	19	P2.3	I/O	
Buzzer	104	94	BD	O	Output pin of buzzer driver
A/D Converter	116	101	AIN0	I/O	Analog voltage input pins. Each of these pins can be switched to provide a constant current output by AD control register 0 (ADCON0).
	118	102	AIN1	I/O	
	119	103	AIN2	I/O	
	120	104	AIN3	I/O	
	121	105	R_A	—	Current-adjusting resistor connection pin
	122	106	R_I	—	Pin for connecting resistor for integration
	123	107	R_{CM}	—	Common connection pin for resistor for integration, capacitor 1 for offset compensation, and capacitor for integration.
	124	108	C_{Z1}	—	Pin for connecting capacitor 1 for offset compensation
	125	109	C_I	—	Pin for connecting capacitor for integration
	126	110	C_{Z2}	—	Pin for connecting capacitor 2 for offset compensation
	127	111	V_G	—	
	109	99	VrA	I	Reference voltage for A/D conversion (internally generated constant voltage)
	115	100	V_{OF}	I	Pin for connecting resistor for voltage amplification circuit offset adjustment
	3	2	OPP0	I	Analog micro-voltage input pin
	6	5	OPP1	I	
	2	1	OPN0	I	Pin for connecting resistor for voltage amplification factor adjustment
	5	4	OPN1	I	
	1	113	OPO0	O	
	4	3	OPO1	O	

Basic Functions (Continued)

Function	Pin	Pad	Symbol	Type	Description
LCD Drivers	27	20	L0/P3.0	O	LCD segment/common signal output pins. These pins can also be mask-programmed to provide an output port.
	28	21	L1/P3.1	O	
	29	22	L2/P3.2	O	
	30	23	L3/P3.3	O	
	31	24	L4/P4.0	O	
	32	25	L5/P4.1	O	
	33	26	L6/P4.2	O	
	34	27	L7/P4.3	O	
	35	28	L8	O	LCD segment/common signal output pins
	36	29	L9	O	
	37	30	L10	O	
	38	31	L11	O	
	39	32	L12	O	
	40	33	L13	O	
	41	34	L14	O	
	42	35	L15	O	
	43	36	L16	O	
	44	37	L17	O	
	45	38	L18	O	
	46	39	L19	O	
	47	40	L20	O	
	48	41	L21	O	
	49	42	L22	O	
	50	43	L23	O	
	51	44	L24	O	
	52	45	L25	O	
	53	46	L26	O	
	54	47	L27	O	
	55	48	L28	O	
	56	49	L29	O	
	57	50	L30	O	

Basic Functions (Continued)

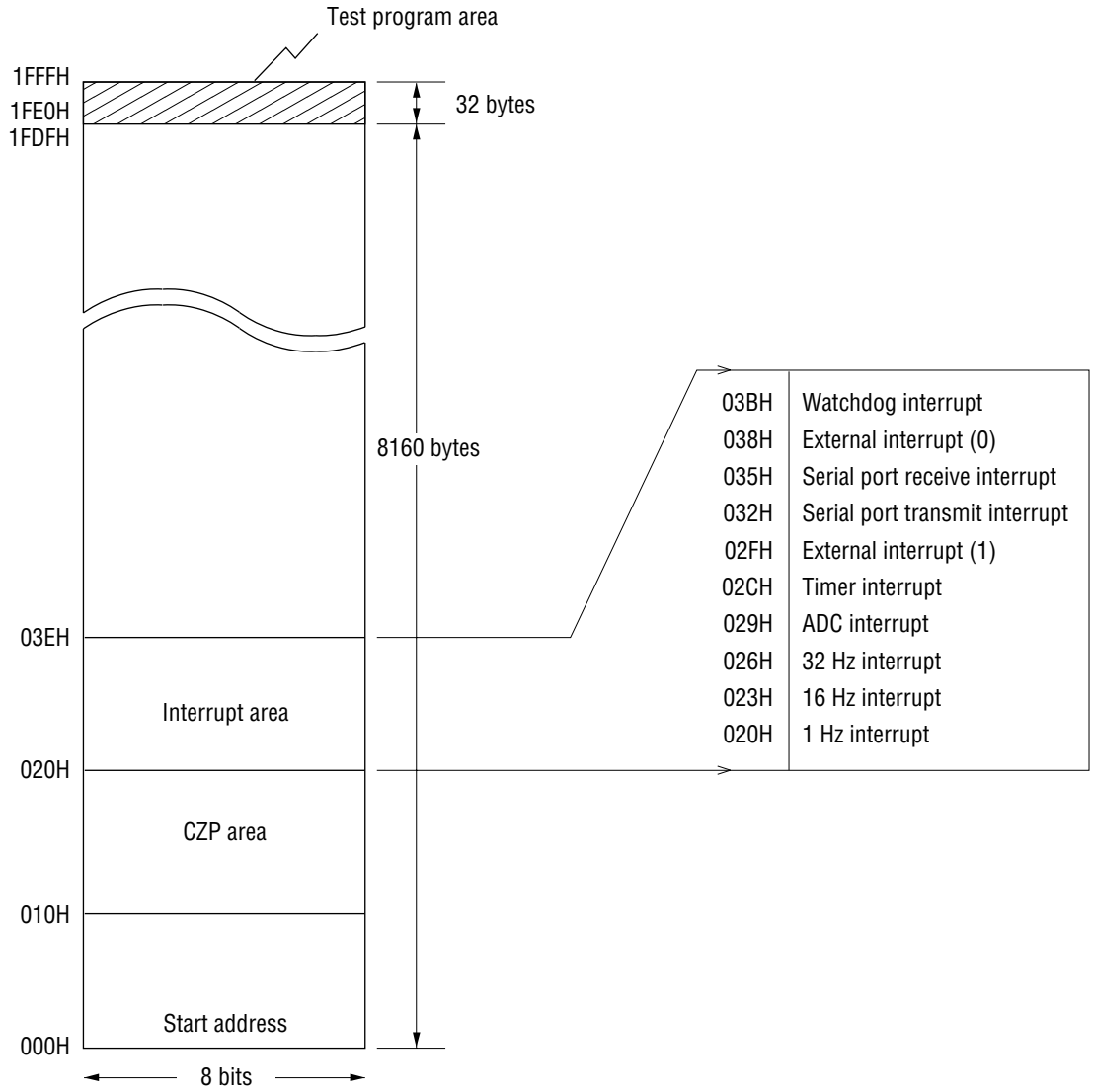
Function	Pin	Pad	Symbol	Type	Description
LCD Drivers	58	51	L31	O	LCD segment/common signal output pins
	59	52	L32	O	
	60	53	L33	O	
	61	54	L34	O	
	62	55	L35	O	
	63	56	L36	O	
	64	57	L37	O	
	65	58	L38	O	
	66	59	L39	O	
	67	60	L40	O	
	68	61	L41	O	
	69	62	L42	O	
	70	63	L43	O	
	71	64	L44	O	
	72	65	L45	O	
	73	66	L46	O	
	74	67	L47	O	
	75	68	L48	O	
	77	69	L49	O	
	78	70	L50	O	
	79	71	L51	O	
	80	72	L52	O	
	82	73	L53	O	
	83	74	L54	O	
	84	75	L55	O	
	86	76	L56	O	
	87	77	L57	O	
	88	78	L58	O	
	89	79	L59	O	
	90	80	L60	O	
	91	81	L61	O	
	92	82	L62	O	
	93	83	L63	O	

Secondary Functions

Function	Pin	Pad	Symbol	Type	Description
External Interrupts	9	8	P0.0	I	External level-sensitive interrupt input pins
	10	9	P0.1		
	12	10	P0.2		
	14	11	P0.3		
	16	12	P1.0		
	17	13	P1.1		
	19	14	P1.2		
	21	15	P1.3		
	22	16	P2.0		
	24	17	P2.1		
	25	18	P2.2		
	26	19	P2.3		
Capture trigger	16	12	P1.0	I	Trigger input pin of the capture circuit
	17	13	P1.1	I	
Serial Port	10	9	P0.1	I	Receive data input pin (RXD) of serial port
	22	16	P2.0	I/O	Transmit clock input/output pin (TXT) of serial port
	24	17	P2.1	I/O	Receive clock output pin (RXC) of serial port
	25	18	P2.2	O	Transmit data output pin (TXD) of serial port
Timer	9	8	P0.0	I	Capture trigger input pin of timer
	12	10	P0.2	I	External clock input pin (TMC) of timer
	26	19	P2.3	O	Timer overflow flag output pin (TMO) of timer

MEMORY MAPS

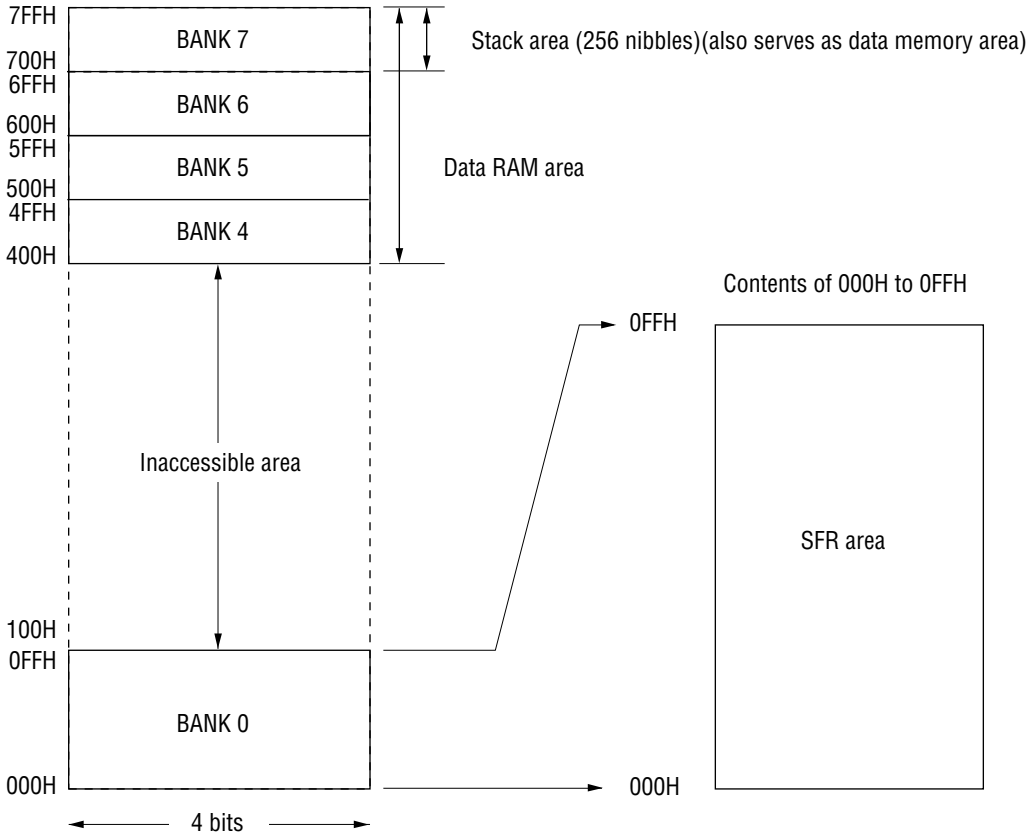
Program Memory



Address 000H is the start address of the instruction execution at system reset.
The "CZP" area from address 010H to 01FH is the start address for the CZP subroutine of one-byte call instruction.
The interrupt area from address 020H to 3DH is assigned the start address of interrupt subroutines. 8160 bytes from address 000H to 1FDFH are available for users. The test program area cannot be used as a program memory area.

Data Memory

The data memory area consists of eight banks and each bank has 256 nibbles (256 × 4 bits). The data RAM is assigned to BANK 4 through BANK 7 and Special Function Registers (SFRs) are assigned to BANK 0.



Quarter the data RAM area (256 nibbles) also serves as the stack area.
The stack is a memory starting from address 7FFH toward the lower-order addresses where 4 nibbles are used by subroutine call instruction and 8 nibbles are used by an interrupt.
It has no access to the area from BANK 1 to BANK 3.

ABSOLUTE MAXIMUM RATINGS

(V_{DD}=V_{DDA}=0 V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage 1	V_{SS1}	Ta=25°C	–2.0 to +0.3	V
Power Supply Voltage 2	V_{SS2}	Ta=25°C	–4.0 to +0.3	V
Power Supply Voltage 3	V_{SS3}	Ta=25°C	–5.5 to +0.3	V
Power Supply Voltage 4	V_{SSL}	Ta=25°C	–4.0 to +0.3	V
Power Supply Voltage 5	V_{SS}	Ta=25°C	–5.5 to +0.3	V
Power Supply Voltage 6	V_{SSA}	Ta=25°C	–4.0 to +0.3	V
Input Voltage 1	V_{IN1}	V_{SS2} input, Ta=25°C	V_{SS2}–0.3 to +0.3	V
Input Voltage 2	V_{IN2}	V_{SS} input, Ta=25°C	V_{SS}–0.3 to +0.3	V
Input Voltage 3	V_{IN3}	V_{SS1} input, Ta=25°C	V_{SS1}–0.3 to +0.3	V
Input Voltage 4	V_{IN4}	V_{SSA} input, Ta=25°C	V_{SSA}–0.3 to +0.3	V
Output Voltage 1	V_{OUT1}	V_{SS2} output, Ta=25°C	V_{SS2}–0.3 to +0.3	V
Output Voltage 2	V_{OUT2}	V_{SS3} output, Ta=25°C	V_{SS3}–0.3 to +0.3	V
Output Voltage 3	V_{OUT3}	V_{SS} output, Ta=25°C	V_{SS}–0.3 to +0.3	V
Output Voltage 4	V_{OUT4}	V_{SS1} output, Ta=25°C	V_{SS1}–0.3 to +0.3	V
Output Voltage 5	V_{OUT5}	V_{SSA} output, Ta=25°C	V_{SSA}–0.3 to +0.3	V
Storage Tempertaure	T_{STG}	—	–55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

(V_{DD}=V_{DDA}=0 V)

Parameter	Symbol	Condition	Range	Unit
Operating Temperature	T_{op}	—	–40 to +85	°C
Operating Voltage	V_{SS2} V_{SSA}	V_{SS2}=V_{SSA}	–3.6 to –2.6	V
	V_{SS}	—	–5.25 to (0.8 • V_{SS2}, –2.6 max) (*)	V
700 kHz OSC External Resistor	R_{OS}	—	90 to 300	kΩ
Crystal Oscillator Frequency	f_{XT}	—	30 to 66	kHz

* Indicates that the value of V_{SS} is 80% of V_{SS2} and should not exceed –2.6 V.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD}=V_{DDA}=0 V, V_{SS2}=V_{SS}= –3.0 V, Ta= –40 to +85°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
V_{SS1} Voltage	V_{SS1}	Ca, Cb, C12=0.1 µF +100% –50%	–1.7	–1.5	–1.3	V	1
V_{SS3} Voltage	V_{SS3}	Ca, Cb, C12=0.1 µF +100% –50%	–4.7	–4.5	–4.3	V	
V_{SSL} Voltage	V_{SSL}	—	–2.1	–1.5	–0.6	V	
XTOSC Oscillation Start Voltage	V_{STA}	Within 5 seconds after oscillation starts	—	—	–2.6	V	
XTOSC Oscillation Hold Voltage	V_{HOLD}	—	—	—	–2.6	V	
XTOSC Stop Detection Time	T_{STOP}	—	0.1	—	1000	ms	
XTOSC Internal Capacitance	C_G	—	10	15	20	pF	
XTOSC External Capacitance	C_{GEX}	When C_G external option is used	10	—	30	pF	
XTOSC Internal Capacitance	C_D	—	10	15	20	pF	
700kOSC Internal Capacitance	C_{OS}	—	8	12	16	pF	
700kOSC Oscillation Frequeney	f_{OSC}	External resistor R_{OS}=100 kΩ, V_{SS2}=–2.6 to –3.6 V	520	700	910	kHz	
POR Generation Voltage	V_{POR1}	POR generated when V_{SS2} is between V_{POR1} and –3.0 V	–0.7	—	0	V	
POR Non-generation Voltage	V_{POR2}	No POR generated when V_{SS2} is between V_{POR2} and –3.0 V	–3	—	–2	V	

Notes: 1. "XTOSC" means a 32 kHz oscillation circuit.
2. "700kOSC" means 700 kHz RC oscillation circuit.
3. "POR" means Power-On Reset.
4. "T_{STOP}" means that system reset will occur if XTOSC stops oscillation over this time.

DC Characteristics (Continued)

(V_{DD}=V_{DDA}=0 V, V_{SS2}=V_{SS}= –3.0 V, Ta= –40 to +85°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Current Consumption 1	I_{DD1}	CPU in HALT state (700kOSC stop)		—	1.2	4.5	µA	1
Current Consumption 2	I_{DD2}	CPU in operation (700kOSC stop)		—	5	15	µA	
Current Consumption 3	I_{DD3}	CPU in operation (700kOSC in operation)		—	400	800	µA	
Current Consumption 4	I_{DD4}	A/D converter in operation, CPU in HALT state (700kOSC stop)	Voltage amplification circuit stop	—	200	300	µA	
			Voltage amplification circuit in operation	—	400	600	µA	

DC Characteristics (Continued)

(V_{DD}=V_{DDA}=0 V, V_{SS1}=V_{SSL}= –1.5 V, V_{SS2}=V_{SS}=V_{SSA}= –3.0 V, V_{SS3}= –4.5 V, Ta= –40 to +85°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Output Current 1	I_{OH1}	V_{OH1}=–0.5 V	–6	–2	–0.7	mA	2
(P0.0 to P0.3)	I_{OL1}	V_{OL1}=V_{SS}+0.5 V	0.7	2	6	mA	
(P1.0 to P1.3)	I_{OH1S}	V_{SS}=–5 V, V_{OH1S}=–0.5 V	–9	–3	–1	mA	
(P2.0 to P2.3)	I_{OL1S}	V_{SS}=–5 V, V_{OL1S}=V_{SS}+0.5 V	1	3	9	mA	
Output Current 2	I_{OH2}	V_{OH2}=–0.7 V	–6	–2	–0.7	mA	
(BD)	I_{OL2}	V_{OL2}=V_{SS2}+0.7 V	0.7	2	6	mA	
Output Current 3	I_{OH3}	V_{OH3}=–0.5 V	–3.0	–1.2	–0.2	mA	
(R_I, C_I, OPO0, OPO1)	I_{OL3}	V_{OL3}=V_{SS}+0.5 V	15	30	100	µA	
Output Current 4	I_{OH4}	V_{OH4}=–0.5 V	–1.5	–0.6	–0.15	mA	
(When L0 to L7 are	I_{OL4}	V_{OL4}=V_{SS}+0.5 V	0.15	0.6	1.5	mA	
output ports)	I_{OH4S}	V_{SS}=–5 V, V_{OH4}=–0.5 V	–2	–0.7	–0.2	mA	
	I_{OL4S}	V_{SS}=–5 V, V_{OL4S}=V_{SS}+0.5 V	0.2	0.7	2.0	mA	
Output Current 5	I_{OH5}	V_{OH5}=–0.5 V	–6	–2	–0.7	mA	
(OSC2)	I_{OL5}	V_{OL5}=V_{SSL}+0.5 V	0.7	2	6	mA	
Output Current 6	I_{OH6}	V_{OH6}=–0.2 V (V_{DD} level)	—	—	–4	µA	
(L0 to L30)	I_{OMH6}	V_{OMH6}=V_{SS1}+0.2 V (V_{SS1} level)	4	—	—	µA	
	I_{OMH6S}	V_{OMH6S}=V_{SS1}–0.2 V (V_{SS1} level)	—	—	–4	µA	
	I_{OML6}	V_{OML6}=V_{SS2}+0.2 V (V_{SS2} level)	4	—	—	µA	
	I_{OML6S}	V_{OML6S}=V_{SS2}–0.2 V (V_{SS2} level)	—	—	–4	µA	
	I_{OL6}	V_{OL6}=V_{SS3}+0.2 V (V_{SS3} level)	4	—	—	µA	
Output Leakage	I_{OOH}	V_{OH}=V_{DD}	—	—	0.3	µA	
(P0.0 to P0.3)	I_{OOL}	V_{OL}=V_{SS2}	–0.3	—	—	µA	
(P1.0 to P1.3)							
(P1.0 to P1.3)							

DC Characteristics (Continued)

(V_{DD}=V_{DDA}=0 V, V_{SS1}=V_{SSL}= –1.5 V, V_{SS2}=V_{SS}=V_{SSA}= –3.0 V, V_{SS3}= –4.5 V, Ta= –40 to +85°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
	I_{IH1}	V_{IH1}=V_{DD} (When pulled down)	30	90	300	µA	
Input Current 1	I_{IL1}	V_{IL1}=V_{SS} (When pulled up)	–300	–90	–30	µA	
(P0.0 to P0.3)	I_{IH1S}	V_{IH1}=V_{DD}, V_{SS}=–5 V	80	250	800	µA	
(P1.0 to P1.3)		(When pulled down)					
(P2.0 to P2.3)	I_{IL1S}	V_{IL1}=V_{SS}=–5 V(When pulled up)	–800	–250	–80	µA	
	I_{IH1Z}	V_{IH1}=V_{DD} (At high impedance)	0	—	1	µA	
	I_{IL1Z}	V_{IL1}=V_{SS} (At high impedance)	–1	—	0	µA	
Input Current 2	I_{IL2}	V_{IL2}=V_{SSA} (When pulled up)	–300	–90	–30	µA	
(OPP0, OPP1, OPN0,	I_{IH2Z}	V_{IH2}=V_{DD} (At high impedance)	0	—	1	µA	
OPN1, V_{OF})	I_{IL2Z}	V_{IL2}=V_{SSA} (At high impedance)	–1	—	0	µA	3
Input Current 3	I_{IL3}	V_{IL3}=V_{SSA} (ENADC=0)	–375	–250	–125	µA	
(VrA)	I_{IH3}	V_{IH3}=VrA+30 mV (ENADC=1)	1	8	—	mA	
Input Current 4	I_{IL4}	V_{IL4}=V_{SS2} (When pulled up)	–300	–110	–10	µA	
(OSC1)	I_{IH4Z}	V_{IH4}=V_{DD} (At high impedance)	0	—	1	µA	
	I_{IL4Z}	V_{IL4}=V_{SS2} (At high impedance)	–1	—	0	µA	
Input Current 5	I_{IH5}	V_{IH5}=V_{DD}	0	—	1	µA	
($\overline{RESET}$, $\overline{TST1}$, $\overline{TST2}$)	I_{IL5}	V_{IL5}=V_{SS2}	–3	–1.5	–0.75	mA	
Input Current 6	I_{IH6Z}	V_{IH6}=V_{DD} (At high impedance)	0	—	1	µA	
(R_{CM}, C_{Z1}, C_{Z2}	I_{IL6Z}	V_{IL6}=V_{SSA} (At high impedance)	–1	—	0	µA	
AIN0 to 3, R_A)							
Input Voltage 1	V_{IH1}		–0.6	—	0	V	
(P0.0 to P0.3)	V_{IL1}		–3.0	—	–2.4	V	
(P1.0 to P1.3)	V_{IH1S}	V_{SS}=–5 V	–1	—	0	V	4
(P2.0 to P2.3)	V_{IL1S}	V_{SS}=–5 V	–5	—	–4	V	
Input Voltage 2	V_{IH2}		–0.6	—	0	V	
(OSC1, $\overline{RESET}$, $\overline{TST1}$, $\overline{TST2}$)	V_{IL2}		–3.0	—	–2.4	V	

DC Characteristics (Continued)

(V_{DD}=V_{DDA}=0 V, V_{SS1}=V_{SSL}= −1.5 V, V_{SS2}=V_{SS}=V_{SSA}= −3.0 V, V_{SS3}= −4.5 V, Ta= −40 to +85°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Hysteresis Width (P0.0 to P0.3) (P1.0 to P1.3) (P2.0 to P2.3)	ΔV_{T1}	—	0.2	0.5	1	V	4
	ΔV_{T1S}	V_{SS}=−5 V	0.25	1.0	1.5	V	
Hysteresis Width ($\overline{RESET}$, $\overline{TST1}$, $\overline{TST2}$)	ΔV_{T2}	—	0.2	0.5	1	V	
Input Capacitance (P0.0 to P0.3) (P1.0 to P1.3) (P2.0 to P2.3)	C_{IN}	—	—	—	5	pF	1

A/D Converter Characteristics

(V_{DD}=V_{DDA}=0 V, V_{SS2}=V_{SS}=V_{SSA}= –3 V, Ta= –40 to +85°C, VrA=–1.2 V, at execution of 12-bit A/D conversion, unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Analog Input Voltage Range (AIN0 to AIN3)	V_{AIN}	—	–1.2	—	–0.4	V	5
Analog Input Voltage Range (OPP0, OPP1) (V_{OF})	V_{OPP}	—	–1.6	—	–0.4	V	
Resolution	—	—	—	—	12+S*	bits	
Linearity Error	—	—	–1	—	+1	LSB	
Zero Scale Error	—	—	–2	—	+2	LSB	
Full Scale Error	—	—	–16	—	+16	LSB	
VrA Voltage (VrA)	VrA	Ta=25°C	–1300	–1200	–1100	mV	
VrA Temperature Coefficient	—	—	–8	—	2	mV/°C	
V_G Voltage (V_G)	V_G	Ta=25°C	–867	–800	–733	mV	
R_A Voltage (R_A)	V_{RA}	Ta=25°C	–440	–400	–360	mV	

* "S" indicates a sign bit.

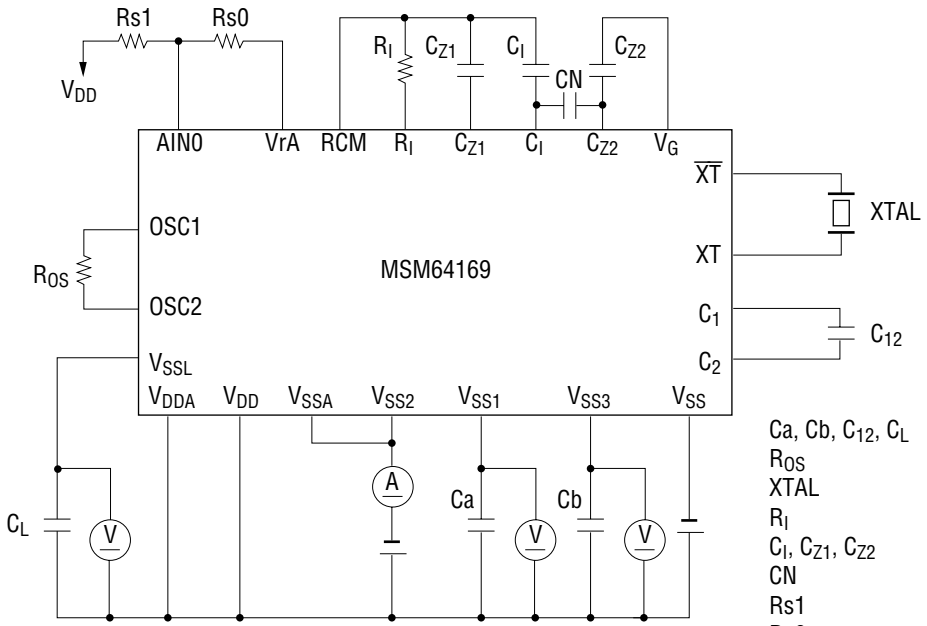
Voltage Amplification Circuit Characteristics

(V_{DD}=V_{DDA}=0 V, V_{SS2}=V_{SS}=V_{SSA}= –3 V, Ta= –40 to +85°C unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition (*1)	Min.	Typ.	Max.	Unit	Measuring Circuit
Amplifier Gain Error *1	Eg (*2)	V_{OPP1}–V_{OPP0}=10 mA, Gain=40 $Eg=\frac{(V_{OPO1}-V_{OPO0})/(V_{OPP1}-V_{OPP0})}{Gain}-1$	–3.0	–1.5	0	%	5
Level Shift Error *1	EI	$EI=\frac{(V_{AIN3}-V_{VOF})}{(V_{OPO1}-V_{OPO0})}-1$	–4	—	+4	%	

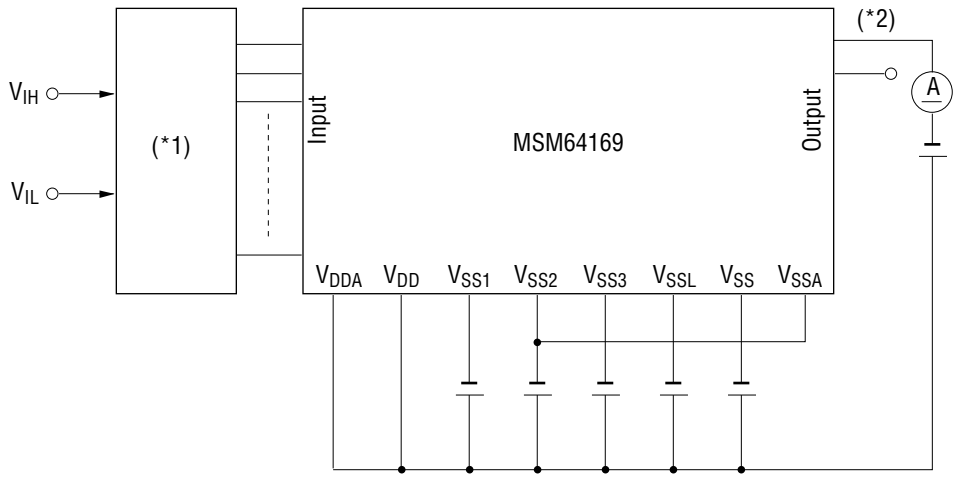
*1 Errors caused by offset voltage are excluded.
*2 Errors decrease in proportion to gain.

Measuring Circuit 1

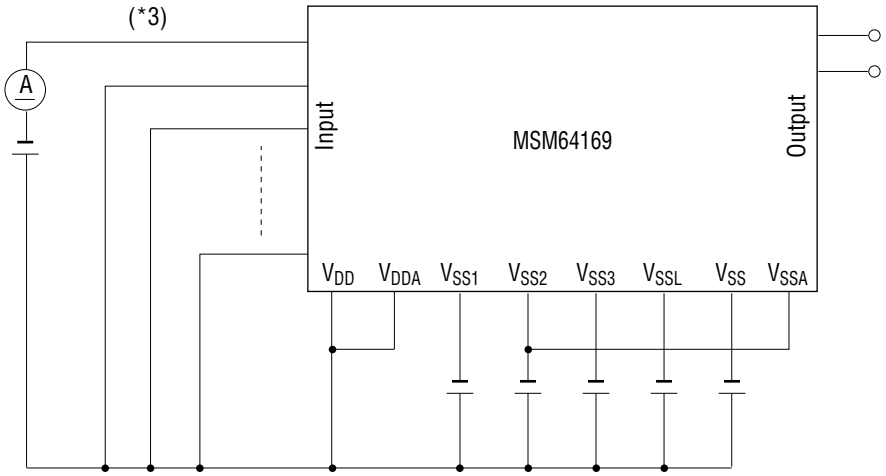


Ca, Cb, C_{12}, C_L	: 0.1 µF
R_{OS}	: 100 kΩ
XTAL	: 32.768 kHz
R_I	: 750 kΩ
C_I, C_{Z1}, C_{Z2}	: 0.1 µF
CN	: 1000 pF
Rs1	: 100 kΩ
Rs0	: 10 kΩ

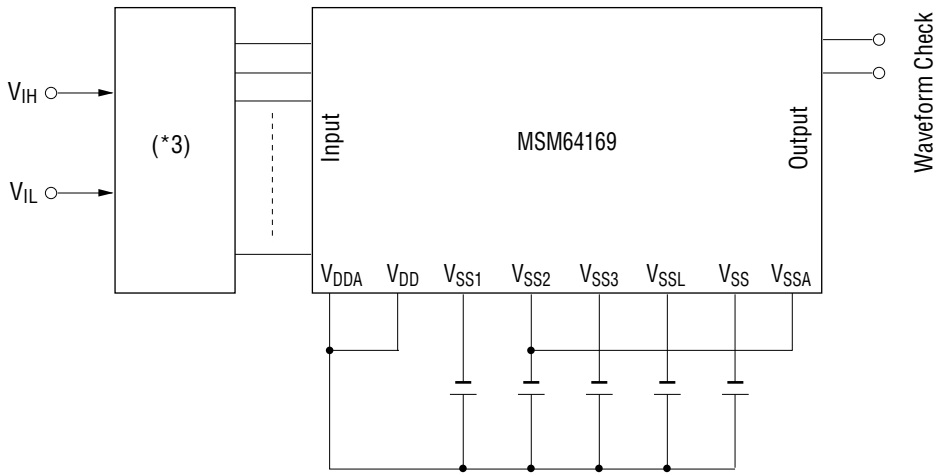
Measuring Circuit 2



Measuring Circuit 3

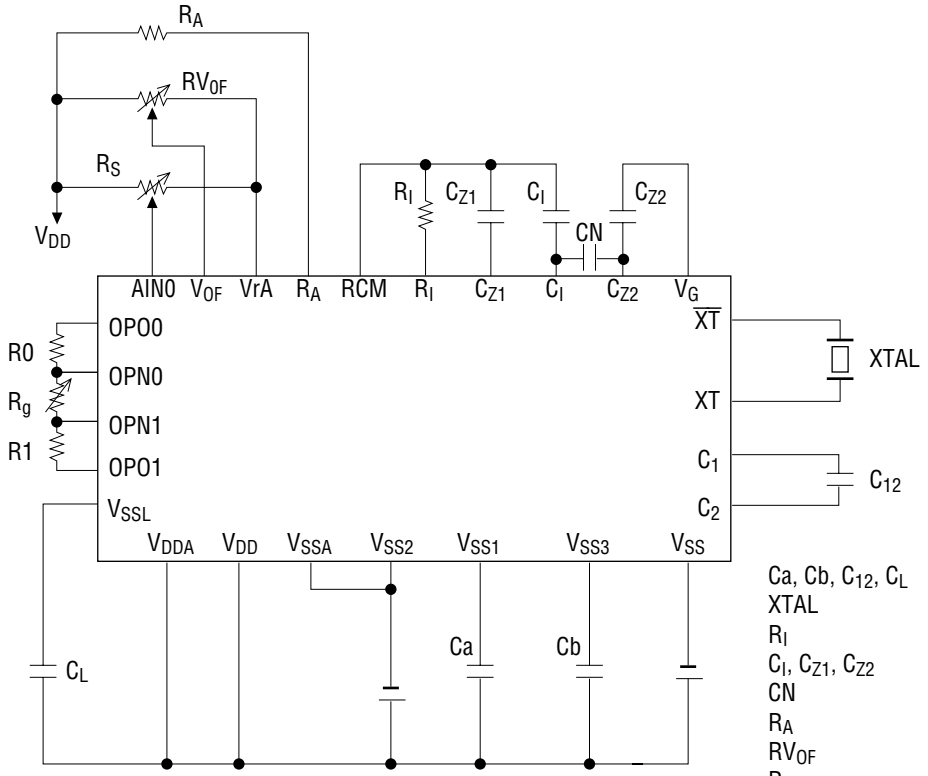


Measuring Circuit 4



*1 Input logic selects specified state.
*2 Repeated for each specified output pin.
*3 Repeated for each specified input pin.

Measuring Circuit 5



Ca, Cb, C_{12}, C_L	: 0.1 µF
XTAL	: 32.768 kHz
R_I	: 750 kΩ
C_I, C_{Z1}, C_{Z2}	: 0.1 µF
CN	: 1000 pF
R_A	: 10 kΩ
RV_{0F}	: 10 kΩ max
R_S	: 10 kΩ max
R0, R1	: 270 kΩ
R_g	: 100 kΩ max

FUNCTIONAL DESCRIPTION

CPU Peripheral Function

• A/D converter (ADC)

The MSM64169 has a 4-channel input dual slope A/D converter. In dual slope A/D conversion, the relationship between integral voltage and time is given by:

$$Vin/Vr = t1/t2$$

where,

t1 = given time for which an analog input voltage is integrated
Vr = reference voltage
Vin = voltage resulted from charging for t1
t2 = time required to discharge the voltage, from Vr to Vin

From the above equation, Vin is found.

The range of Vin is –0.8 ±0.4 V. The A/D converter resolution time is programmable. The A/D converter has a preamplifier for amplifying a microvoltage. It is suited to applications such as thermometer, pressure gauge, and hygrometer.

• LCD driver (LCD)

The MSM64169 has a built-in LCD driver for 64 outputs.

The LCD driver consists of 64 × 4-bit display registers (64 nibbles out of DSPR0 to 127), a display control register (DSPCON), a 63-output LCD driver circuit, and a bias generation circuit (BIAS).

There are three types of driving methods: 1/4 duty, 1/3 duty and 1/2 duty.

A mask option can select either a common driver or a segment driver for each LCD driver pin.

A mask option can also specify the assignment of each bit of the display register to each segment.

L0 to L7 of the LCD driver can become output ports via a mask option.

The relationship between the duty, the bias method and the maximum segment number follows:

1/4 duty 1/3 bias method ..... 240 segments
1/3 duty 1/3 bias method ..... 184 segments
1/2 duty 1/2 bias method ..... 124 segments

• Port (P0, P1, P2)

The MSM64169 has three input-output ports (P0, P1, P2) with 4 bits each. Each bit of the ports can be configured to be an input or output, pull-up/pull-down resistor input or high impedance input, or NMOS open drain output or CMOS output. A change in the input level of each pin of P0 and P1 generates an external interrupt 0 request, and a change in the input level of each pin of P2 generates an external interrupt 1 request.

The serial port function and the timer function area assigned as the secondary funciton.

• Buzzer driver (BD)

The MSM64169 has a built-in buzzer driver with two buzzer output frequencies and four buzzer output modes. Each buzzer output is selected by the Buzzer Control Register (BDCON) and the Buzzer Frequency Control Register (BFCON).

• Serial port (SIOP)

The MSM64169 has a serial port (SIOP). The serial port is a synchronous/asynchronous selectable serial communication port. The transmit section and the receive section are independent of each other, which allows simultaneous operation of transmission and receiving.

• Watchdog timer (WDT)

The MSM64169 has a built-in watchdog timer to detect CPU run-away. The watchdog timer consists of a 6-bit watchdog timer counter (WDTC), which counts the 16 Hz output of the time base counter, and a watchdog timer control register (WDTCON) to reset WDTC.

• Capture circuit (CAP)

The MSM64169 captures a 32 Hz to 256 Hz output of the time base counter at the falling edge of Port 1.0 or 1.1 (P1.0 or P1.1) when the pull-up resistor input is chosen, or at the rising edge when the pull-down resistor input is chosen.
The capture circuit is composed of the Capture Control Register (CAPCON) and the Capture Registers (CAPR0, CAPR1) that fetch output from the time base counter.

•Timer (TM)

The MSM64169 has a 16-bit timer (TM). The timer has three operation modes: auto-reload mode, capture mode, and clock frequency measuring mode. It counts at 32.768 kHz or 700 kHz or by an external clock. The timer is used for pulse generation, time measurement, etc., and is also used as an A/D conversion counter at A/D conversion and as a baud rate generator at serial communication.

• Clock generation circuit (2CLK)

The MSM64169 has a clock generation circuit (2CLK) that generates clocks of two types: low-speed and high-speed. The circuit consists of a 32.768 kHz crystal oscillation circuit, a 700 kHz RC oscillation cricuit, and a clock control section. This circuit generates the system clock (CLK), crystal oscillation clock (32.768 kHz), and RC oscillation clock (700 kHz).
The system clock is the basic operation clock of the CPU, and the crystal oscillation clock is the basic operation clock of the time-base counter and the buzzer driver. The crystal oscillation clock and RC oscillation clock are supplied to the timer to become a timer clock.
The system clock frequency is switched between 32.768 kHz (output of the crystal oscillation circuit) and 700 kHz (output of the RC oscillation circuit) based on the contents of the frequency control register (FCON).

Note: The oscillation frequency of the RC oscillation circuit varies depending on the value of external resistor (R_{OS}), operating voltage (V_{SS2}), and ambient temperature (Ta).

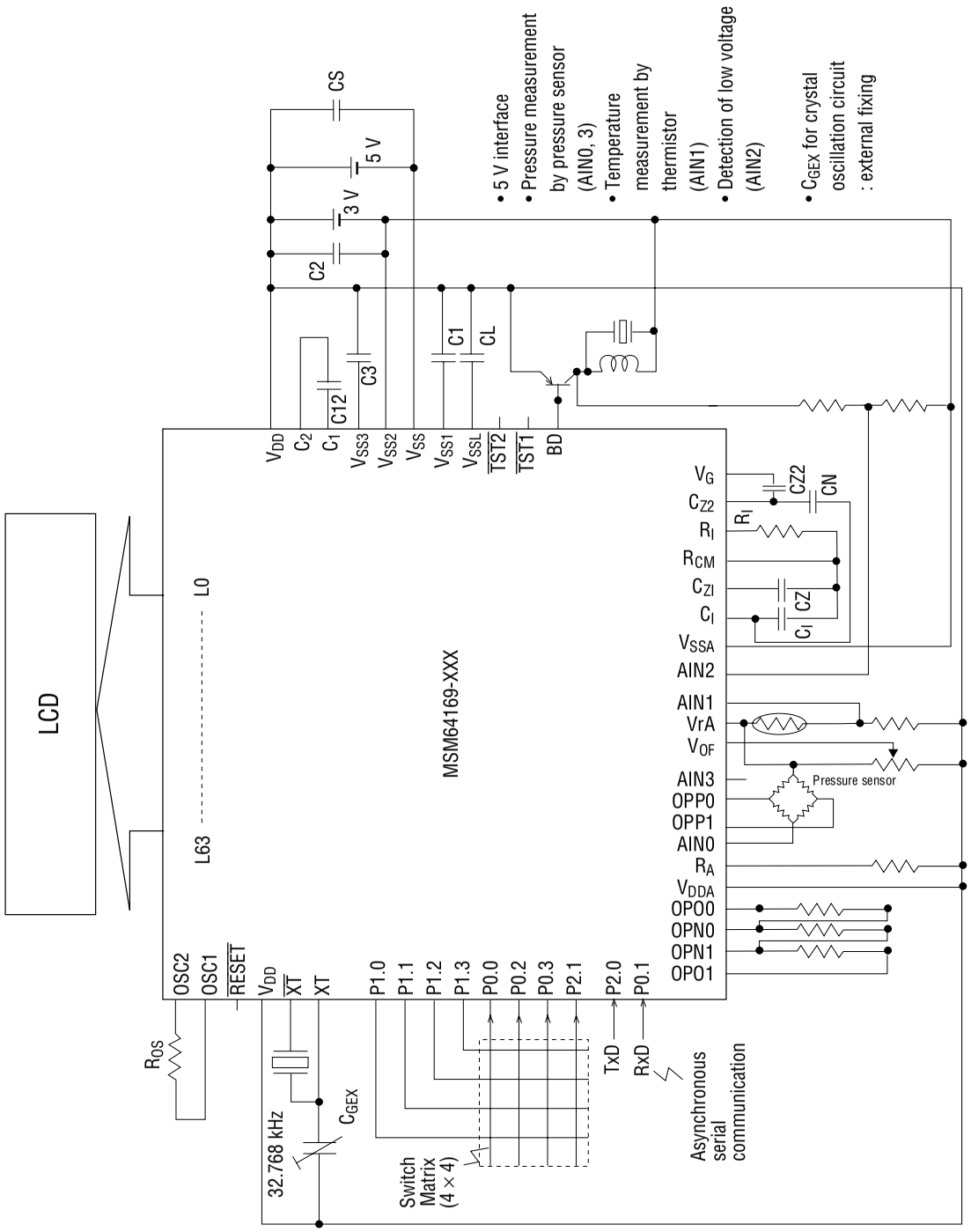
• Time base counter (TBC)

The MSM64169 has a built-in time base counter (TBC) that generates clocks to be supplied to internal peripheral circuits. The time base counter is composed of 15 binary counters. The count clock of the time base is supplied by the oscillation clock (32.768 kHz) of the crystal oscillation circuit. Output of the time base counter is used for buzzer driver, system reset circuit, watchdog timer, time base interrupt, sampling clocks for each port, and LCD driver.

• Interrupt (INTC)

The MSM64169 has ten interrupt sources (ten vector addresses) of which two are external interrupts from ports and eight are internal interrupts.
Of the ten interrupt sources, only the watchdog interrupt cannot be disabled (non-maskable interrupt). The other nine interrupts are controlled by the master interrupt enable flag (MI) and the interrupt enable registers (IE0, IE1 and IE2). When an interrupt condition is met, the program branches to a vector address corresponding to the interrupt source, and then control is passed to the interrupt routine.

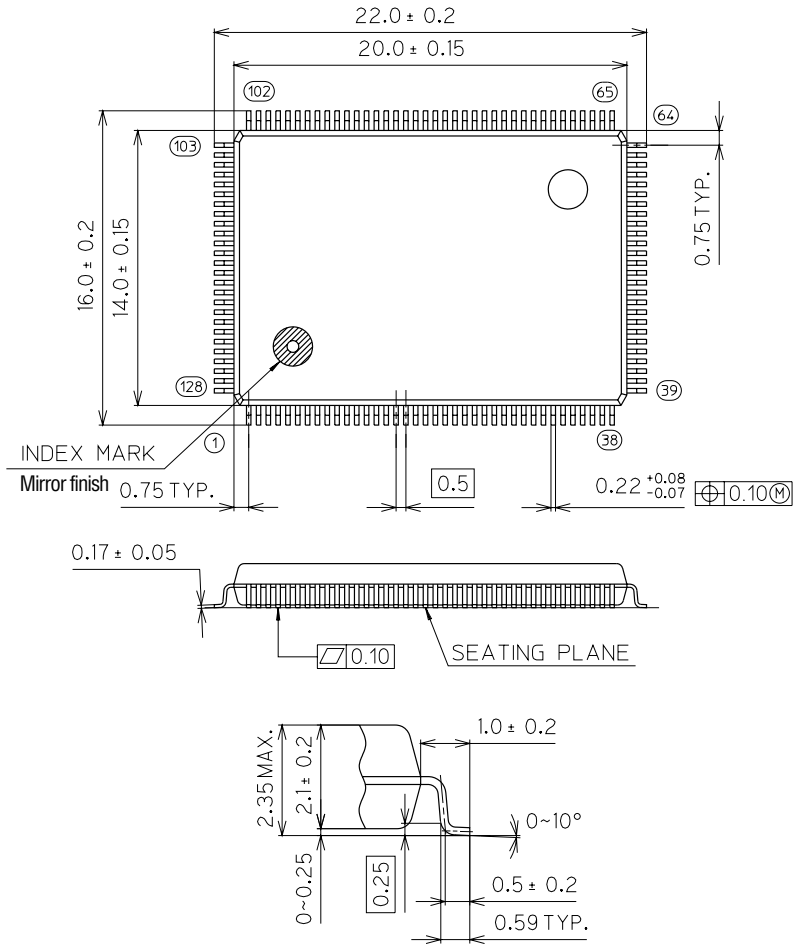
APPLICATION CIRCUIT



PACKAGE DIMENSIONS

(Unit : mm)

QFP128-P-1420-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.19 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).