

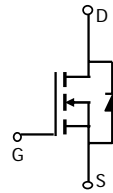
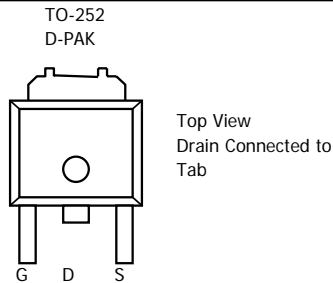
**AOD4120**  
**N-Channel Enhancement Mode Field Effect Transistor**

**General Description**

The AOD4120 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications. Standard product AOD4120 is Pb-free (meets ROHS & Sony 259 specifications). AOD4120L is a Green Product ordering option. AOD4120 and AOD4120L are electrically identical.

**Features**

$V_{DS}$  (V) = 20V  
 $I_D$  = 25A ( $V_{GS}$  = 10V)  
 $R_{DS(ON)}$  < 18 m $\Omega$  ( $V_{GS}$  = 10V)  
 $R_{DS(ON)}$  < 25 m $\Omega$  ( $V_{GS}$  = 4.5V)  
 $R_{DS(ON)}$  < 75 m $\Omega$  ( $V_{GS}$  = 2.5V)  
**UIS Tested**  
**Rg, Ciss, Coss, Crss Tested**


**Absolute Maximum Ratings  $T_A=25^\circ\text{C}$  unless otherwise noted**

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	20	V
Gate-Source Voltage	$V_{GS}$	$\pm 16$	V
Continuous Drain Current	$T_C=25^\circ\text{C}^G$	25	A
	$T_C=100^\circ\text{C}$	23	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	75	
Avalanche Current <sup>C</sup>	$I_{AR}$	13	A
Repetitive avalanche energy $L=0.3\text{mH}^C$	$E_{AR}$	25	mJ
Power Dissipation <sup>B</sup>	$T_C=25^\circ\text{C}$	33	W
	$T_C=100^\circ\text{C}$	16.7	
Power Dissipation <sup>A</sup>	$T_A=25^\circ\text{C}$	2.5	W
	$T_A=70^\circ\text{C}$	1.7	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^\circ\text{C}$

**Thermal Characteristics**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	17	25	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A</sup>		Steady-State	40	50
Maximum Junction-to-Case <sup>B</sup>	$R_{\theta JC}$	3.6	4.5	$^\circ\text{C/W}$

Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$ , $V_{GS}=0\text{V}$	20			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=16\text{V}$ , $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	$\mu\text{A}$
$I_{GSS}$	Gate-Body leakage current	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 16\text{V}$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$	0.6	1.26	2	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}$ , $V_{DS}=5\text{V}$	75			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$ , $I_D=20\text{A}$ $T_J=125^\circ\text{C}$		14 21	18	m $\Omega$
		$V_{GS}=4.5\text{V}$ , $I_D=10\text{A}$		20	25	
		$V_{GS}=2.5\text{V}$ , $I_D=4\text{A}$		57	75	
$g_{FS}$	Forward Transconductance	$V_{DS}=5\text{V}$ , $I_D=20\text{A}$		19		S
$V_{SD}$	Diode Forward Voltage	$I_S=1\text{A}$ , $V_{GS}=0\text{V}$		0.77	1	V
$I_S$	Maximum Body-Diode Continuous Current <sup>G</sup>				30	A
<b>DYNAMIC PARAMETERS</b>						
$C_{iss}$	Input Capacitance	$V_{GS}=0\text{V}$ , $V_{DS}=10\text{V}$ , $f=1\text{MHz}$		900		pF
$C_{oss}$	Output Capacitance			162		pF
$C_{riss}$	Reverse Transfer Capacitance			105		pF
$R_g$	Gate resistance	$V_{GS}=0\text{V}$ , $V_{DS}=0\text{V}$ , $f=1\text{MHz}$		1.8	2.7	$\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$ , $V_{DS}=10\text{V}$ , $I_D=20\text{A}$		15	18	nC
$Q_g(4.5\text{V})$	Total Gate Charge			7.2	9	nC
$Q_{gs}$	Gate Source Charge			1.8		nC
$Q_{gd}$	Gate Drain Charge			2.8		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}$ , $V_{DS}=10\text{V}$ , $R_L=0.5\Omega$ , $R_{GEN}=3\Omega$		4.5		ns
$t_r$	Turn-On Rise Time			9.2		ns
$t_{D(off)}$	Turn-Off DelayTime			18.7		ns
$t_f$	Turn-Off Fall Time			3.3		ns
$t_{rr}$	Body Diode Reverse Recovery Time		$I_F=20\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		18	
$Q_{rr}$	Body Diode Reverse Recovery Charge	$I_F=20\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		9.5		nC

A: The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The Power dissipation  $P_{DSM}$  is based on  $R_{\theta JA}$  and the maximum allowed junction temperature of  $150^\circ\text{C}$ . The value in any given application depends on the user's specific board design, and the maximum temperature of  $175^\circ\text{C}$  may be used if the PCB allows it.

B: The power dissipation  $P_D$  is based on  $T_{J(MAX)}=175^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}=175^\circ\text{C}$ .

D: The  $R_{\theta JA}$  is the sum of the thermal impedance from junction to case  $R_{\theta JC}$  and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using  $<300 \mu\text{s}$  pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of  $T_{J(MAX)}=175^\circ\text{C}$ .

G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The SOA curve provides a single pulse rating.

Rev0: Sept 2006

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

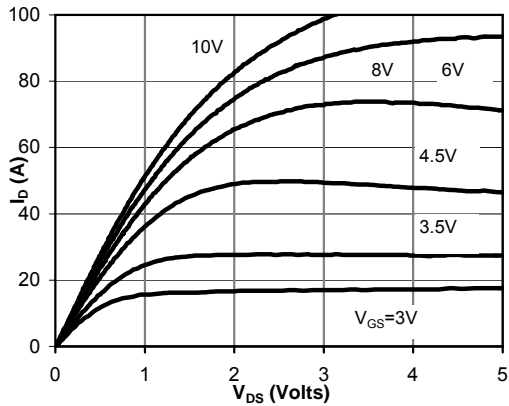


Fig 1: On-Region Characteristics

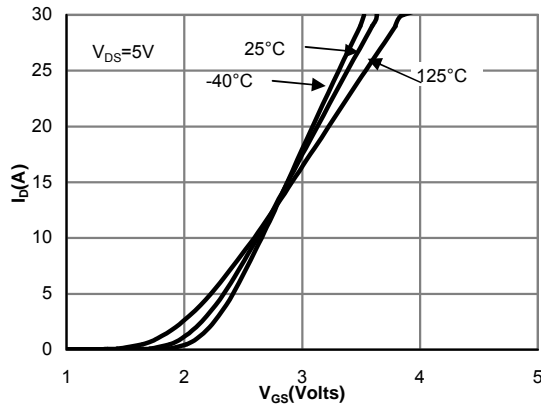


Figure 2: Transfer Characteristics

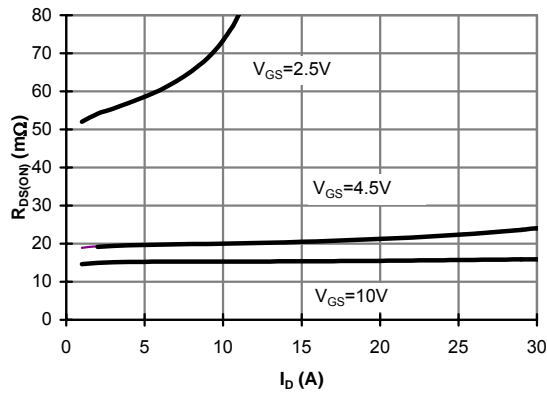


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

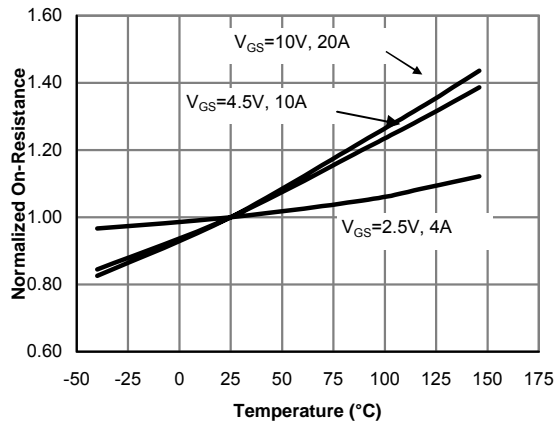


Figure 4: On-Resistance vs. Junction Temperature

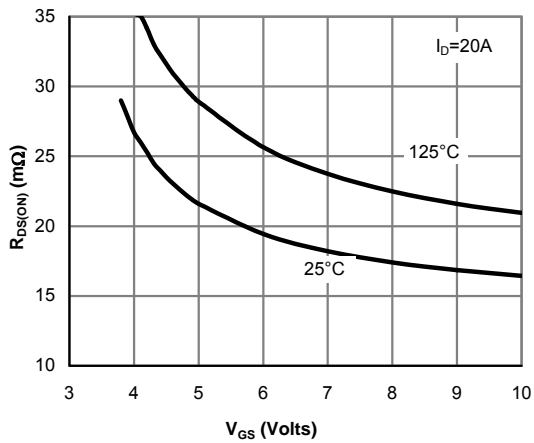


Figure 5: On-Resistance vs. Gate-Source Voltage

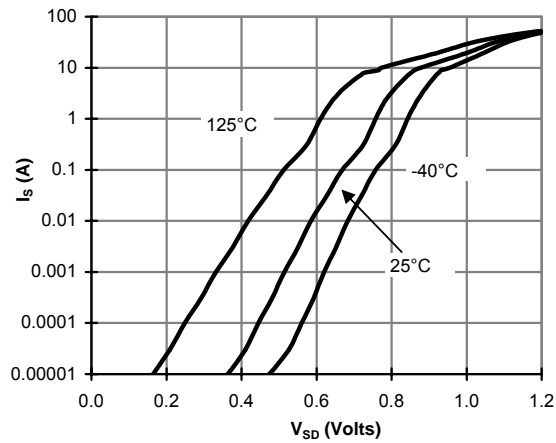


Figure 6: Body-Diode Characteristics

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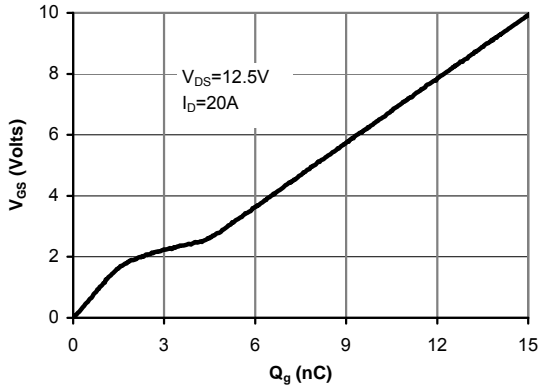


Figure 7: Gate-Charge Characteristics

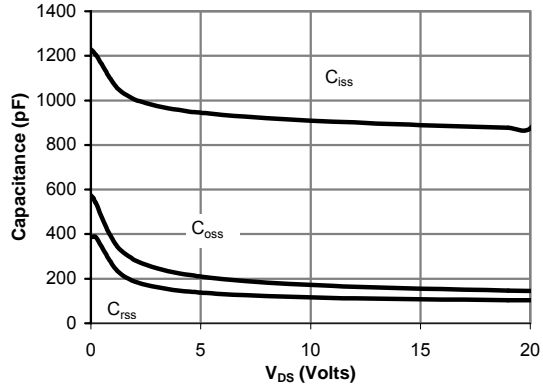


Figure 8: Capacitance Characteristics

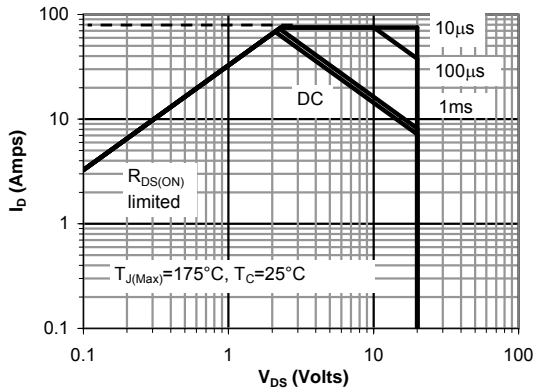


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

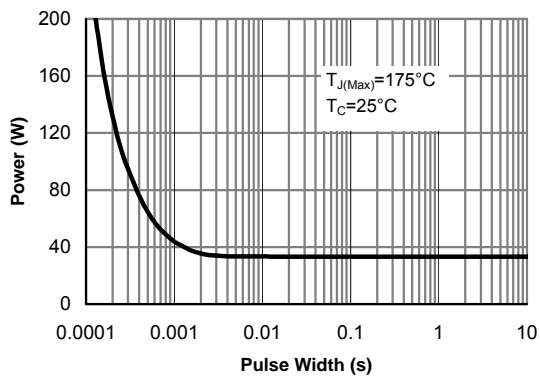


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

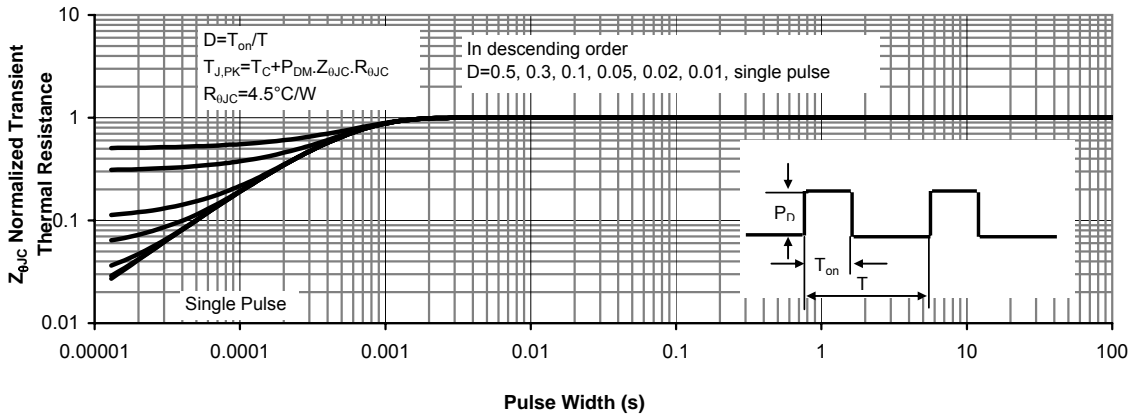


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

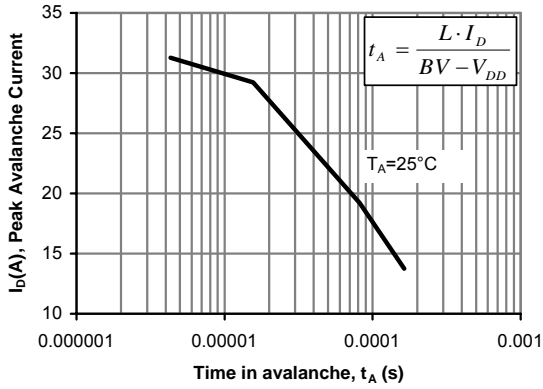


Figure 12: Single Pulse Avalanche capability

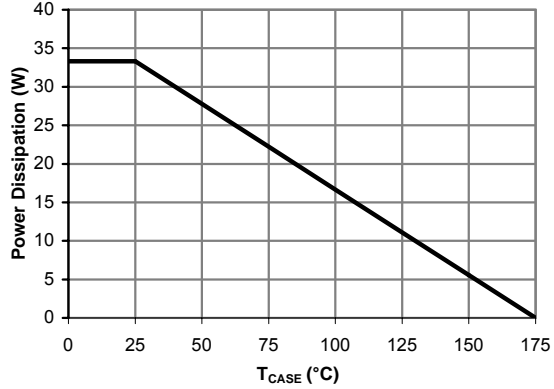


Figure 13: Power De-rating (Note B)

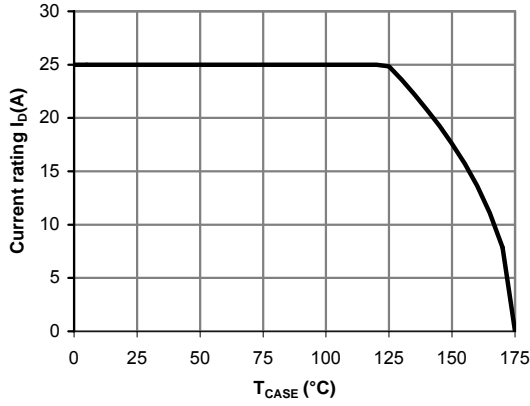


Figure 14: Current De-rating (Note B)

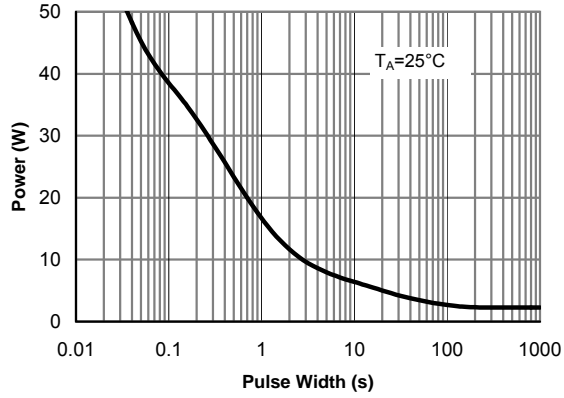


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

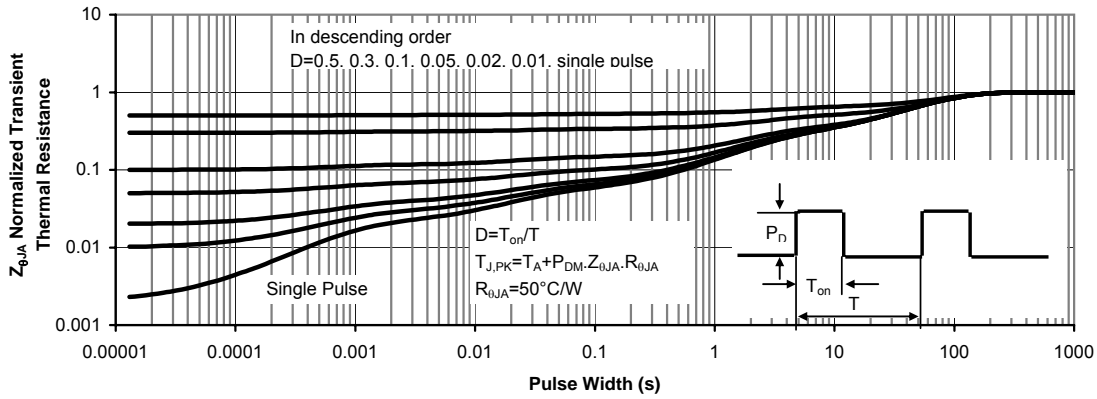


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)