



AL4CS211

AL4CS221

AL4CS231

AL4CS241

AL4CS251

# Data Sheets

Version 1.1

## Amendments

07.11.01 Preliminary Version 1.0

10.17.01 Version 1.1, Added DC and AC timing data

# AL4CS211/AL4CS221/AL4CS231/AL4CS241/ AL4CS251 (512 x9, 1k x9, 2k x9, 4k x9, 8k x9) Synchronous FIFO

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## 1.0 Description

The AL4CS211/AL4CS221/AL4CS231/AL4CS241/AL4CS251 series memory products are high-performance, low-power 9-bit read/write FIFO (First-In-First-Out) memory chips. They are specially designed to buffer high speed streaming data for a wide range of communication applications, such as optical disk controllers, Local Area Networks (LANs), SONET (Synchronous Optical Network).

The input data is synchronous with a free-running clock (WCLK), and input-enable pins (/WEN1, /WEN2). Data is written into the FIFO on every clock when enable pins are asserted. The output is synchronous with the other free-running clock (RCLK) and enables (/REN1, /REN2). An Output Enable pin (/OE) is provided at the read port for tri-state control of the output port. The FIFOs can output two fixed flags, Empty Flag (/EF) and Full Flag (/FF), and two programmable flags, Almost-Empty (/PAE) and Almost-Full (/PAF). The offsets of the /PAE and /PAF flags are loaded when Load pin (/LD) goes low.

## 2.0 Features

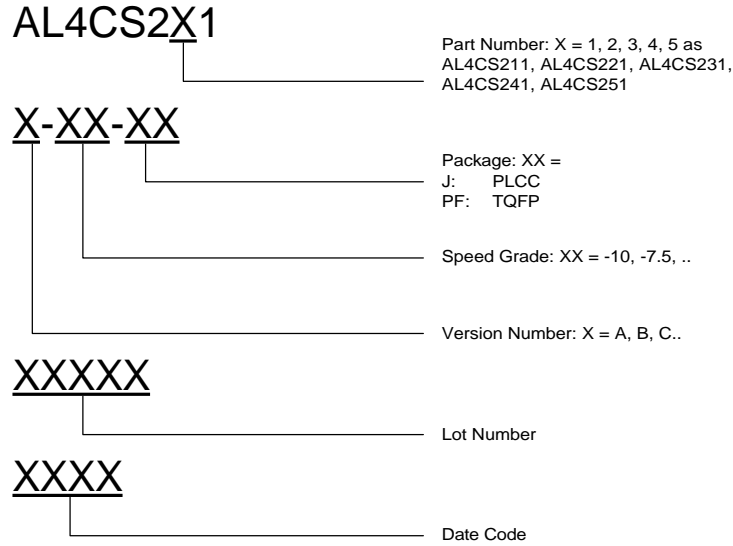
- 512 x9-bit cell array (AL4CS211)
- 1,024 x9-bit cell array (AL4CS221)
- 2,048 x9-bit cell array (AL4CS231)
- 4,096 x9-bit cell array (AL4CS241)
- 8,192 x9-bit cell array (AL4CS251)
- 100/133 MHz Operation
- 10/7.5 ns read/write cycle time
- Independent Read and Write operations
- Empty and Full flags support
- Programmable Almost-Empty and Almost-Full flags
- Output enable (data skipping)
- 3.3V power supply with 5V tolerant
- Available in a 32-pin Thin Quad Flat Pack (TQFP) and 32-pin plastic leaded chip carrier (PLCC) packages

## 3.0 Applications

- Routers
- ATM switches
- Cable modems
- Wireless base stations
- SONET(Synchronous Optical Network) multiplexers
- Multimedia systems
- Time base correction (TBC)

## 4.0 Chip Information

### 4.1 Marking Information



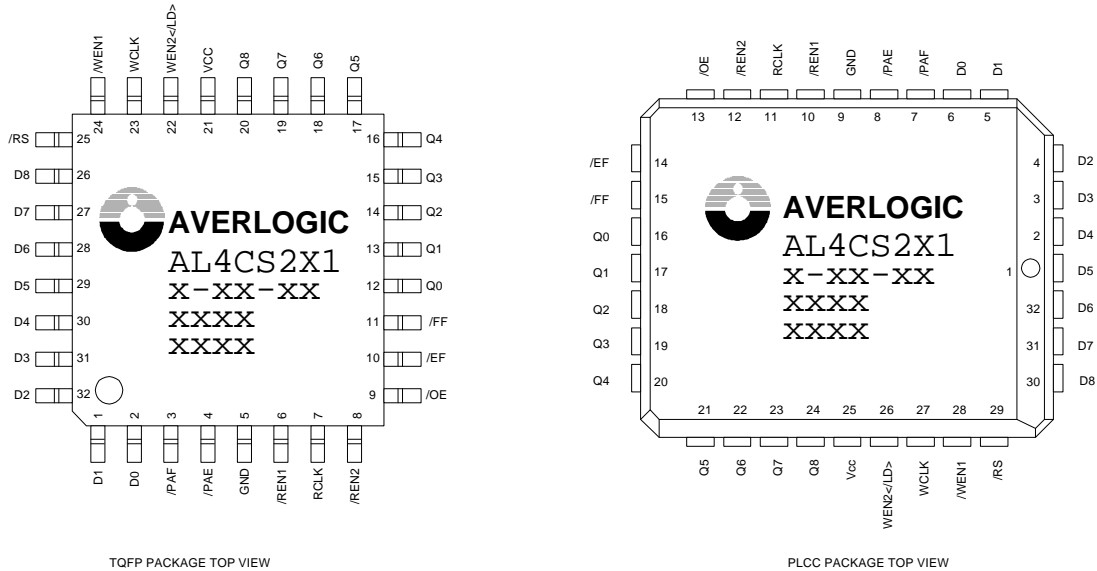
### 4.1 Ordering Information

The ordering information for AL4CS211/AL4CS221/AL4CS231/AL4CS241/AL4CS251 are:

Part number	Package	Power Supply	Status
AL4CS211/221/231/241/251(A-10-PF)	32-pin plastic TQFP(7x7mm)	+3.3V±10%	Sample in Aug., 2001
AL4CS211/221/231/241/251(A-7.5-PF)	32-pin plastic TQFP(7x7mm)	+3.3V±10%	Sample in Aug., 2001
AL4CS211/221/231/241/251(A-10-J)	32-pin plastic PLCC	+3.3V±10%	Sample in Aug., 2001
AL4CS211/221/231/241/251(A-7.5-J)	32-pin plastic PLCC	+3.3V±10%	Sample in Aug., 2001

## 5.0 Pin-out Diagram

The AL4CS211/AL4CS221/AL4CS231/AL4CS241/AL4CS251 pin-out diagram is following:



## 6.0 Block Diagram

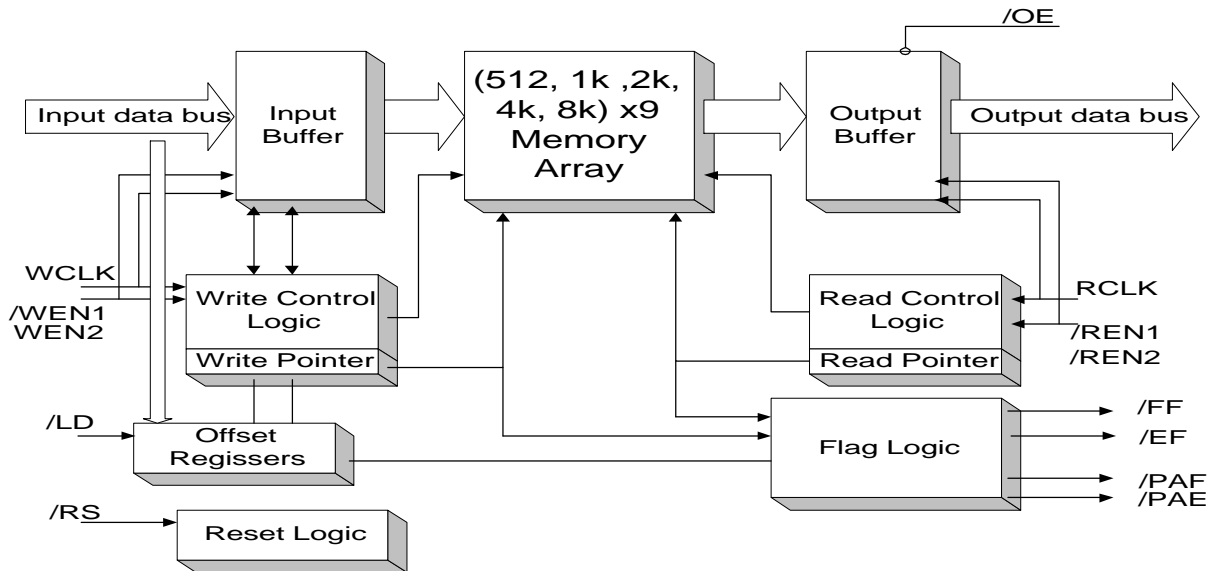


Figure 1. AL4CS2x1 FIFO Block Diagram

The internal structure of the AL4CS211/AL4CS221/AL4CS231/AL4CS241/AL4CS251 consists of Input/Output buffers, Read/Write Control Logic and main (512, 1k, 2k, 4k, 8k) x9 different configuration memory cell array and state-of-the-art logic design that takes care of addressing and controlling the read/write data.

## 7.0 Pin Definition and Description

The pin-out definition and function are described as following:

### Write Bus Signals

Pin Symbol	Pin name	TQFP Pin no.	PLCC Pin no.	I/O Typ	Description
D[8:0]	Data Inputs	[26:32], 1, 2	[30:32], [1:6]	I	9-bit input data bus.
/WEN1	Write Enable	24	28	I	/WEN1 is the only Write Enable pin, if FIFO is configured to support programmable flags. When /WEN1 is LOW, data is written into the FIFO on every rising edge of WCLK. If the FIFO is configured to have two write enables, /WEN1 must be LOW and WEN2 must be HIGH to write data into the FIFO. When FIFO is full (/FF = LOW), data will not be written into FIFO.
WEN2 </LD>	Write Enable	22	26	I	The FIFO is configured at the Reset to either have two write enables or support programmable flags. If Write Enable 2<Load> (WEN2</LD>) is HIGH at Reset (/RS = LOW), this pin will operate as a second Write Enable pin. If Write Enable 2<Load> (WEN2</LD>) is LOW at Reset (/RS = LOW), the FIFO is configured to support programmable flags function and /WEN1 is the only Write Enable pin.
WCLK	Write Clock	23	27	I	Data is written into the FIFO on a rising edge of WCLK when the Write Enable(s) are asserted. Data will not be written into FIFO if /FF is not LOW.

### Read Bus Signals

Pin symbol	Pin name	TQFP Pin no.	PLCC Pin no.	I/O typ	Description
Q[8:0]	Data Outputs	[21:12]	[24:16]	O	9-bit output data bus.
/REN1	Read Enable	6	10	I	When both /REN1 and /REN2 are LOW, data is read from the FIFO on every rising edge of RCLK. Data will not be read from the FIFO if the /EF is LOW.

/REN2	Read Enable	8	12	I	When /REN1 and /REN2 are LOW, data is read from the FIFO on every rising edge of RCLK. Data will not be read from the FIFO if the /EF is LOW.
/OE	Output Enable	9	13	I	When /OE is LOW, the data output bus is active. If /OE is HIGH, the output data bus will be in high-impedance.
RCLK	Read Clock	7	11	I	Data is read from the FIFO on a rising edge of RCLK when /REN1 and /REN2 are LOW, and if the FIFO is not empty.

### Miscellaneous & Flags Signals

Pin Symbol	Pin name	TQFP Pin no.	PLCC Pin no.	I/O typ	Description
/RS	Reset	25	29	I	When /RS is set LOW, internal read and write pointers are set to the first location of the RAM array, /FF and /PAF go HIGH, and /PAE and /EF go LOW. A reset is required before an initial WRITE after power-up.
/FF	Full Flag	11	15	O	/FF indicates whether or not the FIFO memory is full.
/EF	Empty Flag	10	14	O	/EF indicates whether or not the FIFO memory is empty.
/PAE	Programmable Almost-Full Flag	4	8	O	When /PAE is LOW, the FIFO is Almost-Empty based on the offset programmed into the FIFO.
/PAF	Programmable Almost-Full Flag	3	7	O	When /PAF is LOW, the FIFO is Almost-Full based on the offset programmed into the FIFO.

### Power/Ground Signals

Pin Symbol	Pin name	TQFP Pin no.	PLCC Pin no.	I/O typ	Description
VCC	Power	21	25	-	3.3V ± 10% power supply
GND	Ground	5	9	-	Ground.

## 8.0 Memory Operations

### 8.1 Inputs and Outputs

#### 8.1.1 DATA INPUTS (D8 - D0)

D8 ~ D0 are 9-bit wide of input data port.



### 8.1.2 DATA OUTPUTS (Q8-Q0)

Q8 ~ Q0 are 9-bit wide of output data port.

## 8.2 Controls

### 8.2.1 Reset (/RS)

Reset takes place when the Reset (/RS) input is LOW. During reset, both internal read and write pointers are set to the starting position. A reset is required to initial internal logic after power-up. The Full Flag (/FF) and Programmable Almost-Full Flag (/PAF) will be reset to HIGH after  $t_{RSF}$ . The Empty Flag (/EF) and Programmable Almost-Empty Flag (/PAE) will be reset to LOW after  $t_{RSF}$ . During reset, the output register is initialized to all zeros and the offset registers are initialized to their default values.

### 8.2.2 Write Clock (WCLK)

A write cycle is initiated on the rising edge of the Write Clock (WCLK). Data setup and hold times must be met with respect to the rising edge of WCLK. The Full Flag (/FF) and Programmable Almost-Full Flag (/PAF) are synchronized with respect to the rising edge of the Write Clock (WCLK). The Write and Read Clocks can be asynchronous or coincident.

### 8.2.3 Write Enable1 (/WEN1)

If the FIFO is configured to support programmable flags, Write Enable 1 (/WEN1) is the only enable control pin. In this configuration, when Write Enable 1 (/WEN1) is low, data can be written into the input register and memory array on the rising edge of every Write Clock (WCLK). Data is stored in the memory array sequentially and independently of any on going read operation. When Write Enable 1 (/WEN1) is HIGH, the input holds the previous data and no new data can be written into the memory array. If the FIFO is configured to have two write enables, which allows for depth expansion, two enable control pins are involved in the write operations. Please refer Write Enable 2 (WEN2) section for details. To prevent data overflow, the Full Flag (/FF) will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, the Full Flag (/FF) will go HIGH after  $t_{WFF}$ , allowing a valid write to begin. Write Enable(s) are ignored when the FIFO is full.

### 8.2.4 Read Clock (RCLK)

Data can be read on the outputs on the rising edge of the Read Clock (RCLK), when all the output controls /REN1, /REN2, Output Enable (/OE) are set LOW. The Empty Flag (/EF) and Programmable Almost-Empty Flag (/PAE) are synchronized with respect to the rising edge of the Read Clock (RCLK). The Write and Read Clocks can be asynchronous or coincident.

### 8.2.5 Read Enable (/REN1, /REN2)

When both Read Enables (/REN1, /REN2) are LOW, data is read from the memory array to the output register on the rising edge of the Read Clock (RCLK). When either Read Enable (/REN1, /REN2) is HIGH, the output register holds the previous data and no new data can to be loaded into the register. When all the data has been read from the FIFO, the Empty Flag (/EF) will go LOW, inhibiting further read operations. Once a valid write operation has been done, the Empty Flag (/EF) will go HIGH after  $t_{REF}$  and a valid read can begin. The Read Enables (/REN1, /REN2) are ignored when the FIFO is empty.

### 8.2.6 Output Enable (/OE)

When Output Enable (/OE) is enabled (LOW), the parallel output buffers receive data from the output register. When /OE is disabled (HIGH), the Q8 ~ Q0 output data bus is in a high-impedance state.

### 8.2.7 Write Enable2 & /LD (WEN2</LD>)

This is a dual-purpose pin. The FIFO can be configured at Reset to have programmable flags or to have two write enables, which allows depth expansion.

## 2 Write Enable Configuration

If Write Enable 2<Load> (WEN2</LD>) is set high at Reset (/RS = LOW), this pin operates as a second Write Enable pin. In this configuration, when Write Enable (/WEN1) is LOW and Write Enable 2<Load> (WEN2</LD>) is HIGH, data can be written into the FIFO on the rising edge of every Write Clock (WCLK). Data is stored in FIFO sequentially and independently of any on-going read operation. When Write Enable (/WEN1) is HIGH and/or Write Enable 2<Load> (WEN2</LD>) is LOW, the input register holds the previous data and no new data is allowed to be written into the FIFO. To prevent data overflow, the Full Flag (/FF) will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, the Full Flag (/FF) will go HIGH after  $t_{WFF}$ , allowing a valid write to begin. Write Enable 1 (/WEN1) and Write Enable 2<Load> (WEN2</LD>) are ignored when the FIFO is full.

### Single Write Enable and Programmable Flags Support Configuration

The FIFO is configured to have programmable flags when the Write Enable2<Load> (WEN2</LD>) is set to LOW at Reset (/RS = LOW). The AL4CS211/221/231/241/251 devices contain four 8-bit offset registers, which can be loaded with data on the inputs, or read from the outputs. See following table for details of the size of the registers and the default values.

	1 <sup>st</sup> word	2 <sup>nd</sup> word	3 <sup>rd</sup> word	4 <sup>th</sup> word
AL4CS211	[7:0] Empty Offset (LSB) Default = 07h	[0] Empty Offset (MSB) Default = 0b	[7:0] Full Offset (LSB) Default = 07h	[0] Full Offset (MSB) Default = 0b
AL4CS221	[7:0] Empty Offset (LSB) Default = 07h	[1:0] Empty Offset (MSB) Default = 00b	[7:0] Full Offset (LSB) Default = 07h	[1:0] Full Offset (MSB) Default = 00b
AL4CS231	[7:0] Empty Offset (LSB) Default = 07h	[2:0] Empty Offset (MSB) Default = 000b	[7:0] Full Offset (LSB) Default = 07h	[2:0] Full Offset (MSB) Default = 000b
AL4CS241	[7:0] Empty Offset (LSB) Default = 07h	[3:0] Empty Offset (MSB) Default = 0000b	[7:0] Full Offset (LSB) Default = 07h	[3:0] Full Offset (MSB) Default = 0000b
AL4CS251	[7:0] Empty Offset (LSB) Default = 07h	[4:0] Empty Offset (MSB) Default = 00000b	[7:0] Full Offset (LSB) Default = 07h	[4:0] Full Offset (MSB) Default = 00000b

In this configured, when the Write Enable1 (/WEN1) and Write Enable 2<Load> (WEN2</LD>) are set LOW, data on the inputs D8 ~ D0 is written into the Empty (Least Significant Bit) Offset register on the first rising edge of the Write Clock (WCLK). Data is written into the Empty (Most Significant Bit) Offset register on the second rising edge of the Write Clock (WCLK), into the Full (Least Significant Bit) Offset register on the third transition, and into the Full (Most Significant Bit) Offset register on the fourth transition. The fifth transition of the Write Clock (WCLK) again writes to the Empty (Least Significant Bit) Offset register.

However, writing all offset registers does not have to occur consecutively. The FIFO can return to normal read/write operation by bringing the Write Enable 2<Load> (WEN2</LD>) pin HIGH after one or two offset registers can be written. When the Write Enable 2/Load (WEN2/LD) pin is set LOW again, and Write Enable 1 (/WEN1) is LOW, the next offset register in sequence is written. The contents of the offset registers can be read on the output lines when the Write Enable 2<Load> (WEN2</LD>) pin is set low and both Read Enables (/REN1, /REN2) are LOW. Data can be read on the rising edge of the Read Clock (RCLK). A read and write to the offset registers should not be performed simultaneously.

## 8.3 Flags

### 8.3.1 Full Flag (/FF)

The Full Flag (/FF) will go LOW, inhibiting further write operation, when the device is full. If no reads are performed after Reset (/RS), the Full Flag (/FF) will go LOW after 512 writes for the AL4CS211, 1,024 writes for the AL4CS221, 2,048 writes for the AL4CS231, 4,096 writes for the AL4CS241 and 8,192 writes for the AL4CS251. The Full Flag (/FF) is synchronized with respect to the rising edge of the Write Clock (WCLK).

### 8.3.2 Empty Flag (/EF)

The Empty Flag (/EF) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating the device is empty. The Empty Flag (/EF) is synchronized with respect to the rising edge of the Read Clock (RCLK).

### 8.3.3 Programmable Almost- Full Flag (/PAF)

The Programmable Almost-Full flag (/PAF) will go LOW when the FIFO reaches the almost-full condition. If no reads are performed after Reset (/RS), the Programmable Almost-Full flag (/PAF) will go LOW after (512-m) writes for the AL4CS211, (1,024-m) writes for the AL4CS221, (2,048-m) writes for the AL4CS231, (4,096-m) writes for the AL4CS241 and (8,192-m) writes for the AL4CS251. The offset "m" is defined in the Full Offset registers. If there is no full offset specified, the Programmable Almost-Full flag (/PAF) will go LOW at Full-7 words. The Programmable Almost-Full flag (/PAF) is synchronized with respect to the rising edge of the Write Clock (WCLK).

### 8.3.4 Programmable Almost-Empty Flag (/PAE)

The Programmable Almost-Empty flag (/PAE) will go LOW when the read pointer is "n+1" locations less than the write pointer. The offset "n" is defined in the Empty Offset registers. If no reads are performed after Reset the Programmable Almost-Empty flag (/PAE) will go HIGH after "n+1" for the AL4CS211/221/231/241/251. If there is no empty offset specified, the Programmable Almost-Empty flag (/PAE) will go LOW at Empty+7 words. The Programmable Almost-Empty flag (/PAE) is synchronized with respect to the rising edge of the Read Clock (RCLK).

## 9.0 Multiple Devices Bus Expansion and Cascading

### 9.1 Width Expansion Configuration

Simply connecting the corresponding input controls signals of multiple devices may increase data bus width. A composite flag should be created for each of the end-point status flags (/EF and /FF). The partial status flags (/PAE and /PAF) can be detected from any one device. Figure 15 demonstrates an 18-bit word width data bus by using two AL4CS211/221/231/241/251s. Any word width expansion can be attained by adding additional AL4CS211/221/231/241/251s. When these devices are in a Width Expansion Configuration, the Read Enable 2 (/REN2) control input can be grounded (see Figure 15). In this configuration, the Write Enable 2<Load> (WEN2<LD>) pin is set LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

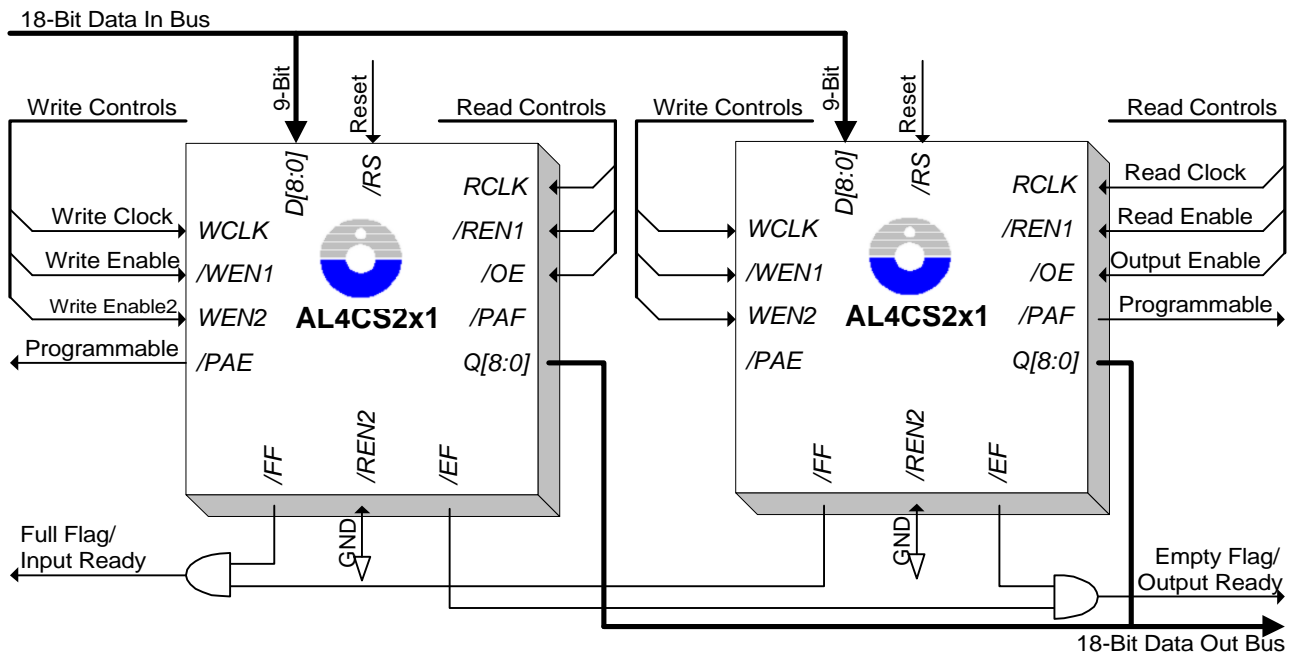


Figure 2. Multiple FIFO memory with programmable flags used in depth expansion configuration

### 9.2 Depth Expansion

The depth expansion of AL4CS211/221/231/241/251 is also possible. The existence of two enable pins on the read and write port allow depth expansion. The Write Enable 2<Load> pin is used as a second write enable in a depth expansion configuration thus the programmable flags are set to the default values. Depth expansion is possible by using one enable input for system control while the other enable input is controlled by expansion logic to direct the flow of data. A typical application would have the expansion logic alternate data access from one device to the next in a sequential manner. These FIFOs operate in the Depth Expansion configuration when the following conditions are met:

1. The WEN2</LD> pin is held HIGH during Reset so that this pin operates a second Write Enable.
2. External logic is used to control the flow of data.

## 10.0 Electrical Characteristics

### 10.1 Absolute Maximum Ratings

Parameter	3.3V Rating	Unit
V <sub>DD</sub> Supply Voltage	-0.3 ~ +3.8	V
V <sub>P</sub> Pin Voltage	-0.3 ~ +(V <sub>DD</sub> +0.3)	V
I <sub>O</sub> Output Current	-20 ~ +20	mA
T <sub>AMB</sub> Ambient Op. Temperature	0 ~ +85	°C
T <sub>stg</sub> Storage temperature	-40 ~ +125	°C

### 10.2 Recommended Operating Conditions

Parameter	3.3V Rating			Unit
	Min	Typ	Max	
V <sub>DD</sub> Supply Voltage	+3.0	+3.3	+3.6	V
V <sub>IH</sub> High Level Input Voltage	0.7 V <sub>DD</sub>		V <sub>DD</sub>	V
V <sub>IL</sub> Low Level Input Voltage	0		0.3 V <sub>DD</sub>	V

### 10.3 DC Characteristics

(V<sub>DD</sub> = 3.3V, V<sub>SS</sub>=0V, T<sub>AMB</sub> = 0 to 70°C)

Parameter		3.3V Rating			Unit
		Min	Typ	Max	
I <sub>DD</sub>	Operating Current @20MHz	-	-	16	mA
I <sub>DDs</sub>	Standby Current	-	1.8	5	mA
V <sub>OH</sub>	Hi-level Output Voltage	2.4	-	V <sub>DD</sub>	V
V <sub>OL</sub>	Lo-level Output Voltage	-	-	+0.4	V
I <sub>LI</sub>	Input Leakage Current	-2	-	+2	μA
I <sub>LO</sub>	Output Leakage Current	-10	-	+10	μA

Note: The Operating Current is tested at RCLK=WCLK=20MHz and data inputs switch at 10MHz

## 10.4 AC Electrical Characteristics

( $V_{DD} = 3.3V$ ,  $V_{SS} = 0V$ ,  $T_{AMB} = 0$  to  $70^{\circ}C$ )

Symbol	Parameter	100Mhz		133Mhz		Unit
		Min	Max	Min	Max	
$t_S$	Clock Cycle Frequency	-	100	-	133	MHz
$t_A$	Data Access Time	2	7.5	2	5	ns
$t_{CLK}$	Clock Cycle Time	10	-	7.5	-	ns
$t_{CLKH}$	Clock HIGH Time	4.5	-	3.5	-	ns
$t_{CLKL}$	Clock LOW Time	4.5	-	3.5	-	ns
$t_{DS}$	Data Setup Time	3	-	2.5	-	ns
$t_{DH}$	Data Hold Time	0.5	-	0.5	-	ns
$t_{ENS}$	Enable Setup Time	3	-	2.5	-	ns
$t_{ENH}$	Enable Hold Time	0.5	-	0.5	-	ns
$t_{RS}$	Reset Pulse Width	10	-	7.5	-	ns
$t_{RSS}$	Reset Setup Time	8	-	6	-	ns
$t_{RSR}$	Reset Recovery Time	8	-	6	-	ns
$t_{RSF}$	Reset to Flag and Output Time	-	10	-	9	ns
$t_{OLZ}$	Output Enable to Output in Low-Z	0	-	0	-	ns
$t_{OE}$	Output Enable to Output Valid	-	6	-	5	ns
$t_{OHZ}$	Output Enable to in High-Z	-	6	-	5	ns
$t_{WFF}$	Write Clock to Full Flag	-	7	-	5	ns
$t_{REF}$	Read Clock to Empty Flag	-	7	-	5	ns
$t_{AF}$	Write Clock to Almost-Full Flag	-	7	-	5	ns
$t_{AE}$	Read Clock to Almost-Empty Flag	-	7	-	5	ns
$t_{SKEW1}$	Skew time between Read Clock & Write Clock for /FF & /EF	5	-	3	-	ns
$T_{SKEW2}$	Skew time between Read Clock & Write Clock for /PAE and /PAF	10	-	8	-	ns

### 10.5 Timing Diagrams

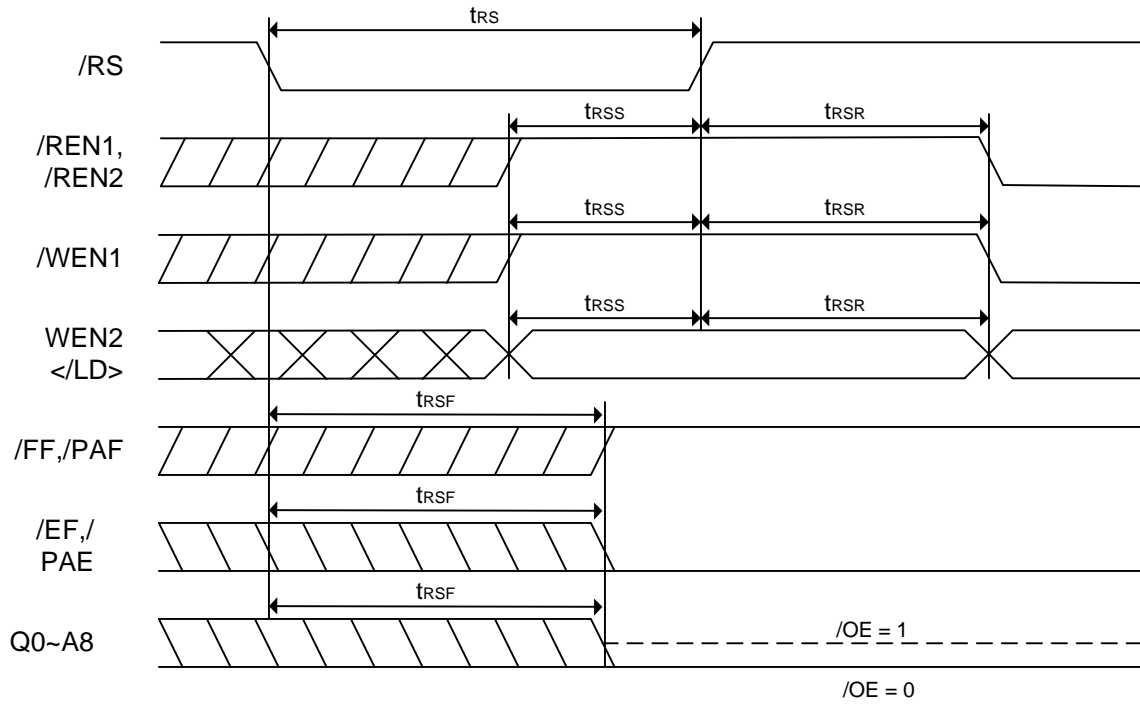


Figure 3. Reset Timing



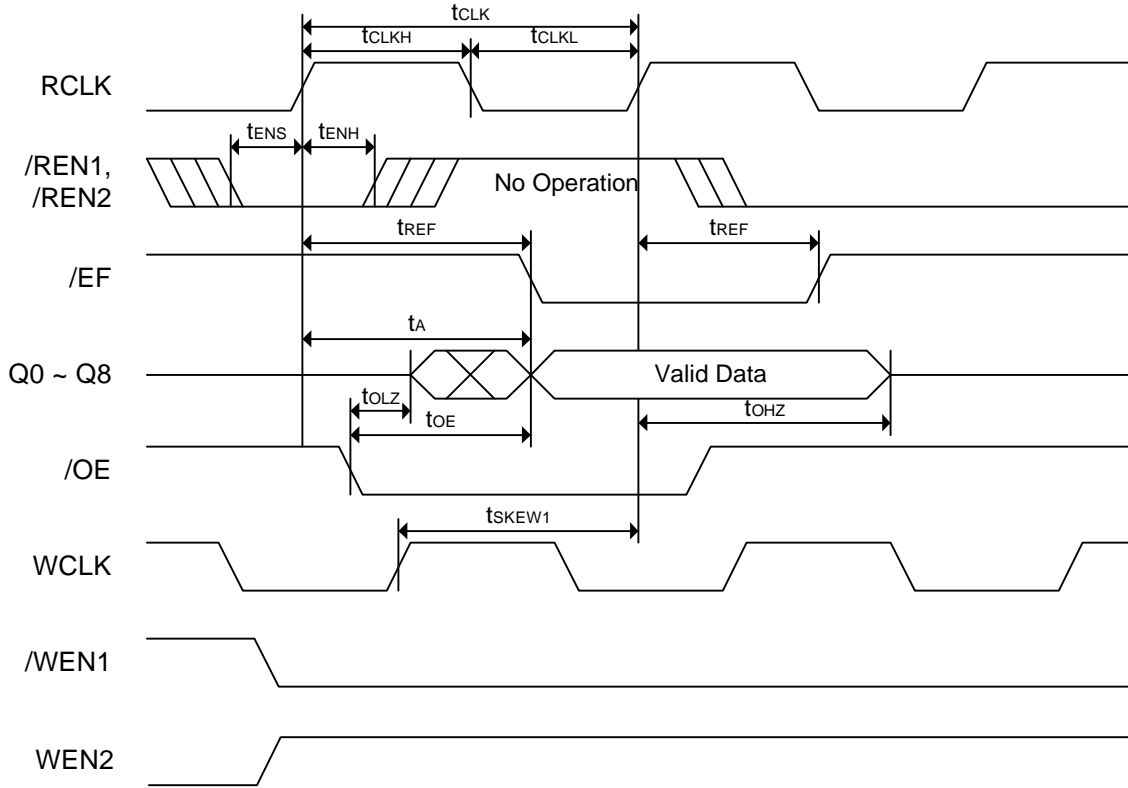


Figure 4. Read Cycle Timing

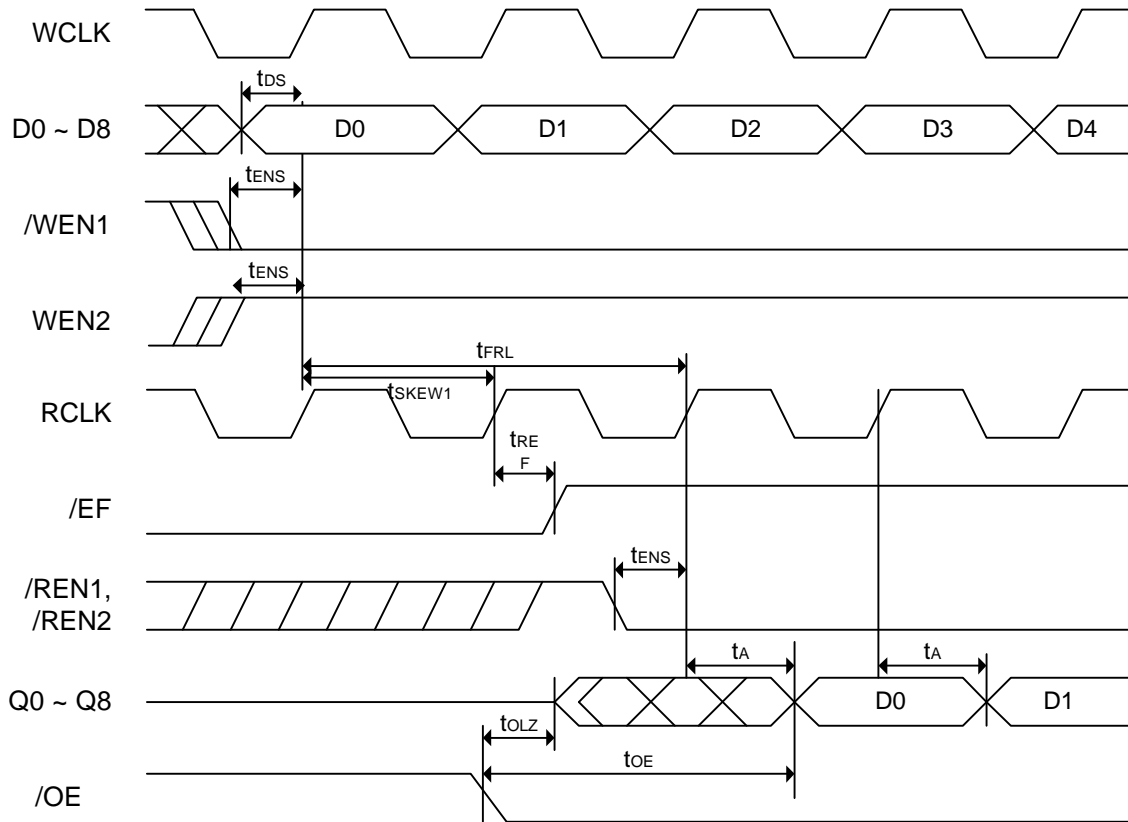


Figure 5. First Data Word Latency Timing

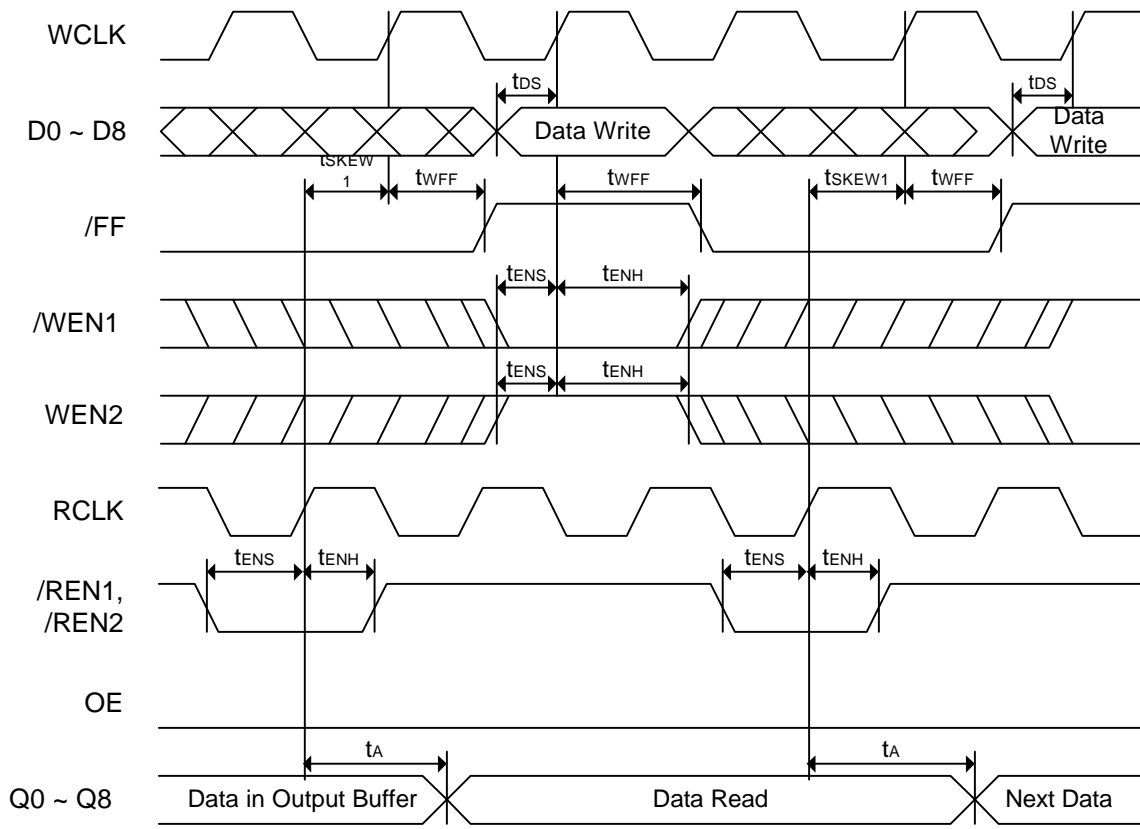


Figure 6. Full Flag Timing

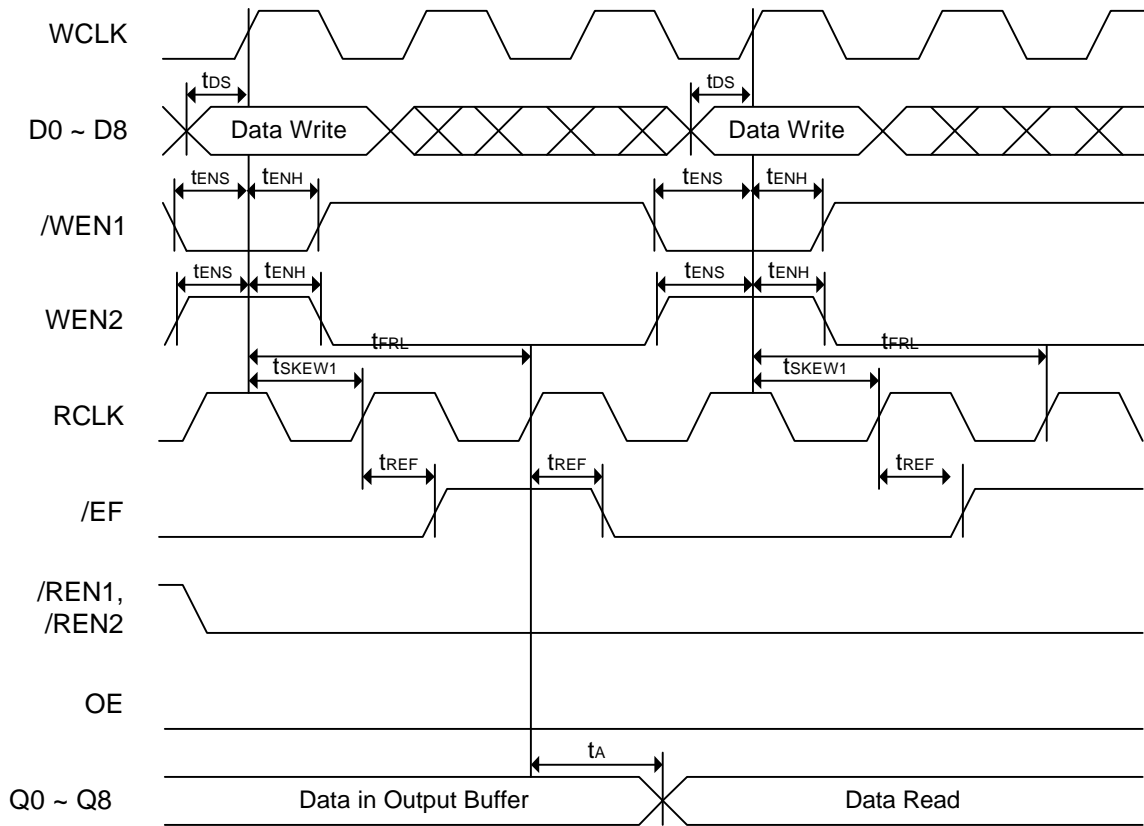


Figure 7. Empty Flag Timing

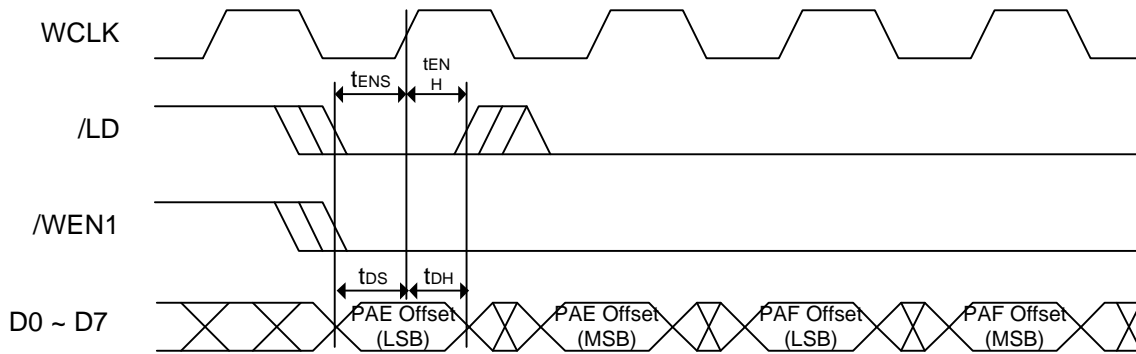


Figure 8. Write Offset Registers

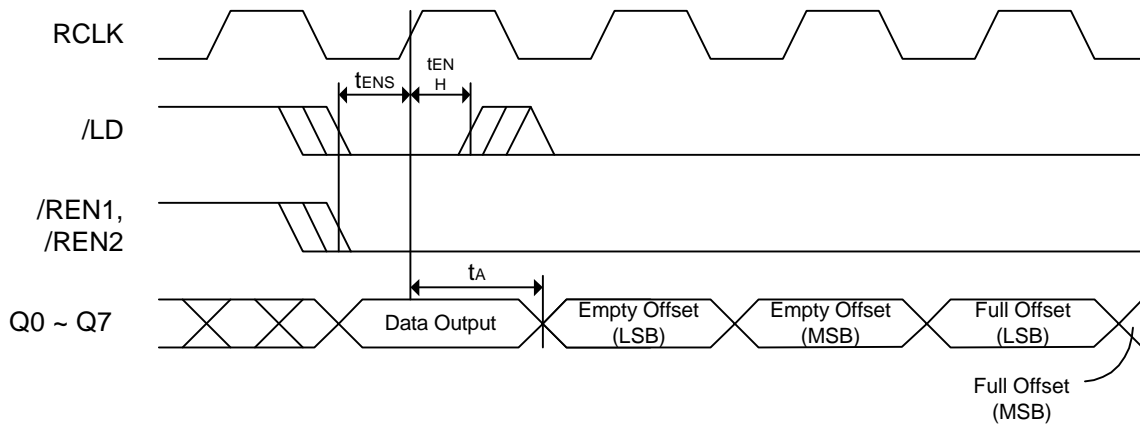


Figure 9. Read Offset Registers Timing

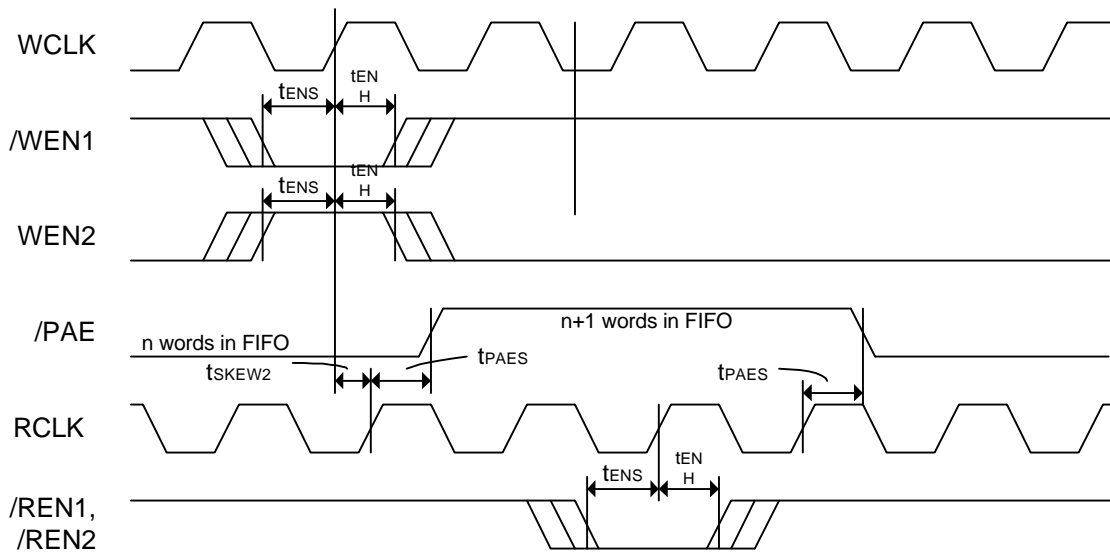


Figure 10. Programmable Empty Flag Timing

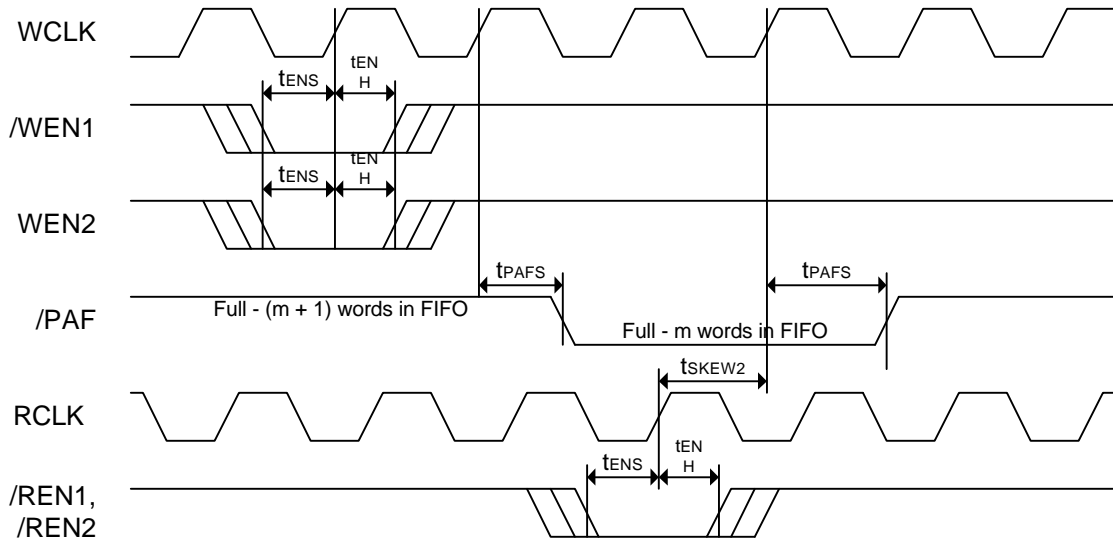
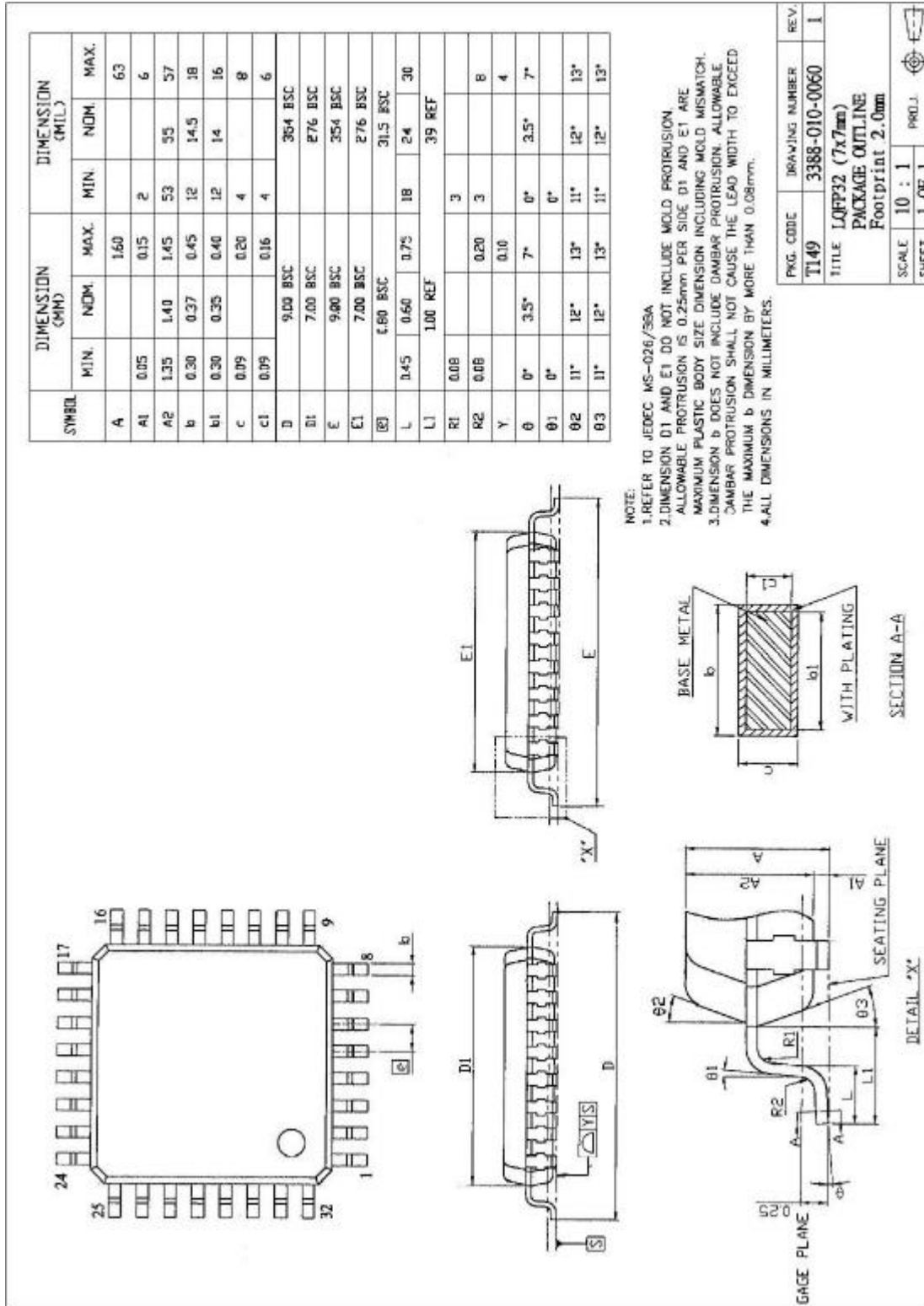


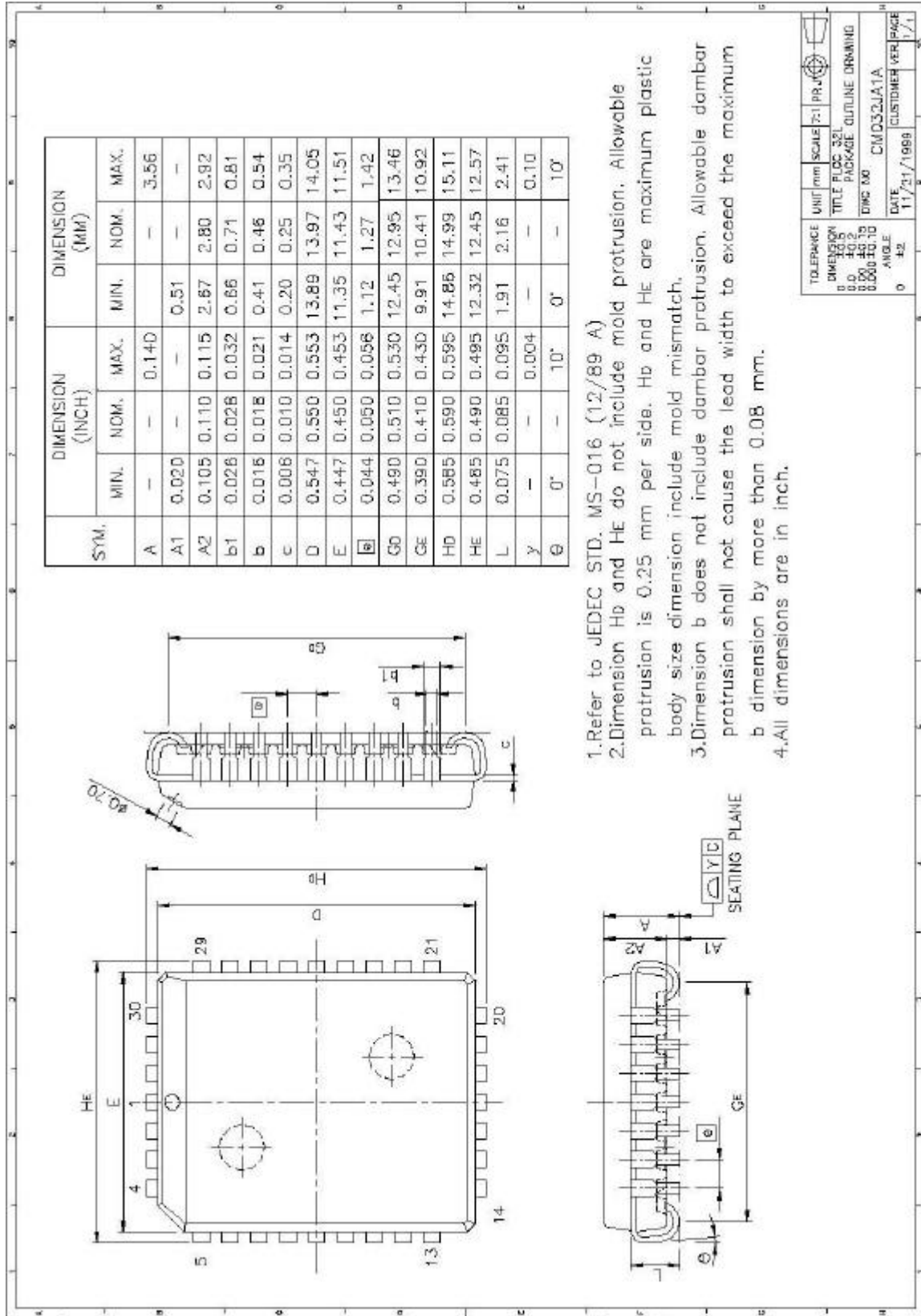
Figure 11. Programmable Full Flag Timing

# 11.0 Mechanical Drawing

## 11.1 7x7mm 32-pin TQFP Package



# 11.2 32-pin PLCC Package



1. Refer to JEDEC STD. MS-016 (12/89 A)
2. Dimension Hb and HE do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Hb and He are maximum plastic body size dimension include mold mismatch.
3. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm.
4. All dimensions are in inch.

TOLERANCE	UNIT	SCALE	7:1	PRJ
DIMENSION	0.005			
ANGLE	0			
TITLE FLOC 32L PACKAGE OUTLINE DRAWING				
DWG NO CVD32JA1A				
DATE 11/21/1989				
CUSTOMER REFERENCE				



## CONTACT INFORMATION

AverLogic Technologies, Inc.  
90 Great Oaks Blvd. #204  
San Jose, CA 95119  
USA

Tel : +1408 361-0400  
Fax : +1408 361-0404  
E-mail : sales@averlogic.com  
URL : [www.averlogic.com](http://www.averlogic.com)

AverLogic Technologies, Corp.  
4F., No.514, Sec.2, Cheng Kung Rd.,  
Nei-Hu Dist., Taipei, Taiwan  
R.O.C

Tel : +886 2-27915050  
Fax : +886 2-27912132  
E-mail : sales@averlogic.com.tw  
URL : [www.averlogic.com.tw](http://www.averlogic.com.tw)