TriQuint SEMICONDUCTOR

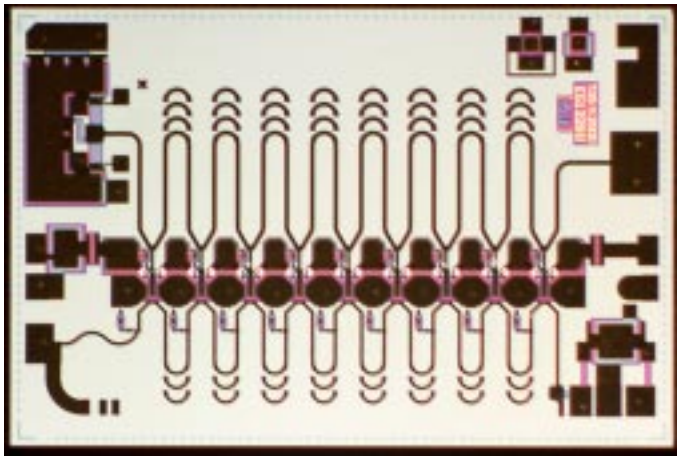
Product Data Sheet

January 24, 2005

DC-18GHz MPA with AGC

TGA1328-SCC

OC-192 12.5GB/s LN/MZ Driver and Receive AGC Applications



Key Features and Performance

- 0.5um pHEMT Technology
- DC - 14GHz Linear Bandwidth
- DC -18GHz Saturated Power BW
- 16dB Small Signal Gain
- 6dB AGC Range
- 20ps Edge Rates (20/80)
- 8Vpp 12.5Gb/s NRZ PRBS
- 4dB Noise Figure @ 10GHz
- Low power dissipation
- Chip Dimensions 3.4mm x 2.3mm

Description

The TriQuint TGA1328-SCC is a medium power wideband AGC amplifier that typically provides 12dB saturated gain with 6dB AGC range. Typical input and output return loss is >10dB. Typical Noise Figure is 2.5dB at 3GHz. Minimum saturated output power is 25dBm. Small signal BW is near 14GHz with saturated power performance to 18GHz. RF ports are DC coupled enabling the user to customize system corner frequencies.

The TGA1328-SCC is an excellent choice for 9.9, 10.7, and 12.5Gb/s NRZ applications driving a Lithium Niobate Optical Modulator with electrical Non-Return-to-Zero (NRZ) data. In addition it may be used as a receive AGC amplifier.

Drain bias may be applied thru the on-chip drain termination resistor for low drive applications or thru the RF output port for high drive applications.

The TGA1328-SCC requires off-chip decoupling and blocking components. Each device is 100% DC and RF tested on-wafer to ensure performance compliance.

The TGA1328SCC is available in chip form or assembled into a surface mount package (see the TGA8652-EPU data sheet for more information on the SMT package).

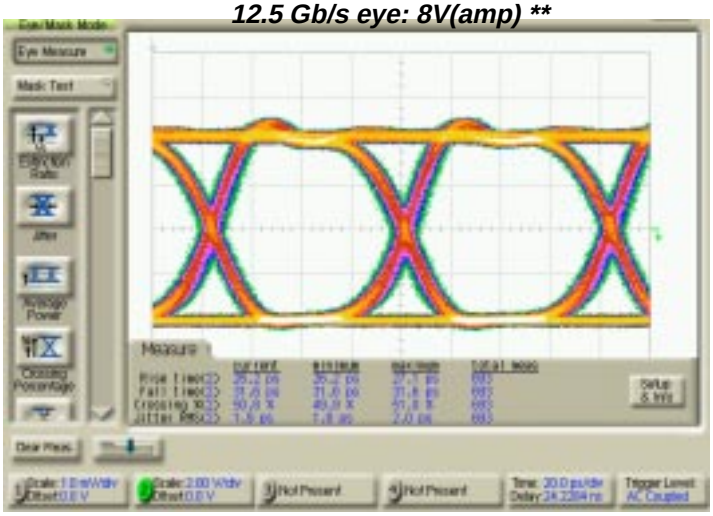
Primary Applications

- 12.5GBit OC192 LN/MZ Driver
- 12.5GBit OC192 AGC Receive

Measured 12.5Gb/s Performance

12.5Gb/s NRZ 2^31-1 ***Single Stage***

12.5 Gb/s eye: 8V(amp) **



***** Input 12.5Gb/s data stream generated using an Anritsu PPG (Vin=2Vpp).***

MAXIMUM RATINGS

SYMBOL	PARAMETER 6/	VALUE	NOTES
	POSITIVE SUPPLY VOLTAGE		
V^+	Biased thru On-chip Drain Termination	12 V	
Vd(FET)	Biased thru the RF Output Port using a Bias Tee	10 V	
	POSITIVE SUPPLY CURRENT		1/
I^+	Biased thru On-chip Drain Termination	110 mA	
Id	Biased thru the RF Output Port using a Bias Tee	250 mA	
P_d	POWER DISSIPATION	2.25 W	2/
	NEGATIVE GATE		
Vg	Voltage	0V to -3V	
Ig	Gate Current	5 mA	
	CONTROL GATE		
Vctl	Voltage	Vd/2 to -3V	3/
Ictl	Gate Current	5 mA	
	RF INPUT		
P_{IN}	Sinusoidal Continuous Wave Power	23 dBm	
V_{IN}	12.5Gb/s PRBS Input Voltage Peak to Peak	5 Vpp	
T_{CH}	OPERATING CHANNEL TEMPERATURE	150 ^{0}C	4/ 5/
T_M	MOUNTING TEMPERATURE (30 SECONDS)	320 ^{0}C	
T_{STG}	STORAGE TEMPERATURE	-65 to 150 ^{0}C	

Notes:

1/ Assure that the combination of Vd and Id does not exceed the maximum power dissipation rating.

2/ When operated at this bias condition with a base plate temperature of 70^{0}C, the median life is reduced from >1E8 to 2.4E6 hours.

3/ Assure that Vctl never exceeds Vd during bias up and down sequences. Also, assure that Vctl never exceeds 1.5V during normal operation.

4/ These ratings apply to each individual FET.

5/ Junction operating temperature will directly affect the device median time to failure (MTTF). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

6/ These ratings represent the maximum operable values for the device.

DC SPECIFICATIONS (100%)
(T_A = 25 °C ± 5 °C)

NOTES	SYMBOL	TEST CONDITIONS 2/	LIMITS		UNITS
			MIN	MAX	
	I_{DSS}	STD	110	516	mA
	I_{MAX}	STD	Infor. only	Infor. only	mA
	Gm	STD	241	581	mS
1/	$\|V_{P1}\|$	STD	0.5	1.5	V
1/	$\|V_{P2}\|$	STD	0.5	1.5	V
1/	$\|V_{BVGD}\|$	STD	13	30	V
1/	$\|V_{BVGS}\|$	STD	13	30	V
	R1,2	STD	30	45	Ohm
	R4	STD	35	56	Ohm

1/ V_P, V_{BVGD}, and V_{BVGS} are negative.

2/ The measurement conditions are subject to change at the manufacture's discretion

THERMAL INFORMATION*

Parameter	**Test Condition**	**P_{diss} (W)**	**T_{Base}** (°C)	**T_{CH} (°C)**	**$R_{\theta JC}$ (°C/W)**	**MTTF (HRS)**
$R_{\theta JC}$ Thermal Resistance (channel to backside of carrier)	Vd(FET)=6.5V, Vctl=1V Id=170mA +/-5%	1.1	70	103	30	>1E7
	V+ = 8 V**, V_{ctrl} = 1.5 V, Id = 80 mA ±5%	0.36	70	80	29	>1E8

Notes:

* Based on a detailed thermal model. Assumes worst case power dissipation condition where no RF is applied at the input (no power is dissipated in the load).

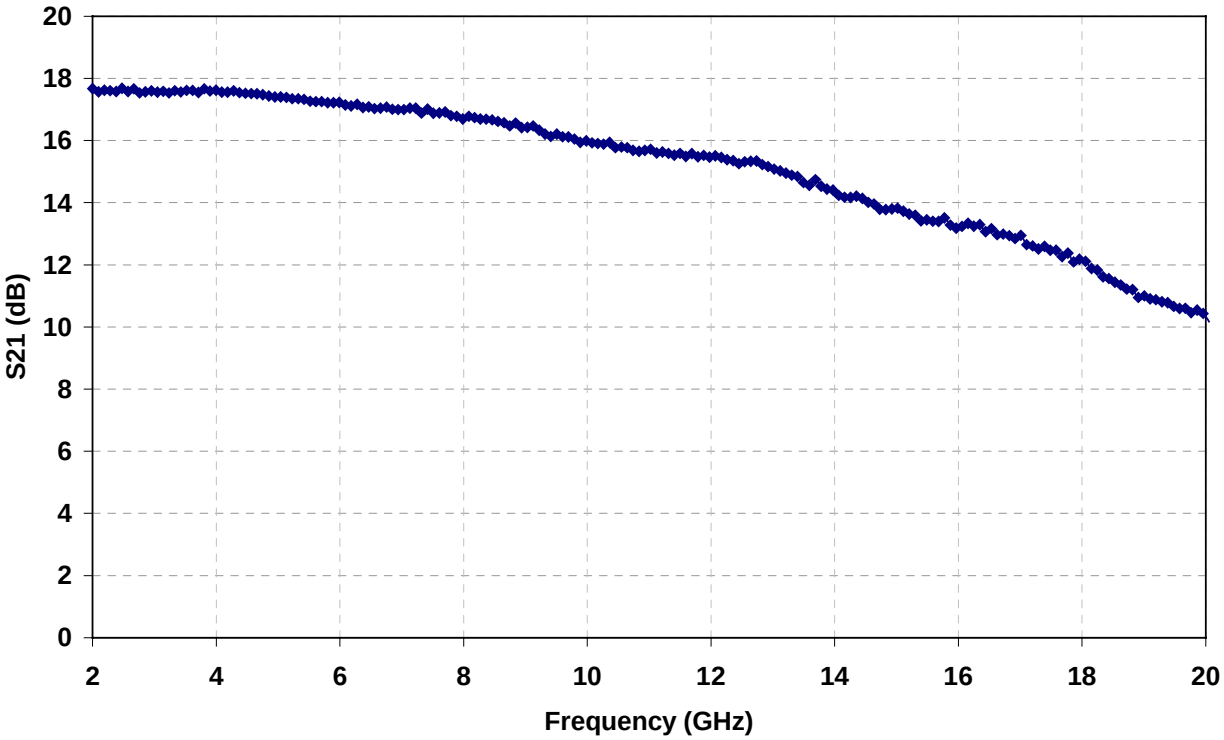
** When applying drain bias at V+, several volts are dropped across the internal drain terminations resistor (between V+ and Vd). For Id=80mA, approximately 3.5V is dropped across the drain termination resistor making Vd(FET)=4.5V. Total power dissipation in the FET is .36 watts.

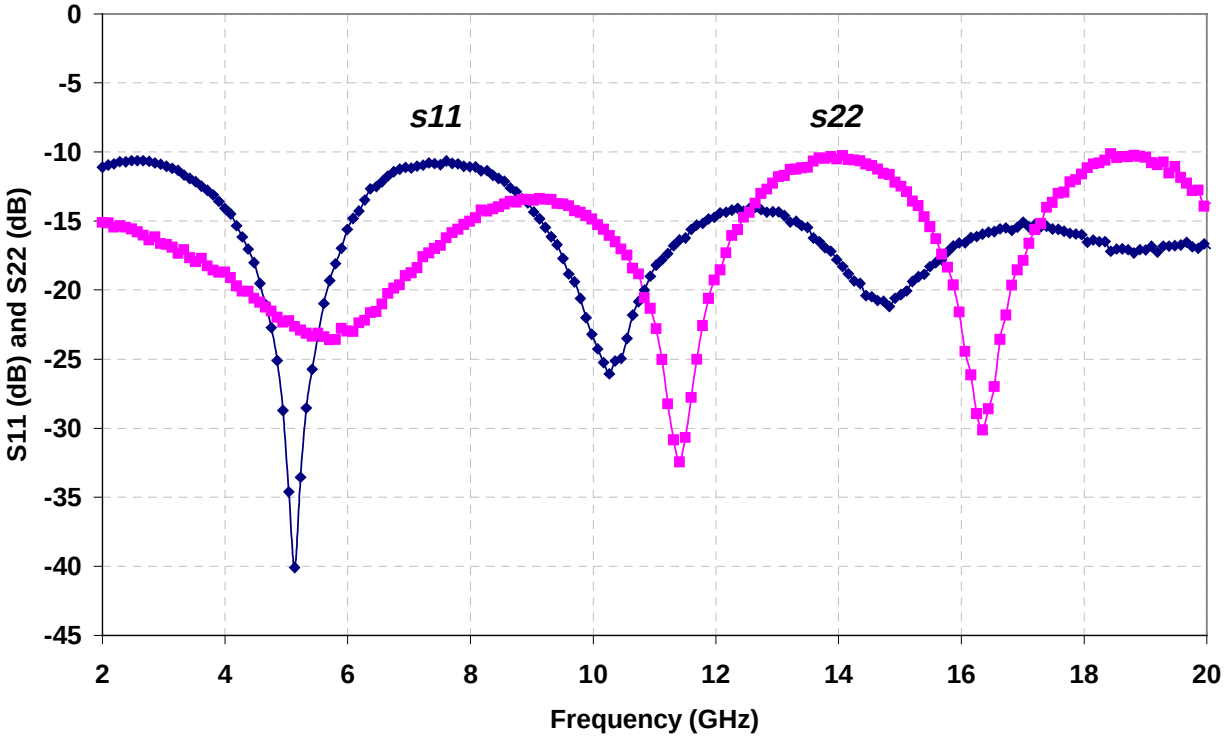
RF SPECIFICATIONS
(T_A = 25°C ± 5°C)

NOTE	TEST	MEASUREMENT CONDITIONS	VALUE			UNITS
			MIN	TYP	MAX	
	3dB BANDWIDTH			14		GHz
	SATURATED POWER BW			18		GHz
1/, 2/	SMALL-SIGNAL GAIN MAGNITUDE	2 and 4 GHz 6 GHz 10 GHz 14 GHz 18 GHz	16 15 14 13 11			dB
	SMALL SIGNAL AGC RANGE	Midband		6		dB
	NOISE FIGURE	3GHz		2.5		dB
	SATURATED OUTPUT VOLTAGE (EYE AMPLITUDE)	Vin=2Vpp at 12.5Gb/s PRBS	8			Vpp
1/, 3/	OUTPUT POWER @ PIN = 14dBm	2, 4, and 6 GHz	25			dBm
	INPUT RETURN LOSS MAGNITUDE	DC-10 GHz		-12		dB
	OUTPUT RETURN LOSS MAGNITUDE	DC-10 GHz		-12		dB
	ADDITIVE JITTER			< 2		pS
	GROUP DELAY	DC-10 GHz		+/- 20		pS
	RISE TIME			< 30		pS

Notes:
1/ Verified at RF on-wafer probe.
2/ S21Bias: V+=8V, adjust Vg1 to achieve Id=80mA+/-5%, Vg2=1.5V
Note: Drain bias is applied thru the on-chip drain termination resistor.
3/ Power Bias: Vtee=8V, adjust Vg1 to achieve Id=175mA+/-5%, Vg2=1.5V
Note: Drain bias is applied thru the RF output port using a bias tee, voltage is at the DC input to the bias tee.

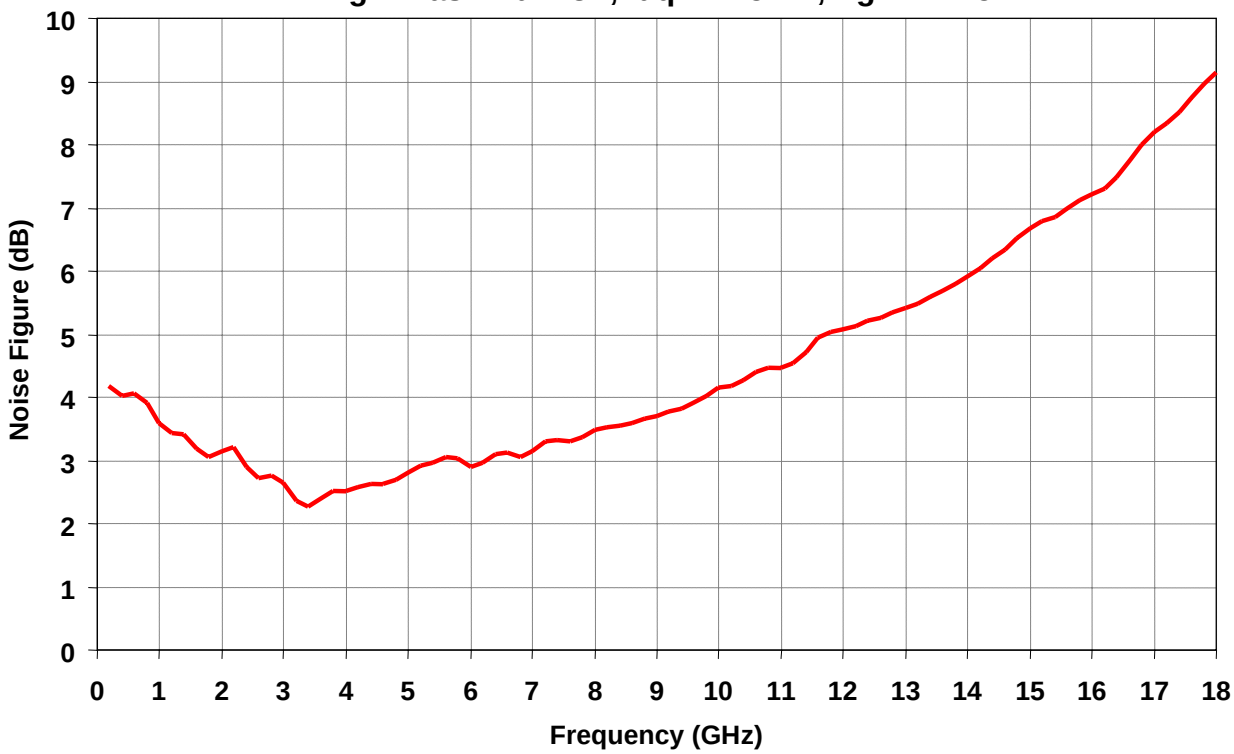
TGA1328 Typical Measured S-parameters



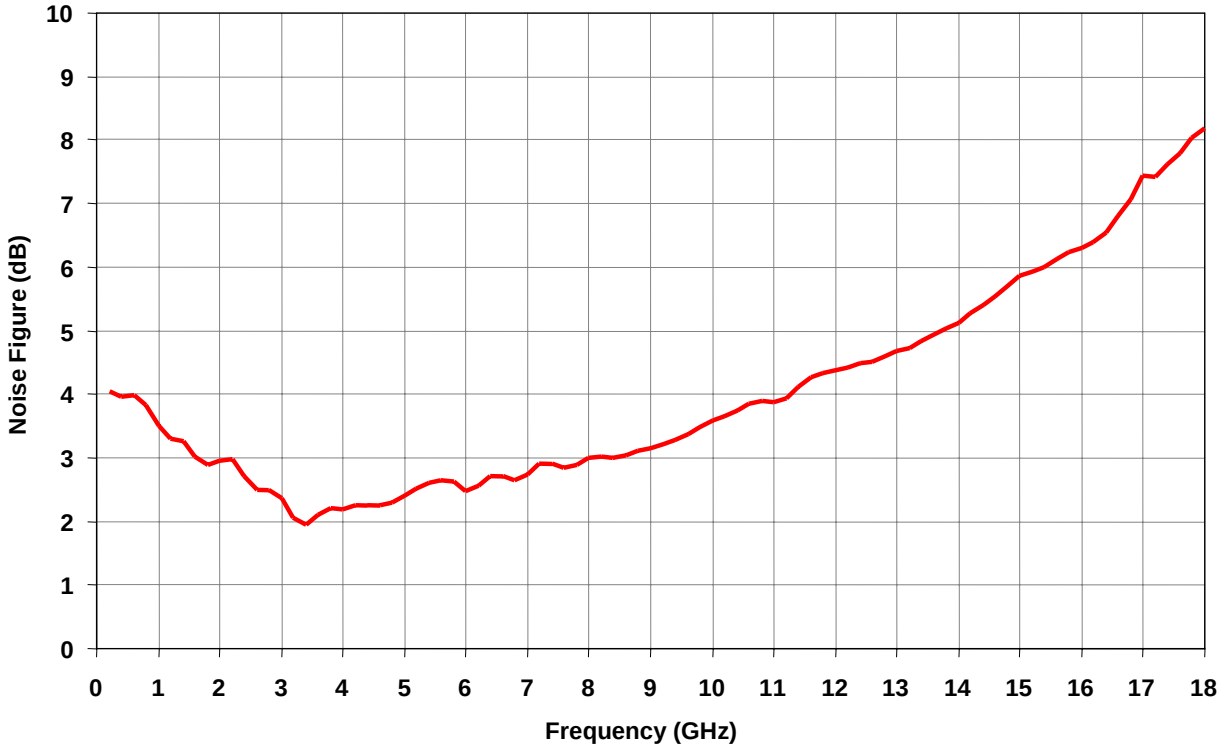


TGA1328 Typical Measured Noise Figure

High Bias: Vd = 8V, Idq = 175mA, Vg2 = +1.5V

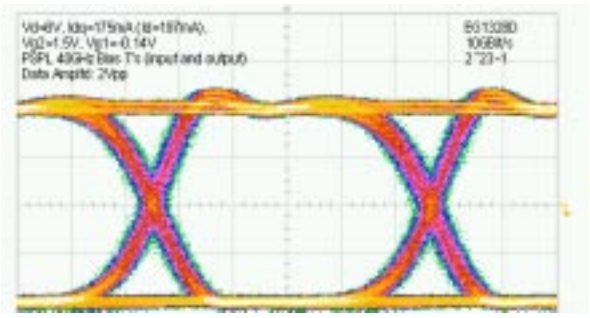


Low Bias: Vd = 4.5V, Idq = 80mA, Vg2 = +1.5V



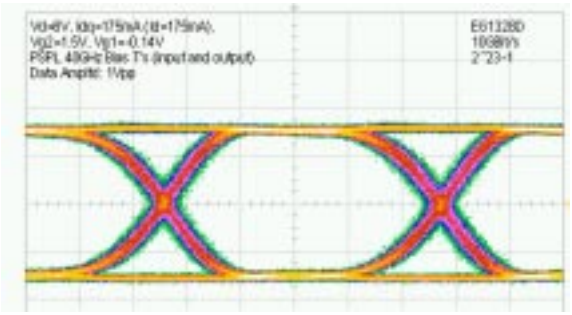
Measured Performance

8V P-P (Saturated)



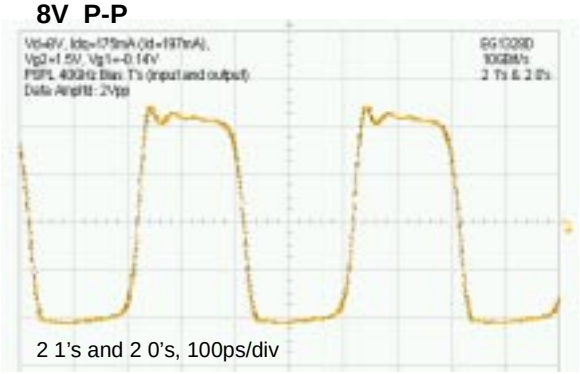
10GBit/s Performance
Output = 8V P-P, Input = 2V P-P
scale 2V/div, 20ps/div

6V P-P (Near Small Signal)



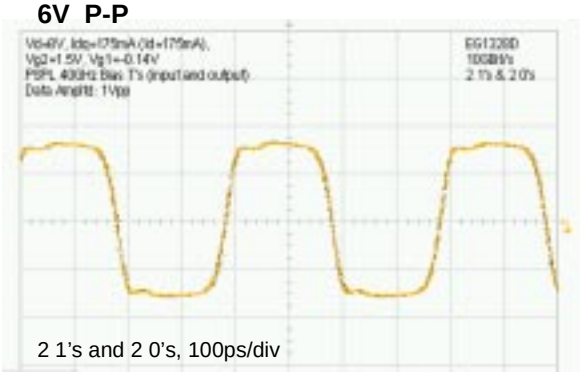
10GBit/s Performance
Output =6V P-P, Input = 1V P-P
scale 2V/div, 20ps/div

8V P-P

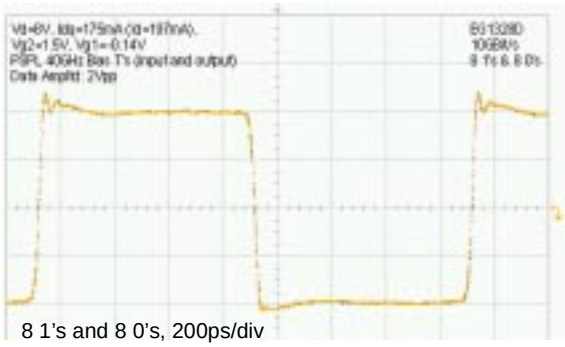


2 1's and 2 0's, 100ps/div

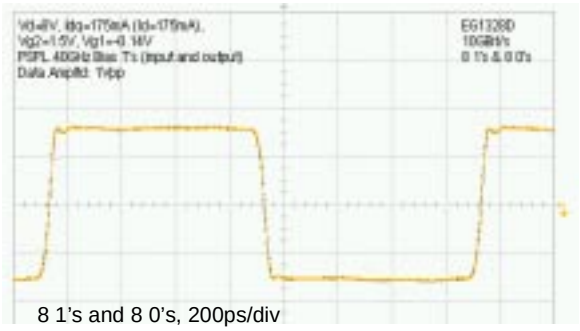
6V P-P



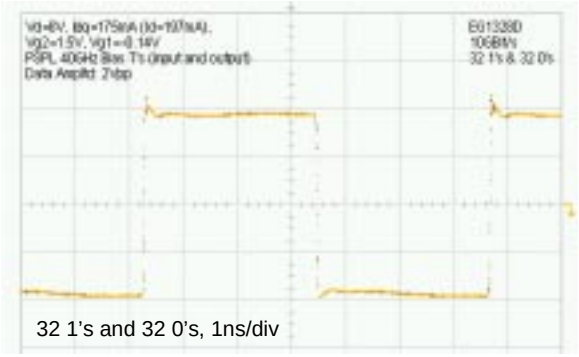
2 1's and 2 0's, 100ps/div



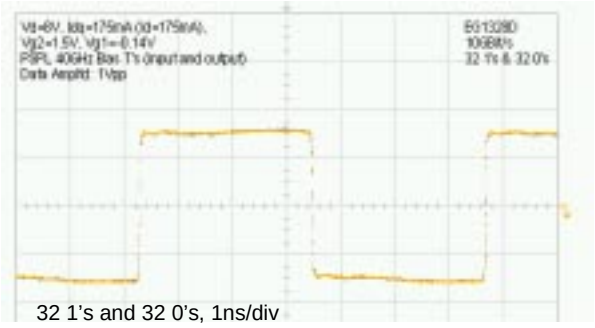
8 1's and 8 0's, 200ps/div



8 1's and 8 0's, 200ps/div



32 1's and 32 0's, 1ns/div



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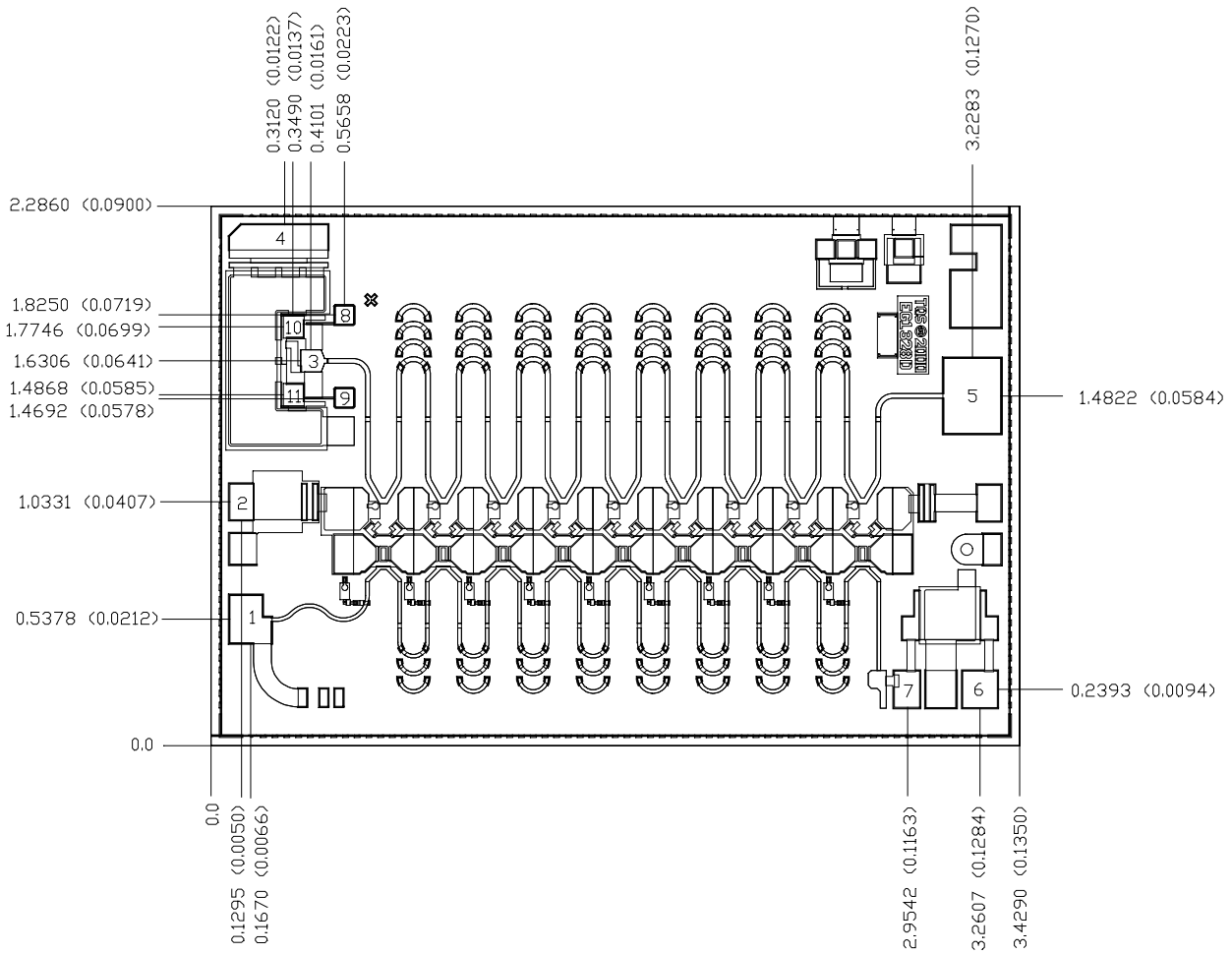
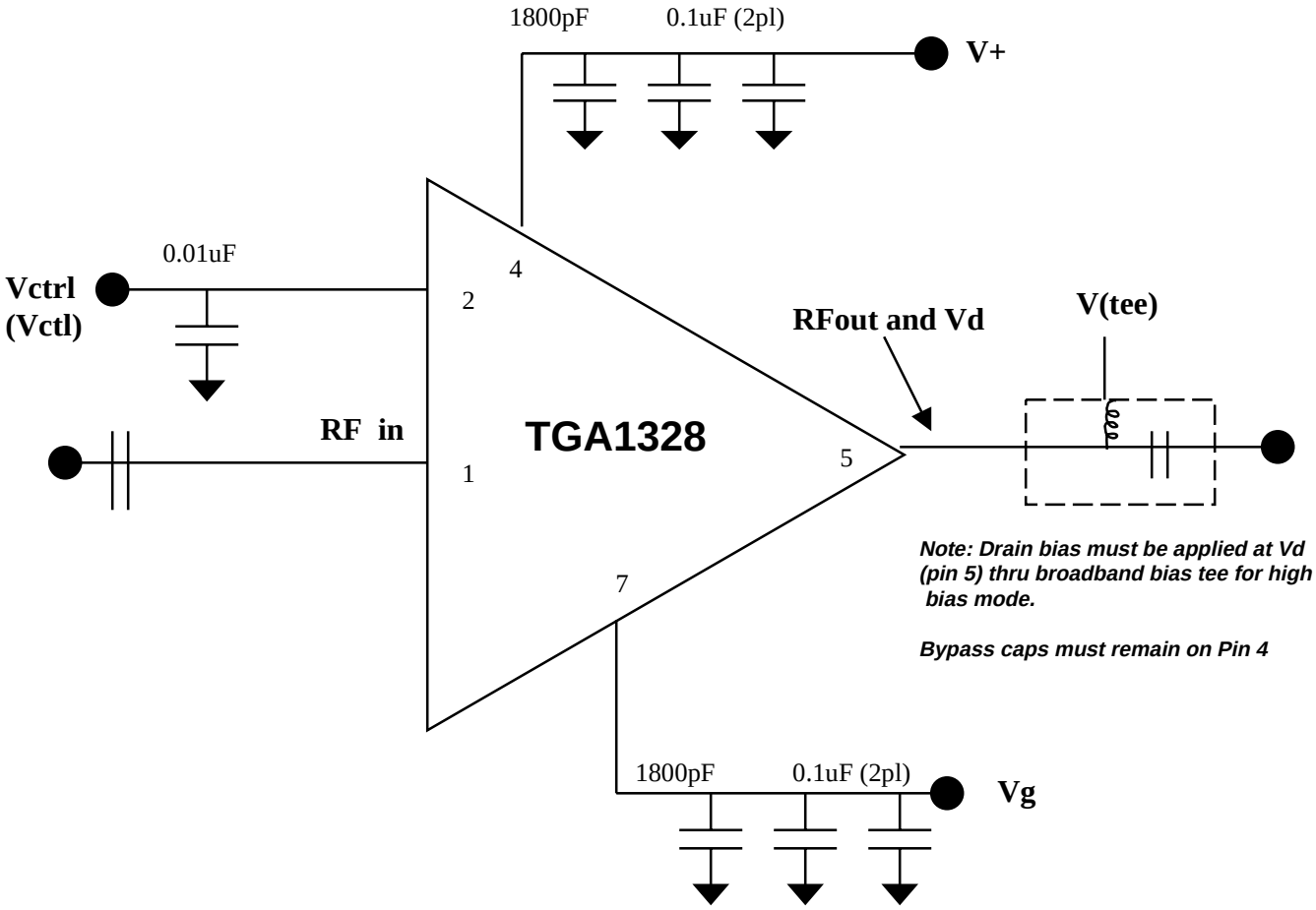


Units: millimeters (inches)
Thickness: 0.1016 (0.004) (reference only)
Chip edge to bond pad dimensions are shown to center of bond pad
Chip size tolerance: +/- 0.0508 (0.002)

Bond Pad #1 (RF Input)	0.152 x 0.203 (0.006 x 0.008)
Bond Pad #2 (Vctrl)	0.102 x 0.152 (0.004 x 0.006)
Bond Pad #3 (Vd)	0.076 x 0.152 (0.003 x 0.006)
Bond Pad #4 (V+)	0.419 x 0.152 (0.016 x 0.006)
Bond Pad #5 (RF Output)	0.254 x 0.330 (0.010 x 0.0013)
Bond Pad #6 (V-)	0.152 x 0.152 (0.006 x 0.006)
Bond Pad #7 (Vaux)	0.127 x 0.152 (0.005 x 0.006)
Bond Pad #8 (resistor tune)	0.085 x 0.085 (0.003 x 0.003)
Bond Pad #9 (resistor tune)	0.085 x 0.085 (0.003 x 0.003)
Bond Pad #10 (resistor tune)	0.091 x 0.095 (0.0036 x 0.0037)
Bond Pad #11 (resistor tune)	0.091 x 0.095 (0.0036 x 0.0037)



Bias Procedure

1) Make sure no RF power is applied to the device before continuing.

2) Pinch off device by setting Vg to –2.5V.

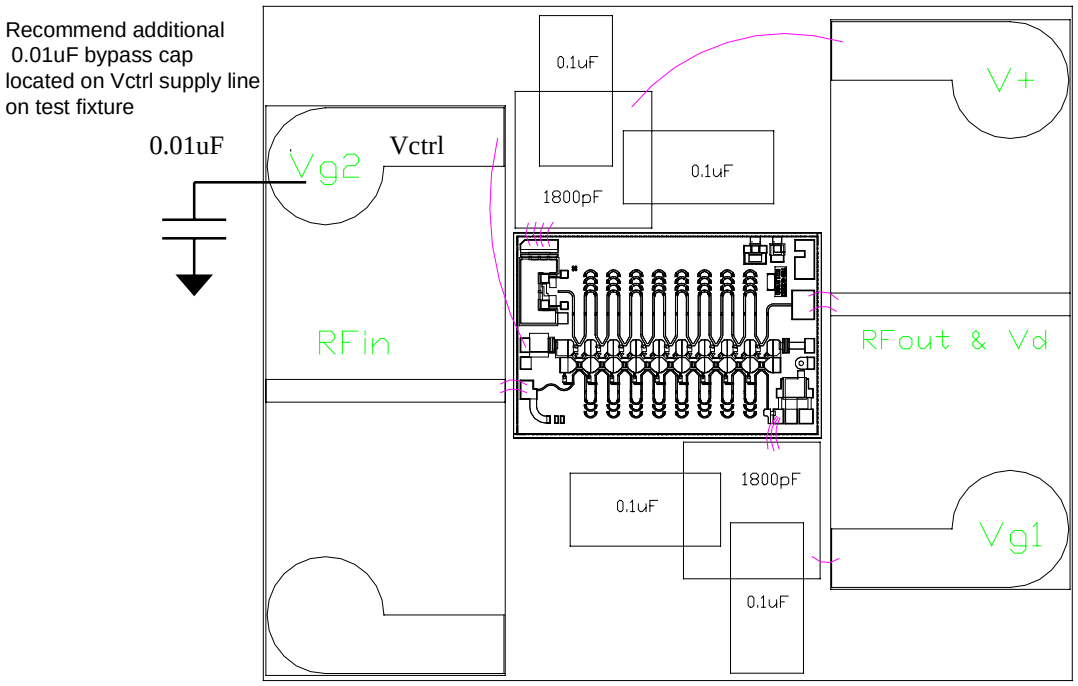
3) Raise Vd to 8.0V while monitoring drain current. Current should be zero.

NOTE: ***Vd bias should be applied to the RF output port via a bias tee for high power bias***.

4) Raise Vctl to 1.0V (no greater than 1.5V).

5) Make Vg more positive until drain current reaches 170mA. (80 mA for low noise bias)

6) Apply RF power. Note Vg supply must be capable of sinking 5mA of current.



Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300°C.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire.
- Maximum stage temperature is 200°C.

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.