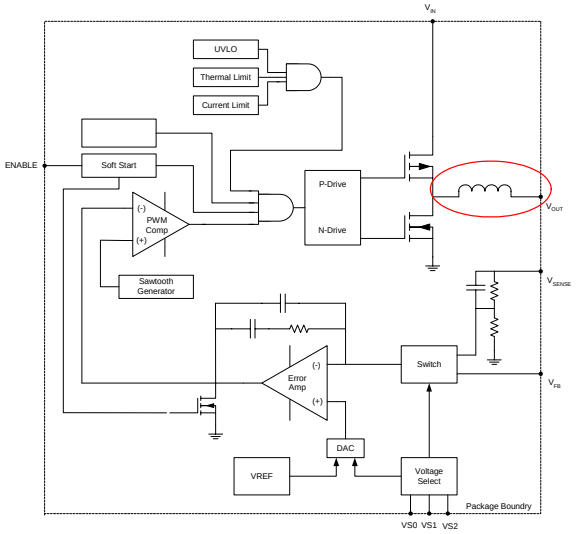
Preliminary

EN5312Q

Fully Integrated Voltage Mode Synchronous Buck PWM DC-DC Converter Module

Rev 0.87 January , 2006

RoHS Compliant



Product Highlights

- **Revolutionary integrated inductor**
- **Total footprint as small as 28mm^2**
- Only two low cost MLCC caps required.
- Very low solution profile at 1.1mm.
- 4mm x 5mm x1.1mm QFN package
- Wide 2.4V to 5.5V input range.
- 1000mA output current.
- Less than 1 µA standby current.
- High efficiency, up to 95%.
- Very low ripple voltage; < 10mV
- 3 Pin VID Voltage select scheme.
- External divider option.
- 5 MHz switching frequency
- 2% accuracy over line, load, & temp.
- Short circuit, UVLO, and thermal protection.
- Stable with up to 100uF output capacitance.

Product Overview

The Ultra-Low-Profile EN5312Q is targeted to applications where board area and profile are critical. EN5312Q is a complete power conversion solution requiring only two low cost ceramic MLCC caps. Inductor, MOSFETS, PWM, and compensation are integrated into a tiny 4mm x 5mm x 1.1mm QFN package. Engineered to minimize all sources of converter noise, the EN5312Q eases design and layout constraints. 5 MHz switching frequency and internal type III compensation provides superior transient response. With a 1.1 mm profile, the entire layout can occupy as little as 28mm^2 of board area.

A 3-pin VID output voltage select scheme provides seven pre-programmed output voltages along with an option for external resistor divider. Output voltage can be programmed on-the-fly to provide fast, dynamic voltage scaling.

Typical Application Circuit

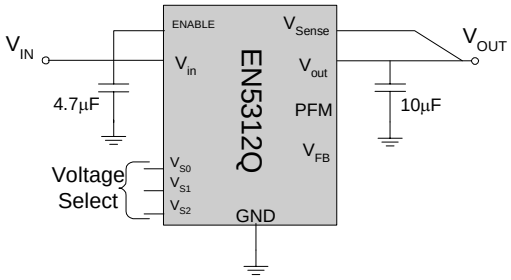


Figure 1. Typical application circuit.

Applications

- Area constrained applications
- Set top box/home gateway
- Smart phones and PDAs.
- VoIP and Video phones
- Personal Media Players.
- Advanced Mobile Processors, DSP, IO, Memory, Video, Multimedia Engines.

Absolute Maximum Ratings

Maximum Electrical Ratings	Min	Max
Voltages on: V_{IN}, V_{OUT}	-0.3V	7.0V
Voltages on: V_{SENSE}	-0.3V	V_{IN} + 0.3V
Voltages on: V_{S0}-V_{S2}	-0.3V	V_{IN} + 0.3V
Voltages on: ENABLE	-0.3V	V_{IN} + 0.3V
Voltages on: V_{FB}	-0.3V	1.5V
Maximum Thermal Ratings		
Ambient operating range (Industrial Rated)	-40°C	+85°C
Max Junction Temperature		+125°C
Storage Temperature Range	-65°C	+125°C
Solder Temperature Range MSL3 (10 Sec)		+260°C
Reflow Peak Body Temperature		+260°C

Electrical Characteristics

NOTE: V_{IN} = 3.6V and T_A = -40°C to +85°C unless otherwise noted. Typical values are at T_A = 25°C.
C_{IN} = 4.7uF, C_{OUT}=10uF

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	V_{IN}		2.4		5.5	V
Output Voltage	V_o	VS2 VS1 VS0 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1		V_{out} 3.3 2.5 1.8 1.5 1.25 1.2 0.8 User Sel		V
Maximum Output Current V_{IN} = 5V, 0.6V <V_{OUT} < 3.3V						
Output Current	I_{OUT}		1000			mA
Shut-Down Current	I_{SD}	Enable = Low		<1		µA
PFET Current Limit	I_{LIM}		1.4			A
Feedback Pin Voltage	V_{FB}			0.6		V
Feedback Pin Input Current	I_{FB}					nA
VS0-VS1, Enable Voltage Threshold	V_{TH}	Pin = Low Pin = High	0.0 1.4		0.4 V_{IN}	
VS0-VS2 Pin Input Current	I_{VSX}					nA
Operating Frequency	F_{OSC}			5		MHz
PFET On Resistance	$R_{DS(ON)}$			300		mΩ
NFET On Resistance	$R_{DS(ON)}$			300		mΩ
Ripple Voltage	V_{Ripple}	COUT=4.7uF 1206 MLCC		10		mV
Operating Junction Temperature	T_J				125	°C
Thermal Shutdown	T_{SD}			150		°C
Thermal Shutdown	T_{SDH}			15		°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Hysteresis						
Voltage Accuracy		All parts over line, load and Temp			±2	%
Voltage Regulation		Any given part, Over load, line, temp			±1	%
Soft-Start Operation						
Time to 90% V_{out}	T_{ss}	Vout = 3.3V		1.6		mSec

Pin Description

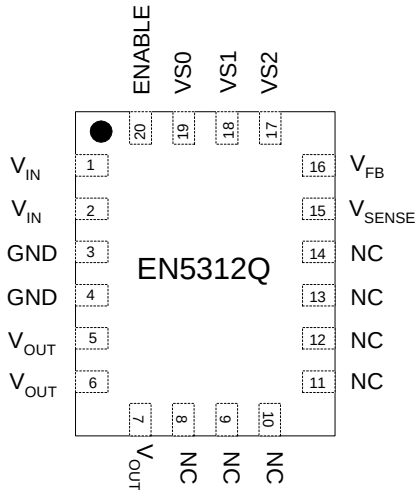


Figure 2. Pin description, top view.

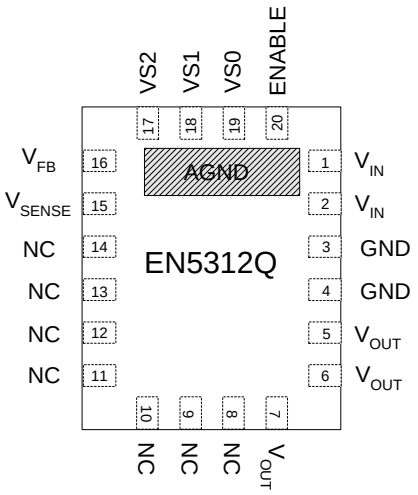


Figure 3. Pin description, bottom view.

V_{IN} (Pin 1,2): Input voltage pin. Supplies power to the IC. VIN can range from 2.4V to 5.5V.

GND: (Pin 3,4): Power ground. This pin is internally connected to bottom thermal/ground pad (AGND). Input and output filter capacitors should be connected to this pin. Good EMI design practice dictates that these pins not be connected to other ground connections. The large thermal pad on the bottom of the package should be the single point of contact to system ground. (refer to section on EMI layout consideration for more detail).

V_{OUT} (Pin 5,6,7): Regulated output voltage.

NC (Pin 8,9,10,11,12,13,14): These pins should not be electrically connected to each other or to any external signal, voltage, or ground. One or more of these pins may be connected internally.

V_{SENSE} (Pin 15): Sense pin for preset output voltages. When using preset voltages connect this to V_{LOAD} or as close to V_{LOAD} as possible to ensure the best regulation. When using external divider, connect this pin to $V_{OUT.}$

V_{FB} (Pin 16): Feed back pin for external divider option. When using the external divider option (VS0=VS1=VS2= high) connect this pin to the center of the external divider. Set the divider such that V_{FB} = 0.6V.

VS0,VS1,VS2 (Pin 17,18,19): Output voltage select. VS0=pin19, VS1=pin18, VS2=pin17. Selects one of seven preset output voltages or choose external divider by connecting pins to logic high or low. Logic low is defined as $V_{LOW} \leq 0.4V$. Logic high is defined as $V_{HIGH} \geq 1.4V$. Any level between these two values is indeterminate. (refer to section on output voltage select for more detail).

ENABLE (Pin 20): Output enable. Enable = logic high, disable = logic low. Logic low is defined as $V_{LOW} \leq 0.4V$. Logic high is defined as $V_{HIGH} \geq$

1.4V. Any level between these two values is indeterminate.

AGND (Bottom thermal/ground pad): System ground for single point grounding. Also functions as thermal pad to remove heat from package. Connect to surface or PWB internal ground plane.

Functional Block Diagram

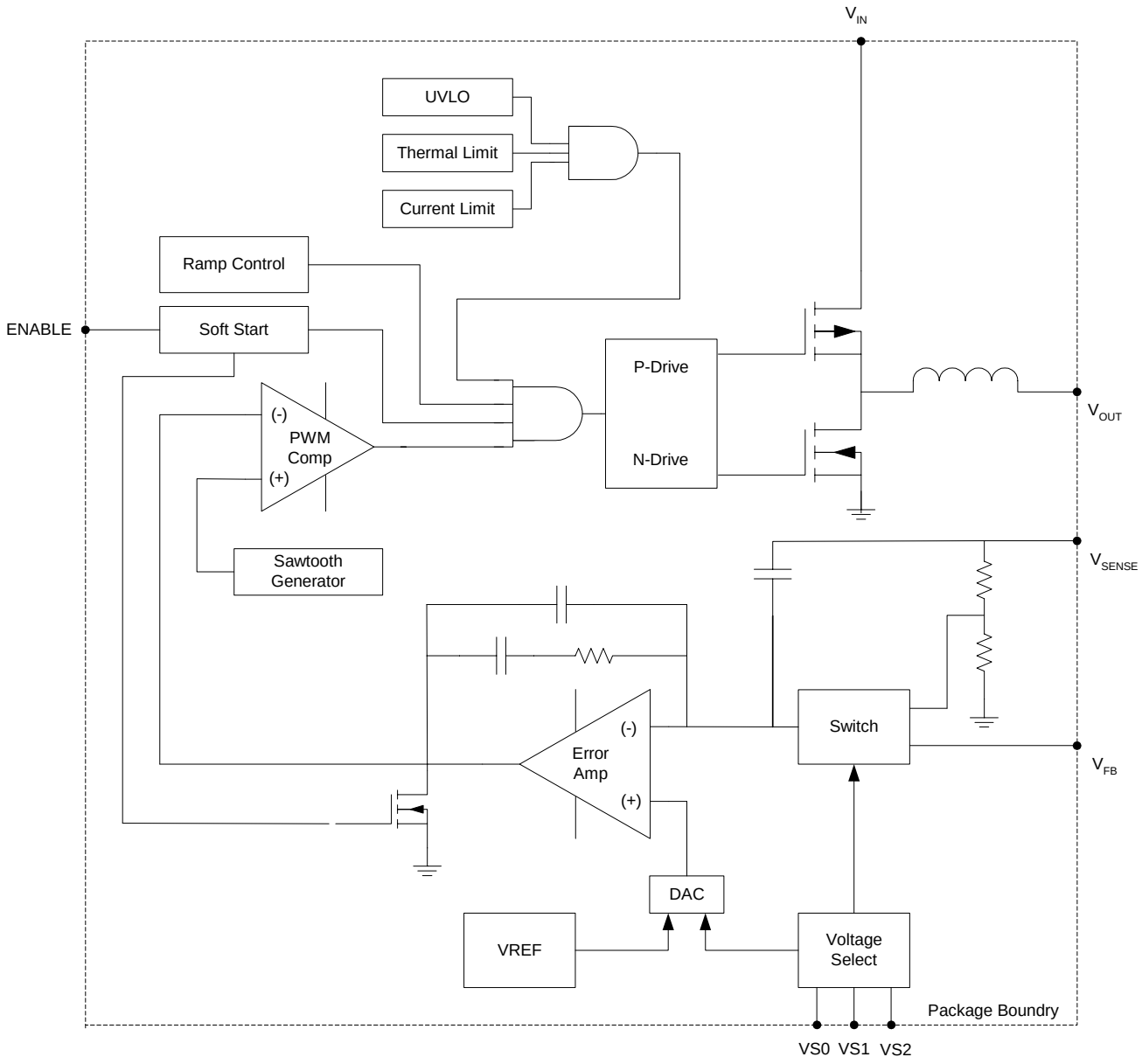


Figure 4. Functional block diagram.

Typical Performance Characteristics

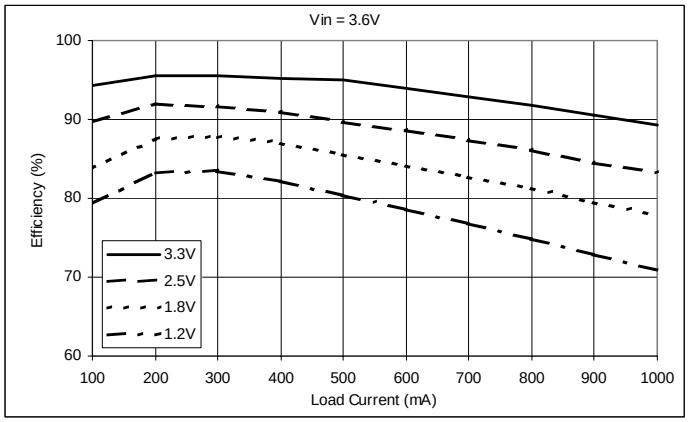


Figure 5. Efficiency -vs- Load, Vin = 3.6V.

Detailed Description

Functional Overview

The EN5312Q is a complete DCDC converter solution requiring only two low cost MLCC capacitors. MOSFET switches, PWM controller, Gate-drive, compensation, and inductor are integrated into the tiny 4mm x 5mm x 1.1mm package to provide the smallest footprint possible while maintaining high efficiency, low quiescent current, and high performance. The converter uses voltage mode control to provide the simplest implementation while also providing excellent transient response. The device operates at a 5 MHz switching frequency to make possible the very small components required to enable this unprecedented level of integration.

Enpirion's proprietary power MOSFET technology provides very low switching loss at frequencies of 5 MHz and higher, allowing for the use of very small internal components, and very wide control loop bandwidth. Unique magnetics allow for high value inductor integrated into a low profile 1.1mm package. Integration of the inductor substantially reduces switching noise and design/layout issues normally associated with switch-mode DCDC converters. All of this enables much easier and faster integration into various applications to meet demanding EMI requirements.

Output voltage is chosen from seven preset values via a three pin VID voltage select scheme. An external divider option enables the selection of any voltage in the 3.3V to 0.6V range. This reduces the number of components that must be qualified and reduces inventory problems. The VID pins can be toggled on the fly to implement glitch free dynamic voltage scaling.

Protection features include under-voltage lock-out (UVLO), over-current protection (OCP), short circuit protection, and thermal overload protection.

Integrated Inductor for Low Noise Design

Enpirion has introduced the world's first product family featuring integrated inductors. The EN5312Q family utilizes a low loss, planar construction inductor. The use of an internal inductor reduces noise associated with pulsed switching currents that would otherwise be present on the user circuit board. Integration minimizes the path impedance between the MOSFET switches and the inductor electrode, thereby reducing one of the

key sources of conducted noise associated with switch-mode DCDC converters. The planar inductor construction orients the leakage magnetic fields in a direction that is orthogonal to those that can couple noise onto signal traces on the circuit board. Further, the package layout is optimized to reduce the electrical path length for the AC ripple currents that are the leading source of radiated emissions from DCDC converters. The integrated inductor significantly reduces switching noise effects, reduces parasitic effects that can harm loop stability, and makes layout very easy.

Stable Over Wide Range of Operating Conditions

The EN5312Q utilizes an internal type III compensation network and is designed to provide a high degree of stability over a wide range of operating conditions. One of the key features of this device is the ability to add supplementary capacitance to the output to further improve transient performance or reduce output voltage ripple. The EN5312Q is stable with up to 100uF of total output capacitance. The very high switching frequency allows for a very wide control loop bandwidth.

Soft Start

Internal soft start circuits limit in-rush current when the device starts up from a power down condition or when the "ENABLE" pin is asserted "high". Digital control circuitry limits the V_{OUT} ramp rate to levels that are safe for the Power MOSFETS and the integrated inductor. The soft start ramp rate is nominally 2mV/µSec.

Over Current/Short Circuit Protection

The current limit function is achieved by sensing the current flowing through a sense P-MOSFET which is compared to a reference current. When this level is exceeded the P-FET is turned off and the N-FET is turned on, pulling V_{OUT} low. This condition is maintained for a period of 1mS and then a normal soft start is initiated. If the over current condition still persists, this cycle will repeat in a "hick-up" mode.

Under Voltage Lockout

During initial power up an under voltage lockout circuit will hold-off the switching circuitry until the input voltage reaches a sufficient level to insure proper operation. If the voltage drops below the UVLO threshold the lockout circuitry will again disable the switching. Hysteresis is included to prevent chattering between states.

Enable

The ENABLE pin provides a means to shut down the converter or enable normal operation. A logic low will disable the converter and cause it to shut down. A logic high will enable the converter into normal operation. In shutdown mode, the device quiescent current will be less than 1 uA.

NOTE: This pin must not be left floating.

Thermal Shutdown

When excessive power is dissipated in the chip, the junction temperature rises. Once the junction temperature exceeds the thermal shutdown temperature the thermal shutdown circuit turns off the converter output voltage thus allowing the device to cool. When the junction temperature decreases by 15C°, the device will go through the normal startup process.

Application Information

Output Voltage Select

To provide the highest degree of flexibility in choosing output voltage, the EN5312Q family uses a 3 pin VID, or Voltage ID, voltage select arrangement. This allows the designer to choose one of seven preset voltages, or to use an external voltage divider. Internally, the output of the VID multiplexer sets the value for the voltage reference DAC, which in turn is connected to the non-inverting input of the error amplifier. This allows the use of a single feedback divider with constant loop gain and optimum compensation, independent of the output voltage selected.

VS2	VS1	VS0	V_{OUT}
0	0	0	3.3V
0	0	1	2.5V
0	1	0	1.8V
0	1	1	1.5V
1	0	0	1.25V
1	0	1	1.2V
1	1	0	0.8V
1	1	1	User Selectable

Table 1. Voltage select settings.

Table 1 shows the various VS0-VS2 pin logic states and the associated output voltage levels. A logic "1" indicates a connection to V_{IN} or to a "high" logic voltage level. A logic "0" indicates a connection to ground or to a "low" logic voltage level. These pins can be either hardwired to V_{IN} or GND or alternatively can be driven by standard logic levels. Logic low is defined as $V_{LOW} \leq 0.4V$. Logic high is defined as $V_{HIGH} \geq 1.4V$. Any level between these two values is indeterminate.

External Voltage Divider

As described above, the external voltage divider option is chosen by connecting the VS0, VS1, and VS2 pins to VIN or logic "high". The EN5312Q uses a separate feedback pin, V_{FB}, when using the external divider. VSENSE must be connected to V_{OUT} as indicated in Figure 6.

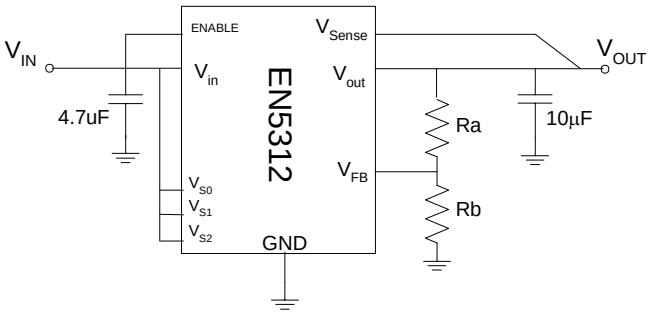


Figure 6. External Divider.

The output voltage is selected by the following formula:

$$V_{OUT} = 0.6V\left(1 + \frac{Ra}{Rb}\right)$$

R_a must be chosen as 200KΩ to maintain loop gain. Then R_b is given as:

$$R_b = \frac{1.2x10^5}{V_{OUT} - 0.6}\Omega$$

Dynamically Adjustable Output

The EN5312Q is designed to allow for dynamic switching between the predefined VID voltage levels, or between the predefined output levels and an external divider. The inter-voltage slew rate is optimized to prevent excess undershoot or overshoot as the output voltage levels transition. The slew rate is identical to the soft-start slew rate of 2mV/uS.

Input and Output Capacitors

The **input** capacitance requirement is 4.7uF. Enpirion recommends that a low ESR MLCC capacitor be used. The input capacitor must use a X5R or X7R dielectric formulation. Y5V or equivalent dielectric formulations loose capacitance

with frequency, bias, and temperature and are not recommended for switch-mode DC-DC converter input and output filter applications.

The **output** capacitance requirement is a minimum of 10uF. The control loop is designed to be stable with up to 100uF of total output capacitance. Capacitance above the 10uF minimum should be added if the transient performance is not sufficient using the 10uF. Enpirion recommends a low ESR MLCC type capacitor be used. The output capacitor must use a X5R or X7R dielectric formulation. Y5V or equivalent dielectric formulations loose capacitance with frequency, bias, and temperature and are not recommended for switch-mode DC-DC converter input and output filter applications

Layout Considerations and Application Circuits

EMI Considerations for Board Layout

Integrated inductor and planar inductor construction go a long way toward reducing many of the sources of EMI, both conducted and radiated. However, care must still be taken to minimize potential sources of EMI. The package pin-out is carefully engineered to allow for the optimal layout. Input, output, and power ground planes are arranged such that the physical size of the AC current loops can be minimized and noisy power ground isolated.

1. **Single point grounding:** To limit AC current from flowing onto sensitive signal ground planes it is strongly recommended that a single point of contact be used for system ground. The thermal/ground pad located on the bottom of the package should be used for this common grounding point. The PGND pins, pins 3 and 4, are internally connected to the thermal/ground pad and so provides for an isolated power ground node for the input and output filter capacitors. Connect the input and output filter capacitors to these ground pins as shown in figure 7. Do not use these grounds for any other connections.

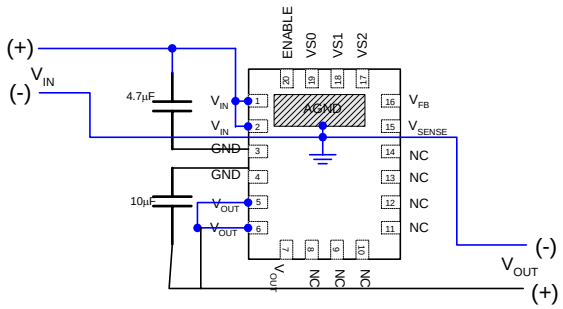


Figure 7. Common point grounding schematic.

2. **Pins 9, 11, 12, 13 are connected internally to V_{DRAIN}.** Keep all sensitive signal traces away from these pins.
3. **Do not use vias for input and output filter caps.** It is very important that input and output filter caps be placed on the same side of the board as the EN5312Q. At frequencies above 1 MHz, the skin penetration is too shallow for the AC signals to pass properly through a via. The AC currents will instead conduct along the surface of the planes and potentially couple noise.

Typical Applications Circuits

Example 1: Application utilizing preset output voltage, 1.8V.

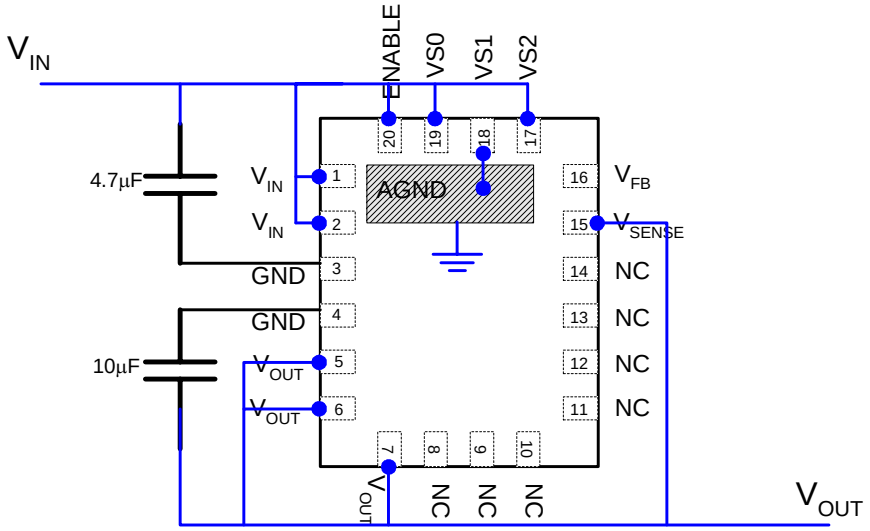


Figure 8. Application circuit with Vout = 1.8V.

Example 2: Application using external divider to program V_{OUT}

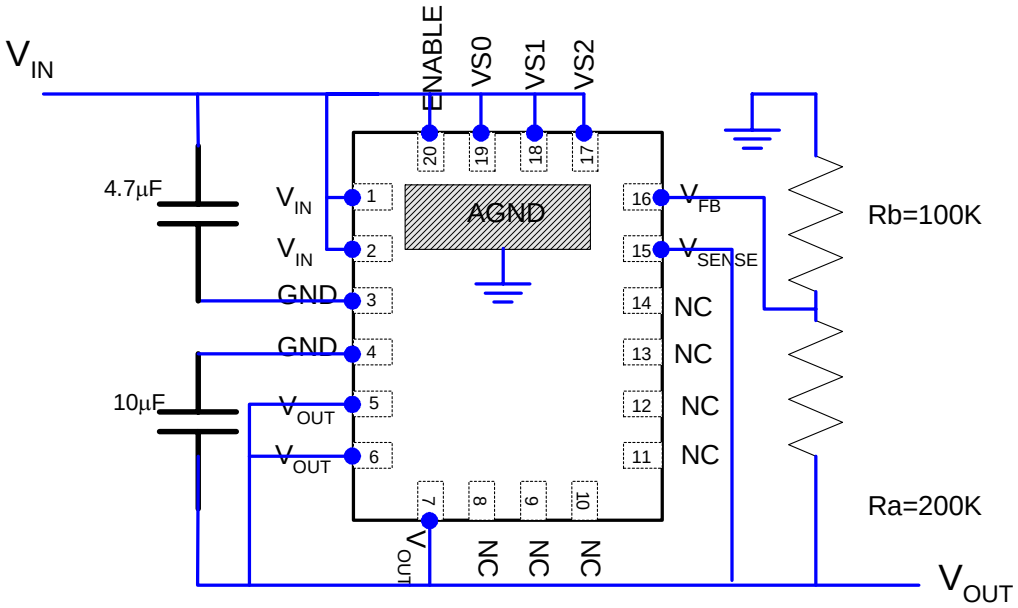


Figure 9. Application demonstrating use of external divider output voltage programming; V_{OUT} = 1.8V.

Exposed Metal on Bottom Of Package

Lead frame offers many advantages in thermal performance, in reduced electrical lead resistance, and in overall foot print. However, they do require some special considerations.

In the assembly process lead frame construction requires that for mechanical support, some of the lead-frame cantilevers be exposed at the point where wire-bond or internal passives are attached. This results in several small pads being exposed on the bottom of the package.

Only the AGND/Thermal pad and the perimeter pads are to be mechanically or electrically connected to the PC board. PWB solder mask must be used to prevent connection to the other pads. Figure 11 shows the shape and location of these metal pads as well as the mechanical dimension of the AGND/Thermal pad and the pins. The "grayed-out" area represents the area that should be protected by solder mask on the PWB.

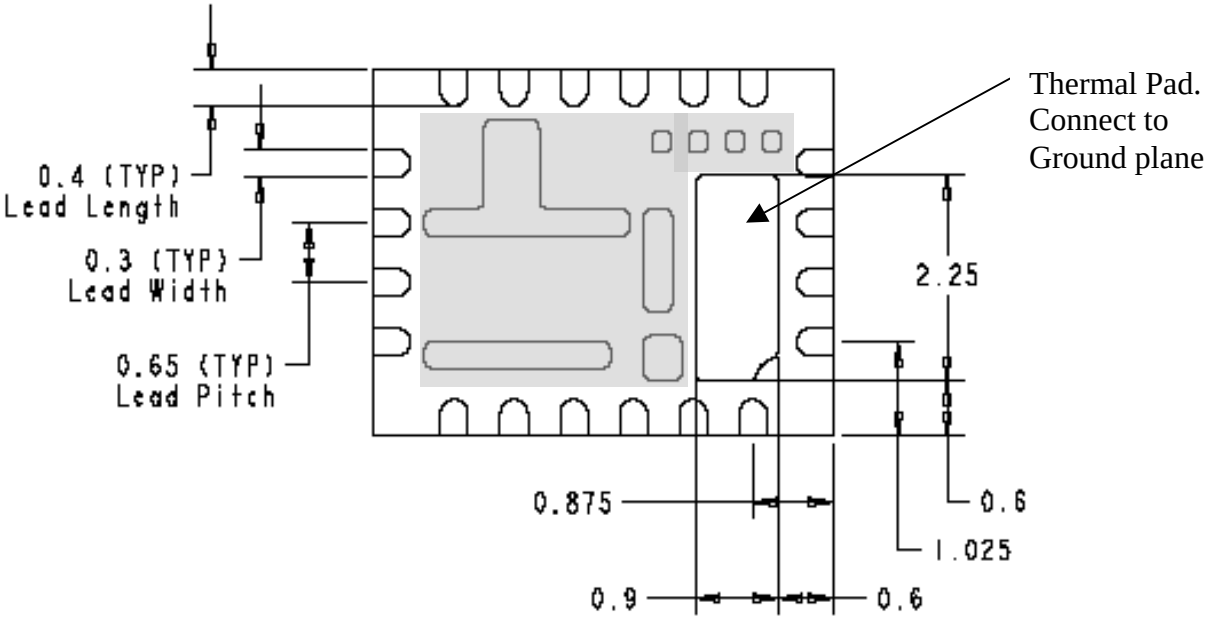


Figure 10. Exposed metal and mechanical dimensions of the package .

Figure 11 shows the recommended PWB solder mask openings.

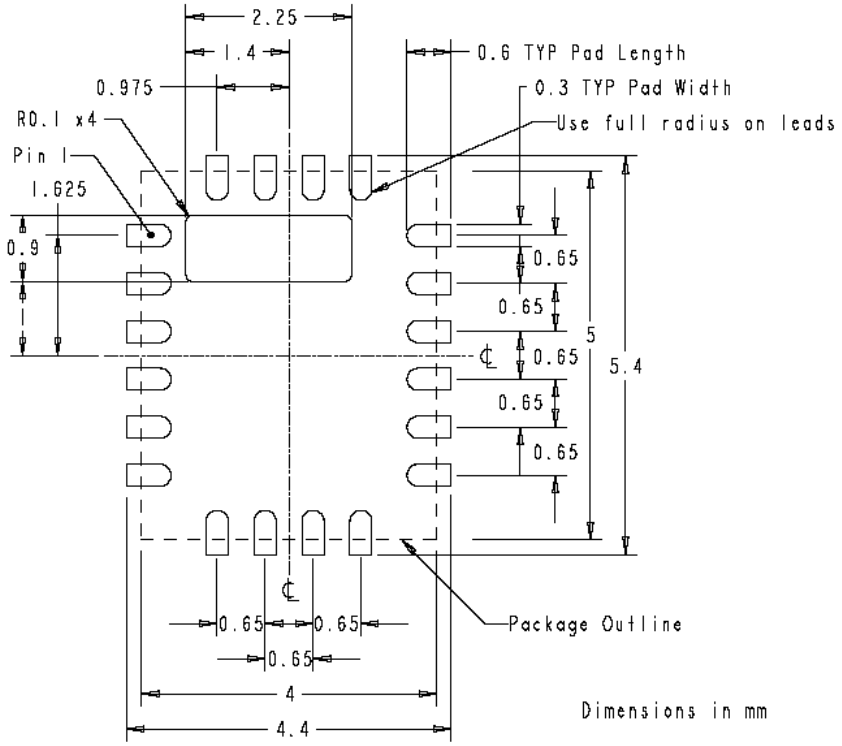
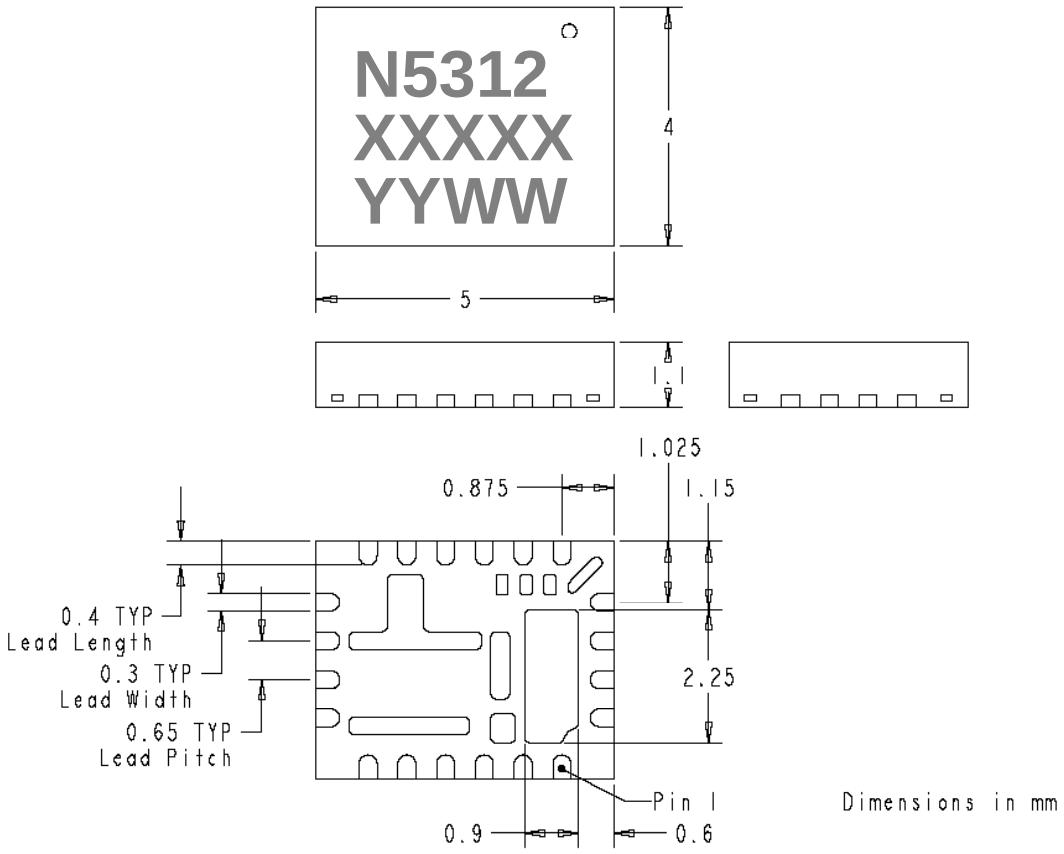


Figure 11. PWB Solder Mask Openings.



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