W83697SF

WINBOND I/O

W83697SF Data Sheet Revision History

	Pages	Dates	Version	Version on Web	Main Contents
1	n.a.	04/16/01	0.50	0.50	First published
2	111	04/27/01	0.51	0.51	Update the Top Marking
3		12/16/02	1.0	1.0	New Update
4					
5					
6					
7					
8					
9					
10					

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

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GENERAL DESCRIPTION

The W83697SF is evolving product from Winbond's most popular I/O family. They feature a whole new interface, namely LPC (**Low Pin Count**) interface, which will be supported in the new generation chip-set. This interface as its name suggests is to provide an economical implementation of I/O's interface with lower pin count and still maintains equivalent performance as its ISA interface counterpart. Approximately 40 pin counts are saved in LPC I/O comparing to ISA implementation. With this additional freedom, we can implement more devices on a single chip as demonstrated in W83697SF's integration of Game Port and MIDI Port. It is fully transparent in terms of software which means no BIOS or device driver update is needed except chip-specific configuration.

As Smart Card application is gaining more and more attention, W83697SF also implements a smart card reader interface featuring Smart wake-up function. This smart card reader interface fully meets the ISO7816 and PC/SC (Personal Computer/Smart Card Workgroup) standards. W83697SF provides a minimum external components and lowest cost solution for smart card applications.

The disk drive adapter functions of W83697SF include a floppy disk drive controller compatible with the industry standard 82077/ 765, data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. The wide range of functions integrated onto the W83697SF greatly reduces the number of components required for interfacing with floppy disk drives. The W83697SF supports four 360K, 720K, 1.2M, 1.44M, or 2.88M disk drives and data tranSFer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s,1 Mb/s, and 2 Mb/s.

The W83697SF provides two high-speed serial communication ports (UARTs), one of which supports serial Infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and a processor interrupt system. Both UARTs provide legacy speed with baud rate up to 115.2k bps and also advanced speed with baud rates of **230k**, **460k**, or **921k bps** which support higher speed modems. In addition, the W83697SF provides IR functions: **IrDA 1.0** (**SIR** for 1.152K bps) and TV remote IR (**Consumer IR**, supporting NEC, RC-5, extended RC-5, and RECS-80 protocols).

The W83697SF supports one PC-compatible printer port (SPP), Bi-directional Printer port (BPP) and also Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP). Through the printer port interface pins, also available are: Extension FDD Mode and Extension 2FDD Mode allowing one or two external floppy disk drives to be connected.

The configuration registers support mode selection, function enable/disable, and power down function selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature demand of Windows 95/98™, which makes system resource allocation more efficient than ever.

The W83697SF provides a set of flexible I/O control functions to the system designer through a set of General Purpose I/O ports. These GPIO ports may serve as simple I/O or may be individually configured

to provide a predefined alternate function. General Purpose Port 1 is designed to be functional even in power down mode (VCC is off).

The W83697SF is made to fully comply with **Microsoft® PC98 and PC99 Hardware Design Guide, and meet the requirements of ACPI.**

The W83697SF contains a game port and a MIDI port. The game port is designed to support 2 joysticks and can be applied to all standard PC game control devices, They are very important for a entertainment or consumer computer.

The W83697SF provides Flash ROM interface. That can support up to 4M legacy flash ROM.

Moreover, W83697SF support 3 sets PWM Fan Speed Control, which are very important for a high-end computer system to work stably and properly.

FEATURES

General

- Meet LPC Spec. 1.1
- Support LDRQ#(LPC DMA), SERIRQ (serial IRQ)
- Include all the features of Winbond I/O W83877TF
- Integrate Smart Card functions
- Compliant with Microsoft PC98/PC99 Hardware Design Guide
- Support DPM (Device Power Management), ACPI
- Programmable configuration settings
- Single 24 or 48 MHz clock input

FDC

- Compatible with IBM PC AT disk drive systems
- Variable write pre-compensation with track selectable capability
- Support vertical recording format
- DMA enable logic
- 16-byte data FIFOs
- Support floppy disk drives and tape drives
- Detects all overrun and underrun conditions
- Built-in address mark detection circuit to simplify the read electronics
- FDD anti-virus functions with software write protect and FDD write enable signal (write data signal was forced to be inactive)
- Support up to four 3.5-inch or 5.25-inch floppy disk drives
- Completely compatible with industry standard 82077
- 360K/720K/1.2M/1.44M/2.88M format; 250K, 300K, 500K, 1M, 2M bps data transfer rate
- Support **3-mode FDD, and its Win95/98 driver**

UART

- Two high-speed 16550 compatible UARTs with 16-byte send/receive FIFOs
- MIDI compatible
- Fully programmable serial-interface characteristics:
  --- 5, 6, 7 or 8-bit characters
  --- Even, odd or no parity bit generation/detection
  --- 1, 1.5 or 2 stop bits generation

- Internal diagnostic capabilities:
  --- Loop-back controls for communications link fault isolation
  --- Break, parity, overrun, framing error simulation
- Programmable baud generator allows division of 1.8461 MHz and 24 MHz by 1 to (2^{16}-1)
- Maximum baud rate up to **921k bps** for 14.769 MHz and 1.5M bps for 24 MHz

Infrared

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps
- Support Consumer IR with Wake-Up function.

Parallel Port

- Compatible with IBM parallel port
- Support PS/2 compatible bi-directional parallel port
- Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
- Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
- Extension FDD mode supports disk drive B; and Extension 2FDD mode supports disk drives A and B through parallel port
- Enhanced printer port back-drive current protection

Game Port

- Support two separate Joysticks
- Support every Joystick two axes (X,Y) and two buttons (S1,S2) controllers

MIDI Port

- The baud rate is 31.25 Kbaud
- 16-byte input FIFO
- 16-byte output FIFO

Flash ROM Interface

- Support up to 4M flash ROM

General Purpose I/O Ports

- 60 programmable general purpose I/O ports
- General purpose I/O ports can serve as simple I/O ports, watch dog timer output, power LED output, infrared I/O pins, suspend LED output, Beep output
- Functional in power down mode

Smart Card Reader Interface

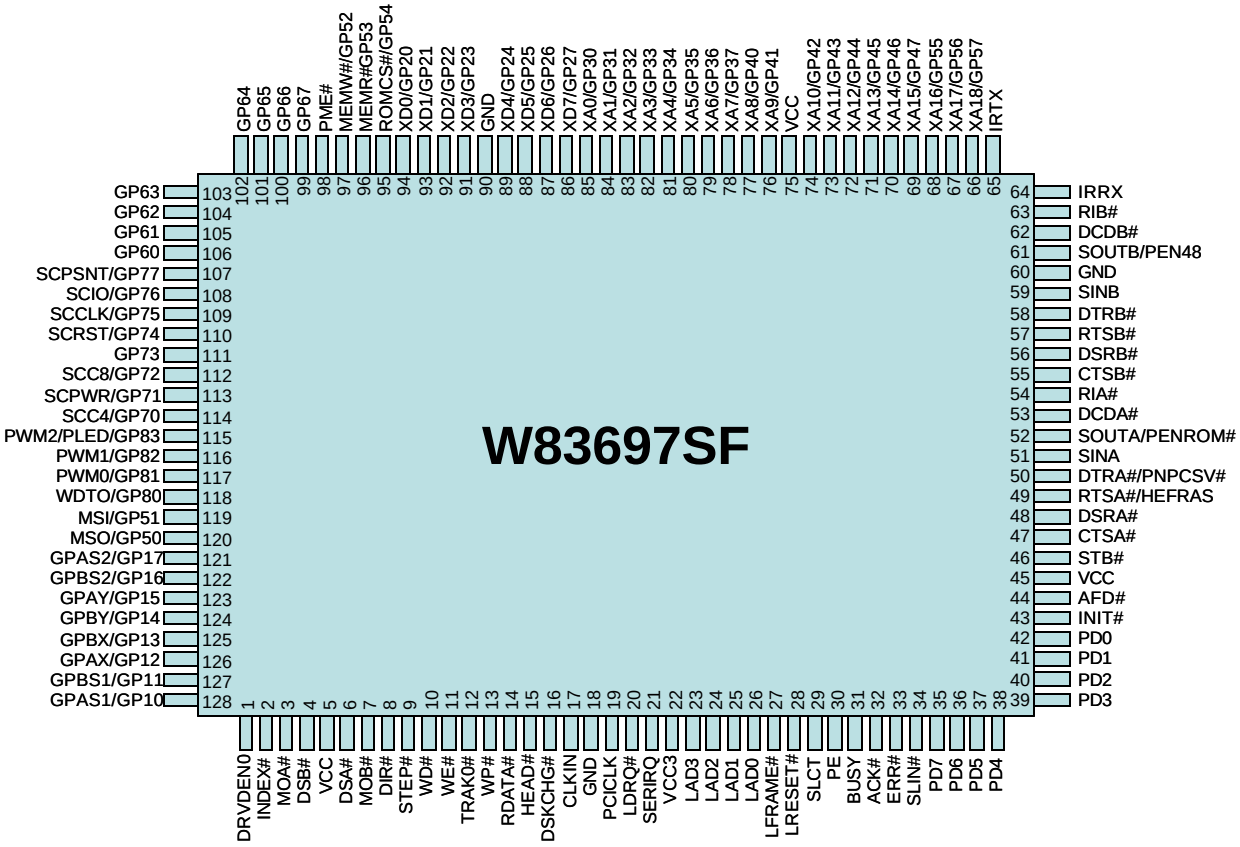
- ISO7816 protocol compliant
- PC/SC T=0, T=1 compliant

Fan Speed Control

- 3 Sets PWM Fan Speed Control

Package

- 128-pin PQFP



PIN CONFIGURATION FOR 697SF

1. PIN DESCRIPTION

Note: Please refer to Section 10.2 DC CHARACTERISTICS for details

PIN DESCRIPTION	
I/O8t	TTL level bi-directional pin with 8mA source-sink capability
I/O12t	TTL level bi-directional pin with 12mA source-sink capability
I/O24t	TTL level bi-directional pin with 24 mA source-sink capability
I/O12tp3	3.3V TTL level bi-directional pin with 12mA source-sink capability
I/O12ts	TTL level Schmitt-trigger bi-directional pin with 12mA source-sink capability
I/O24ts	TTL level Schmitt-trigger bi-directional pin with 24mA source-sink capability
I/O24tsp3	3.3V TTL level Schmitt-trigger bi-directional pin with 24mA source-sink capability
I/OD12t	TTL level bi-directional pin and open-drain output with 12mA sink capability
I/OD24t	TTL level bi-directional pin and open-drain output with 24mA sink capability
I/OD24c	CMOS level bi-directional pin and open-drain output with 24mA sink capability
I/OD24a	Bi-directional pin with analog input and open-drain output with 24mA sink capability
I/OD12ts	TTL level Schmitt-trigger bi-directional pin and open-drain output with 12mA sink capability
I/OD24ts	TTL level Schmitt-trigger bi-directional pin and open-drain output with 24mA sink capability
I/OD12cs	CMOS level Schmitt-trigger bi-directional pin and open-drain output with 12mA sink capability
I/OD16cs	CMOS level Schmitt-trigger bi-directional pin and open-drain output with 16mA sink capability
I/OD24cs	CMOS level Schmitt-trigger bi-directional pin and open-drain output with 24mA sink capability
I/OD12csd	CMOS level Schmitt-trigger bi-directional pin with internal pull down resistor and open-drain output with 12mA sink capability
I/OD12csu	CMOS level Schmitt-trigger bi-directional pin with internal pull up resistor and open-drain output with 12mA sink capability
O4	Output pin with 4 mA source-sink capability
O8	Output pin with 8 mA source-sink capability
O12	Output pin with 12 mA source-sink capability
O16	Output pin with 16 mA source-sink capability
O24	Output pin with 24 mA source-sink capability
O12p3	3.3V output pin with 12 mA source-sink capability
O24p3	3.3V output pin with 24 mA source-sink capability
OD12	Open-drain output pin with 12 mA sink capability
OD24	Open-drain output pin with 24 mA sink capability

OD_{12p3}	3.3V open-drain output pin with 12 mA sink capability
IN_t	TTL level input pin
IN_{tp3}	3.3V TTL level input pin
IN_{td}	TTL level input pin with internal pull down resistor
IN_{tu}	TTL level input pin with internal pull up resistor
IN_{ts}	TTL level Schmitt-trigger input pin
IN_{tsp3}	3.3V TTL level Schmitt-trigger input pin
IN_c	CMOS level input pin
IN_{cu}	CMOS level input pin with internal pull up resistor
IN_{cd}	CMOS level input pin with internal pull down resistor
IN_{cs}	CMOS level Schmitt-trigger input pin
IN_{csu}	CMOS level Schmitt-trigger input pin with internal pull up resistor

1.1 LPC Interface

SYMBOL	PIN	I/O	FUNCTION
CLKIN	17	IN_{tp3}	System clock input. According to the input frequency 24MHz or 48MHz, it is selectable through register. Default is 24MHz input.
PME#	98	OD_{12p3}	Generated PME event.
PCICLK	19	IN_{tsp3}	PCI clock input.
LDRQ#	20	O_{12p3}	Encoded DMA Request signal.
SERIRQ	21	I/O_{12tp3}	Serial IRQ input/Output.
LAD[3:0]	23-26	I/O_{12tp3}	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
LFRAME#	27	IN_{tsp3}	Indicates start of a new cycle or termination of a broken cycle.
LRESET#	28	IN_{tsp3}	Reset signal. It can connect to PCIRST# signal on the host.

1.2 FDC Interface

SYMBOL	PIN	I/O	FUNCTION
DRVDEN0	1	OD_{24}	Drive Density Select bit 0.
INDEX#	2	IN_{csu}	This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
MOA#	3	OD_{24}	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
DSB#	4	OD_{24}	Drive Select B. When set to 0, this pin enables disk drive B. This is an open drain output.
DSA#	6	OD_{24}	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
MOB2#	7	OD_{24}	Motor B On. When set to 0, this pin enables disk drive 1. This is an open drain output.
DIR#	8	OD_{24}	Direction of the head step motor. An open drain output. Logic 1 = outward motion Logic 0 = inward motion
STEP#	9	OD_{24}	Step output pulses. This active low open drain output produces a pulse to move the head to another track.

WD#	10	OD_{24}	Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output.
WE#	11	OD_{24}	Write enable. An open drain output.
TRAK0#	12	IN_{csu}	Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
WP#	13	IN_{csu}	Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
RDATA#	14	IN_{csu}	The read data input signal from the FDD. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
HEAD#	15	OD_{24}	Head select. This open drain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1
DSKCHG#	16	IN_{csu}	Diskette change. This signal is active low at power on and whenever the diskette is removed. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).

1.3 Multi-Mode Parallel Port

The following pins have alternate functions, which are controlled by CR28 and L3-CRF0.

SYMBOL	PIN	I/O	FUNCTION
SLCT	29	IN_{ts}	PRINTER MODE: An active high input on this pin indicates that the printer is selected. This pin is pulled high internally. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
WE2#		OD_{12}	EXTENSION FDD MODE: WE2# This pin is for Extension FDD B; its function is the same as the WE# pin of FDC. EXTENSION 2FDD MODE: WE2# This pin is for Extension FDD A and B; its function is the same as the WE# pin of FDC.
PE	30	IN_{ts}	PRINTER MODE: An active high input on this pin indicates that the printer has detected the end of the paper. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
WD2#		OD_{12}	EXTENSION FDD MODE: WD2# This pin is for Extension FDD B; its function is the same as the WD# pin of FDC. EXTENSION 2FDD MODE: WD2# This pin is for Extension FDD A and B; its function is the same as the WD# pin of FDC.

1.3 Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
BUSY	31	IN_{ts}	PRINTER MODE: An active high input indicates that the printer is not ready to receive data. This pin is pulled high internally. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
MOB2#		OD_{12}	EXTENSION FDD MODE: MOB2# This pin is for Extension FDD B; its function is the same as the MOB# pin of FDC. EXTENSION 2FDD MODE: MOB2# This pin is for Extension FDD A and B; its function is the same as the MOB# pin of FDC.
ACK#	32	IN_{ts}	PRINTER MODE: ACK# An active low input on this pin indicates that the printer has received data and is ready to accept more data. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DSB2#		OD_{12}	EXTENSION FDD MODE: DSB2# This pin is for the Extension FDD B; its functions is the same as the DSB# pin of FDC. EXTENSION 2FDD MODE: DSB2# This pin is for Extension FDD A and B; its function is the same as the DSB# pin of FDC.
ERR#	33	IN_{ts}	PRINTER MODE: ERR# An active low input on this pin indicates that the printer has encountered an error condition. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
HEAD2#		OD_{12}	EXTENSION FDD MODE: HEAD2# This pin is for Extension FDD B; its function is the same as the HEAD#pin of FDC. EXTENSION 2FDD MODE: HEAD2# This pin is for Extension FDD A and B; its function is the same as the HEAD# pin of FDC.

1.3 Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
SLIN#	34	OD_{12}	PRINTER MODE: SLIN# Output line for detection of printer selection. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
STEP2#		OD_{12}	EXTENSION FDD MODE: STEP2# This pin is for Extension FDD B; its function is the same as the STEP# pin of FDC. EXTENSION 2FDD MODE: STEP2# This pin is for Extension FDD A and B; its function is the same as the STEP# pin of FDC.
INIT#	43	OD_{12}	PRINTER MODE: INIT# Output line for the printer initialization. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DIR2#		OD_{12}	EXTENSION FDD MODE: DIR2# This pin is for Extension FDD B; its function is the same as the DIR# pin of FDC. EXTENSION 2FDD MODE: DIR2# This pin is for Extension FDD A and B; its function is the same as the DIR# pin of FDC.
AFD#	44	OD_{12}	PRINTER MODE: AFD# An active low output from this pin causes the printer to auto feed a line after a line is printed. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DRVDEN0		OD_{12}	EXTENSION FDD MODE: DRVDEN0 This pin is for Extension FDD B; its function is the same as the DRVDEN0 pin of FDC. EXTENSION 2FDD MODE: DRVDEN0 This pin is for Extension FDD A and B; its function is the same as the DRVDEN0 pin of FDC.

1.3 Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
STB#	46	OD_{12}	PRINTER MODE: STB# An active low output is used to latch the parallel data into the printer. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		-	EXTENSION 2FDD MODE: This pin is a tri-state output.
PD0	42	I/O_{12ts}	PRINTER MODE: PD0 Parallel port data bus bit 0. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
INDEX2#		IN_{ts}	EXTENSION FDD MODE: INDEX2# This pin is for Extension FDD B; its function is the same as the INDEX# pin of FDC. It is pulled high internally.
			EXTENSION 2FDD MODE: INDEX2# This pin is for Extension FDD A and B; its function is the same as the INDEX# pin of FDC. It is pulled high internally.
PD1	41	I/O_{12ts}	PRINTER MODE: PD1 Parallel port data bus bit 1. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
TRAK02#		IN_{ts}	EXTENSION FDD MODE: TRAK02# This pin is for Extension FDD B; its function is the same as the TRAK0# pin of FDC. It is pulled high internally.
			EXTENSION. 2FDD MODE: TRAK02# This pin is for Extension FDD A and B; its function is the same as the TRAK0# pin of FDC. It is pulled high internally.
PD2	40	I/O_{12ts}	PRINTER MODE: PD2 Parallel port data bus bit 2. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
WP2#		IN_{ts}	EXTENSION FDD MODE: WP2# This pin is for Extension FDD B; its function is the same as the WP# pin of FDC. It is pulled high internally.
			EXTENSION. 2FDD MODE: WP2# This pin is for Extension FDD A and B; its function is the same as the WP# pin of FDC. It is pulled high internally.

1.3 Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
PD3	39	I/O_{12ts}	PRINTER MODE: PD3 Parallel port data bus bit 3. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
RDATA2#		IN_{ts}	EXTENSION FDD MODE: RDATA2# This pin is for Extension FDD B; its function is the same as the RDATA# pin of FDC. It is pulled high internally. EXTENSION 2FDD MODE: RDATA2# This pin is for Extension FDD A and B; its function is the same as the RDATA# pin of FDC. It is pulled high internally.
PD4	38	I/O_{12ts}	PRINTER MODE: PD4 Parallel port data bus bit 4. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DSKCHG2#		IN_{ts}	EXTENSION FDD MODE: DSKCHG2# This pin is for Extension FDD B; the function of this pin is the same as the DSKCHG# pin of FDC. It is pulled high internally. EXTENSION 2FDD MODE: DSKCHG2# This pin is for Extension FDD A and B; this function of this pin is the same as the DSKCHG# pin of FDC. It is pulled high internally.
PD5	37	I/O_{12ts}	PRINTER MODE: PD5 Parallel port data bus bit 5. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		-	EXTENSION 2FDD MODE: This pin is a tri-state output.
PD6	36	I/OD_{12ts}	PRINTER MODE: PD6 Parallel port data bus bit 6. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
MOA2#		OD_{12}	EXTENSION. 2FDD MODE: MOA2# This pin is for Extension FDD A; its function is the same as the MOA# pin of FDC.
PD7	35	I/OD_{12ts}	PRINTER MODE: PD7 Parallel port data bus bit 7. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
DSA2#		OD_{12}	EXTENSION 2FDD MODE: DSA2# This pin is for Extension FDD A; its function is the same as the DSA# pin of FDC.

1.4 Serial Port Interface

SYMBOL	PIN	I/O	FUNCTION
CTSA# CTSB#	47 55	IN_t	Clear To Send. It is the modem control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
DSRA# DSRB#	48 56	IN_t	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
RTSA# HEFRAS	49	O_8 INcd	UART A Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. During power-on reset, this pin is pulled down internally and is defined as HEFRAS, which provides the power-on value for CR26 bit 6 (HEFRAS). A 4.7 kΩ is recommended if intends to pull up. (select 4EH as configuration I/O port's address)
RTSB#	57	O_8	UART B Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
DTRA# PNPCSV#	50	O_8 INcd	UART A Data Terminal Ready. An active low signal informs the modem or data set that the controller is ready to communicate. During power-on reset, this pin is pulled down internally and is defined as PNPCSV#, which provides the power-on value for CR24 bit 0 (PNPCSV#). A 4.7 kΩ is recommended if intends to pull up. (clear the default value of FDC, UARTs, and PRT)
DTRB#	58	O_8	UART B Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
SINA SINB	51 59	IN_t	Serial Input. It is used to receive serial data through the communication link.
SOUTA PENROM#	52	O_8 INcd	UART A Serial Output. It is used to transmit serial data out to the communication link. During power on reset , this pin is pulled down internally and is defined as PENROM#, which provides the power on value for CR24 bit 1. A 4.7kΩ is recommended if intends to pull up .
SOUTB PEN48	61	O_8 INcd	UART B Serial Output. During power-on reset, this pin is pulled down internally and is defined as PEN48, which provides the power-on value for CR24 bit 6 (EN48). A 4.7 kΩ resistor is recommended if intends to pull up.
DCDA# DCDB#	53 62	IN_t	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
RIA# RIB#	54 63	IN_t	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.

1.5 Infrared Port

SYMBOL	PIN	I/O	FUNCTION
IRRX	64	IN_{ts}	Alternate Function Input: Infrared Receiver input. General purpose I/O port 3 bit 6.
IRTX	65	O_{12}	Alternate Function Output: Infrared Transmitter Output. General purpose I/O port 3 bit 7.

1.6 Flash ROM Interface

SYMBOL	PIN	I/O	FUNCTION
XA18-XA16 GP57-GP55	66-68	O_{12} I/OD_{12t}	Flash ROM interface Address[18:16] General purpose I/O port 5 bit7-5
XA15-XA10 GP47-GP42	69-74	O_{12} I/OD_{12t}	Flash ROM interface Address[15:10] General purpose I/O port 4 bit7-2
XA9-XA8 GP41-GP40	76-77	O_{12} I/OD_{12t}	Flash ROM interface Address[9:8] General purpose I/O port 4 bit1-0
XA7-XA0 GP37-GP30	78-85	O_{12} I/OD_{12t}	Flash ROM interface Address[7:0] General purpose I/O port 3 bit7-0
XD7-XD4 GP27-GP24	86-89	I/O_{12t} I/OD_{12t}	Flash ROM interface Data Bus[7:4] General purpose I/O port 2 bit7-4
XD3-XD0 GP23-GP20	91-94	I/O_{12t} I/OD_{12t}	Flash ROM interface Data Bus [3:0] General purpose I/O port 2 bit3-0
ROMCS# GP54	95	O_{12} I/OD_{12t}	Flash ROM interface Chip Select General purpose I/O port 5 bit4
MEMR# GP53	96	O_{12} I/OD_{12t}	Flash ROM interface Memory Read Enable General purpose I/O port 5 bit3
MEMW# GP52	97	O_{12} I/OD_{12t}	Flash ROM interface Memory Write Enable General purpose I/O port 5 bit2

1.7 General Purpose I/O Port

SYMBOL	PIN	I/O	FUNCTION
GP73	111	I/OD_{12t}	General purpose I/O port 7 bit3
GP80 WDTO	118	I/OD_{12t} O_{12}	General purpose I/O port 8 bit0 Watch dog timer output.
GP67	99	I/OD_{12t}	General purpose I/O port 6 bit7.
GP66	100	I/OD_{12t}	General purpose I/O port 6 bit6.
GP65	101	I/OD_{12t}	General purpose I/O port 6 bit5.
GP64	102	I/OD_{12t}	General purpose I/O port 6 bit4.
GP63	103	I/OD_{12t}	General purpose I/O port 6 bit3.
GP62	104	I/OD_{12t}	General purpose I/O port 6 bit2.
GP61	105	I/OD_{12t}	General purpose I/O port 6 bit1.
GP60	106	I/OD_{12t}	General purpose I/O port 6 bit0.

1.8 Smart Card Interface

SYMBOL	PIN	I/O	FUNCTION
SCPSNT GP77	107	IN_{ts} I/OD_{24t}	Smart card present detection Schmitt-trigger input. General purpose I/O port 7 bit7.
SCIO GP76	108	I/O_{24t} I/OD_{24t}	Smart card data I/O channel. General purpose I/O port 7 bit6.
SCCLK GP75	109	O_4 I/OD_{4t}	Smart card clock output. General purpose I/O port 7 bit5.
SCRST GP74	110	O_{24} I/OD_{24t}	Smart card reset output. General purpose I/O port 7 bit4.
SCC8 GP72	112	I/O_{24t} I/OD_{24t}	Smart card General Purpose I/O channel. General purpose I/O port 7 bit2.
SCPWR GP71	113	O_{12} I/OD_{12t}	Smart card power control. General purpose I/O port 7 bit1.
SCC4 GP70	114	I/O_{24t} I/OD_{24t}	Smart card General Purpose I/O channel. General purpose I/O port 7 bit0.

1.9 PWM & General Purpose I/O Port 8

SYMBOL	PIN	I/O	FUNCTION
PWM2	115	O_{12}	Fan speed control . Use the Pulse Width Modulation (**PWM**)
PLED		O_{12}	Power LED output, this signal is low after system reset.
GP83		I/OD_{12t}	General purpose I/O port 8 bit2-1
PWM1-0	116-117	O_{12}	Fan speed control . Use the Pulse Width Modulation (**PWM**) Techno knowledge to control the Fan's RPM.
GP82-81		I/OD_{12t}	General purpose I/O port 8 bit2-1

1.10 Game Port & MIDI Port

SYMBOL	PIN	I/O	FUNCTION
MSI	119	INcu	MIDI serial data input .
GP51		I/OD_{24c}	General purpose I/O port 5 bit 1.
MSO	120	O_{12}	MIDI serial data output.
GP50		I/OD_{12t}	General purpose I/O port 5 bit 0.
GPAS2	121	INcs	Active-low, Joystick I switch input 2. This pin has an internal pull-up resistor. (Default)
GP17		I/OD_{24cs}	General purpose I/O port 1 bit 7.
GPBS2	122	INcs	Active-low, Joystick II switch input 2. This pin has an internal pull-up resistor. (Default)
GP16		I/OD_{24cs}	General purpose I/O port 1 bit 6.
GPAY	123	I/OD_{24a}	Joystick I timer pin. this pin connect to Y positioning variable resistors for the Joystick. (Default)
GP15		I/OD_{24cs}	General purpose I/O port 1 bit 5.
GPBY	124	I/OD_{24a}	Joystick II timer pin. this pin connect to Y positioning variable resistors for the Joystick. (Default)
GP14		I/OD_{24cs}	General purpose I/O port 1 bit 4.

1.10 Game Port & MIDI Port, continued

SYMBOL	PIN	I/O	FUNCTION
GPBX	125	I/OD_{24a}	Joystick II timer pin. this pin connect to X positioning variable resistors for the Joystick. (Default)
GP13		I/OD_{24cs}	General purpose I/O port 1 bit 3.
GPAX	126	I/OD_{24a}	Joystick I timer pin. This pin connect to X positioning variable resistors for the Joystick. (Default)
GP12		I/OD_{24cs}	General purpose I/O port 1 bit 2.
GPBS1	127	Incs	Active-low, Joystick II switch input 1. This pin has an internal pull-up resistor. (Default)
GP11		I/OD_{24cs}	General purpose I/O port 1 bit 1.
GPAS1	128	Incs	Active-low, Joystick I switch input 1. This pin has an internal pull-up resistor. (Default)
GP10		I/OD_{24cs}	General purpose I/O port 1 bit 0.

1.11 POWER PINS

SYMBOL	PIN	FUNCTION
VCC	5, 45, 75,	+5V power supply for the digital circuitry.
VCC3V	22	+3.3V power supply for driving 3V on host interface.
GND	18, 60, 90,	Ground.

2. SMART CARD READER INTERFACE (SCR)

2.1 Features

Winbond's implementation of Smart Card Reader interface is based on ISO/IEC 7816-3 standard and fully compliant with PC/SC Specifications 1.0. Except for pins specified in ISO/IEC 7816-3, W83697SF's SCI also includes SCPSNT (Smart Card Present) monitoring status of card insertion/extraction, SCLED (Smart Card traffic LED display) which is active high when host is accessing information to/from card, and two general-purpose I/O pins SCC4 and SCC8 (only available in W83697SF) for users to design application-specific functions.

Register file (control and status registers) of Winbond's Smart Card interface is designed in an UART-like structure so that users with previous UART experience should have no trouble to implement Winbond's SCI applications.

Power consumption is minimized by sophisticated device's operation scheme.

2.2 Register file

Complete register file table

Bit Number										
Register file		**Abbr.**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Base + 0 BDLAB = 0	Receiver Buffer Register (Read only)	RBR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Base + 0 BDLAB = 0	Transmitter Buffer Register (Write only)	TBR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Base + 1 BDLAB = 0	Interrupt Enable Register	IER	SCC8	SCC4	SCC8_IO (note)	SCC4_IO (note)	ESCPTI (note)	ESCSRI (note)	ETBREI (note)	ERDRI (note)
	default		x	x	0	0	0	0	0	0
Base + 2 BDLAB = 0	Interrupt Status Register (Read only)	ISR	FIFO enabled	FIFO enabled	SCPSNT	SCPTI (note)	INTS2 (note)	INTS1 (note)	INTS0 (note)	Interrupt pending
Base + 2 BDLAB = 0	Smart Card FIFO control Register (Write only)	SCFR	RxTL1 (note)	RxTL0 (note)	Reserved	Reserved	Reserved	TxFRST (note)	RxFRST (note)	Enable FIFO
	default		0	0	x	x	x	0	0	0
Base + 3	Smart Card Control Register	SCCR	BDLAB (note)	Reserved	Reserved	EPE (note)	PBE (note)	Reserved	Reserved	SC_SEL
	default		0	x	x	0	0	x	x	0
Base + 4	Clock Base Register	CBR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	default		0	0	0	0	1	1	0	0
Base + 5	Smart Card Status Register (Read only)	SCSR	RxFEI (note)	TSRE (note)	TBRE (note)	SBD (note)	NSER (note)	PBER (note)	OER (note)	RDR (note)
Base + 6	Guard Time Register	GTR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	default		0	0	0	0	0	0	0	1
Base + 7	Extended Control Register	ECR	Cold reset	Reserved	SCKFS1 (note)	SCKFS0 (note)	CLKSTPL (note)	CLKSTP (note)	SCIODIR (note)	Warm reset
	default		0	x	0	1	0	0	1	0
Base + 0 BDLAB = 1	Baud rate divisor Latch Lower byte	BLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	default		0	0	0	1	1	1	1	1
Base + 1 BDLAB = 1	Baud rate divisor Latch Higher byte	BLH	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	default		0	0	0	0	0	0	0	0

Base + 2 BDLAB = 1	Smart Card ID number (Read only)		0	1	1	1	0	0	0	0

Note:

Abbreviation explanation (in alphabetical order) –

BDLAB – Baud rate divisor latch access bit.

CLKSTP – Stop Smart Card interface's clock SCCLK.

CLKSTPL – Set SCCLK level when CLKSTP is "1".

EPE – Even parity enable.

ERDRI – Enable RBR (Receiver Buffer Register) data ready interrupt.

ESCPTI - Enable SCPSNT interrupt.

ESCSRI - Enable interrupts of SCSR (read only Smart Card Status Register at base address + 5) events.

ETBREI – Enable TBR (write only Transmitter Buffer Register at base address + 0) empty interrupt.

INTS2 ~ INTS0 – Interrupt status bits. Refer to description of ISR (read only Interrupt Status Register at base address + 2) for details.

NSER – No stop bit error.

OER – Overrun error.

PBE – Parity bit enable.

PBER – Parity bit error.

RDR – Receiver data ready status.

RxFEI – Receiver FIFO error indication.

RxFRST – Receiver FIFO reset.

RxTL1 ~ RxTL0 – Receiver threshold level setting bits. Refer to description of SCFR (write only Smart Card FIFO control register at base address + 2) for details.

SBD – Silent byte detected.

SCIODIR – SCIO direction bit (0/1 mean output/input respectively).

SCKFS1 ~ SCKFS0 – Smart Card interface clock frequency selection bits. Refer to description of ECR (Extended Control Register at base address + 7) for details.

SCPTI – SCPSNT toggle interrupt status.

SC_SEL – Smart Card socket selection.

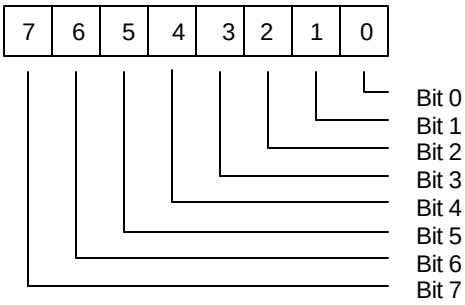
TBRE – TBR (write only Transmitter Buffer Register at base address + 0) empty status.

TSRE – TSR (Transmitter shift register) empty status.

TxFRST – Transmitter FIFO reset.

Receiver Buffer Register (RBR at base address + 0 when BDLAB = 0, read only)

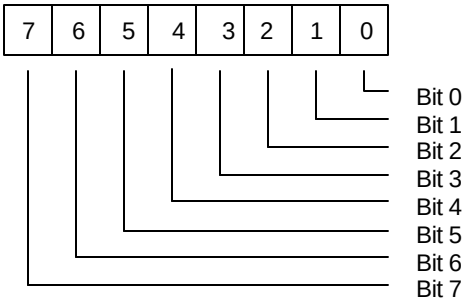
This register is the access port for receiver FIFO. It is active when Smart Card interface is in input mode with SCIODIR (bit 1 of ECR at base address + 7) set to "1". The depth of receiver FIFO is 16 bytes.



Bit 7 ~ bit 0: Access port for receiver FIFO.

Receiver Buffer Register (RBR at base address + 0 when BDLAB = 0, read only)

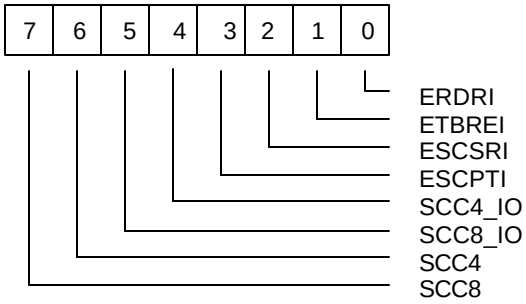
This register is the access port for transmitter FIFO. It is active when Smart Card interface is in output mode with SCIODIR (bit 1 of ECR at base address + 7) set to "0". The depth of transmitter FIFO is 16 bytes.



Bit 7 ~ bit 0: Access port for receiver FIFO.

Interrupt Enable Register (IER at base address + 1 when BDLAB = 0)

This register includes four control bits to enable interrupt events. The other four bits are allocated for control of general-purpose I/O pins which are usually connected to C4 and C8 pads of a smart card for application specific function.



Bit 7: SCC8 means Smart Card C8 pad. When SCC8_IO (bit 5) is set to "0" for output mode, this bit controls the voltage level of SCC8 pin which is high when SCC8 is set to "1" and low for setting of "0". Its value reflects what could be observed on SCC8 pin when SCC8_IO is set to "1" for input mode with the same convention as in output mode.

Bit 6: SCC4 means Smart Card C4 pad. When SCC4_IO (bit 4) is set to "0" for output mode, this bit controls the voltage level of SCC4 pin which is high when SCC4 is set to "1" and low for setting of "0". Its value reflects what is observed on SCC4 pin when SCC4_IO is set to "1" for input mode with the same convention as in output mode.

Bit 5: SCC8_IO means input/output direction control for SCC8 pin.

= 0 SCC8 is in output mode.

= 1 SCC8 is in input mode.

Bit 4: SCC4_IO means input/output direction control for SCC4 pin.

= 0 SCC4 is in output mode.

= 1 SCC4 is in input mode.

Bit 3: ESCPTI means SCPSNT toggle interrupt enable bit. A rising/falling edge of SCPSNT signal triggers an interrupt if this bit is set to "1".

= 0 SCPSNT toggle interrupt is disabled.

= 1 SCPSNT toggle interrupt is enabled.

Bit 2: ESCSRI means interrupt enable bit for SCSR-related events such as silent byte detected error, no stop bit error, parity bit error or overrun error. Any SCSR-related event as described above will trigger an interrupt if this bit is set to "1".

= 0 SCSR-related event interrupt is disabled.

= 1 SCSR-related event interrupt is enabled.

Bit 1: ETBREI means interrupt enable bit for TBR (Transmitter Buffer Register) empty condition. An interrupt is issued when TBR is empty and this bit is set to "1". It is used in output mode (SDIODIR = 0) to request host's attention to transfer data byte to card.

= 0 TBR empty interrupt is disabled.

= 1 TBR empty interrupt is enabled.

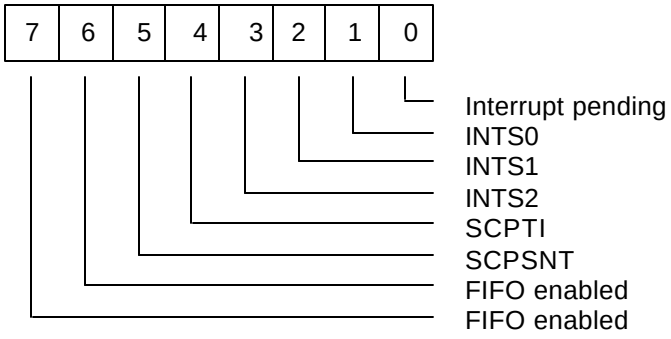
Bit 0: ERDRI means interrupt enable bit for receiver data ready status. The active FIFO threshold level for this kind of interrupt when FIFO is enabled is specified in RxTL1 and RxTL0 (bit 7 and bit 6 of SCFR at base address + 2. Refer to description of SCFR for details). An interrupt is issued if a data byte is ready for host to read when FIFO is disabled or incoming data from card reaches active FIFO threshold level when FIFO is enabled.

= 0 Receiver data ready interrupt is disabled.

= 1 Receiver data ready interrupt is enabled.

Interrupt Status Register (ISR at base address + 2 when BDLAB = 0, read only)

This register contains mainly interrupt status including transmission-related interrupts and SCPSNT toggle interrupt. Transmission-related interrupt status is coded and prioritized as in UART implementation. User may also find FIFO enable/disabled status reflecting what is set in bit 0 of SCFR (write only Smart Card FIFO Register at base address + 2 when BDLAB = 0) and SCPSNT line status.



Bit 7, 6: FIFO enabled status bits reflect what is set in bit 0 of SCFR (write only Smart Card FIFO Register at base address + 2 when BDLAB = 0).

Bit 5: SCPSNT line status. User may poll this bit to see SCPSNT pin's voltage level.

Bit 4: SCPTI means SCPSNT toggle interrupt status. A rising/falling edge of SCPSNT signal triggers an interrupt and set this status bit if ESCPTI (IER bit 3) is set to "1" to enable SCPSNT toggle interrupt.

= 0 No SCPSNT toggle interrupt.
= 1 SCPSNT toggle interrupt occurs.

Bit 3 ~ 1: INTS2 ~ INTS0 mean interrupt status bit 2 ~ 0. The combination indicates which kind of transmission-related interrupt has occurred. Refer to the following table for details.

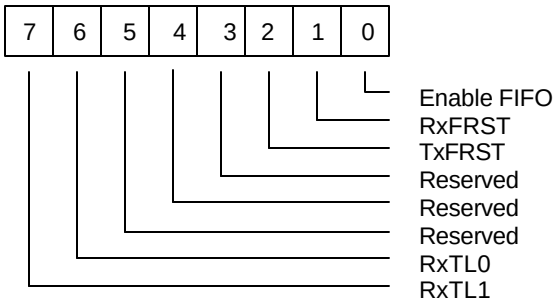
ISR bit				Interrupt set and function			
3	2	1	0	Priority	Interrupt type	Interrupt source	Clear interrupt condition
0	0	0	1	-	-	No interrupt pending	-
0	1	1	0	first	Data receiving status	1. OER = 1 2. PBER = 1 3. NSER = 1 4. SBD = 1	Read SCSR
0	1	0	0	second	RBR data ready	1. RBR data ready 2. FIFO interrupt active level reached	1. Read RBR 2. Read RBR until FIFO is under active level
1	1	0	0	second	FIFO data time out	Data present in Rx FIFO for 4-character period of time since last access of Rx FIFO.	Read RBR
0	0	1	0	third	TBR empty	TBR empty	1. Write data to TBR 2. Read ISR (if priority is third)

Bit 0: Interrupt pending status bit. This bit is a logical "1" if there is no interrupt pending. If one of the interrupt sources occurs, this bit will be set to a logical "0".

= 0 Interrupt pending.
= 1 No interrupt occurs.

Smart Card FIFO control Register (SCFR at base address + 2 when BDLAB = 0, write only)

This register controls FIFO function of Smart Card interface.



Bit 7, 6: RxTL1 and RxTL0 mean receiver FIFO active threshold level control bits. These two bits are used to set the active level for the receiver FIFO interrupt. For example, if the interrupt active level is set as 4 bytes, once there are at least 4 data characters in the receiver FIFO, an interrupt is activated to notify host to read data from FIFO. Default to be 00b.

RxTL1	RxTL0	Rx FIFO Interrupt Active Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

Bit 5 ~ 3: Reserved.

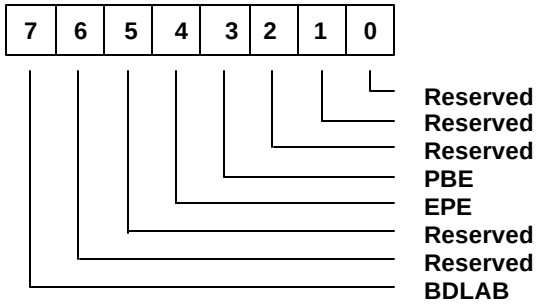
Bit 2: TxFRST means transmitter FIFO reset control bit. Setting this bit to a logical "1" resets the transmitter FIFO counter to initial state. This bit is self-cleared to "0" after being set to "1". Default is "0".

Bit 1: RxFRST means receiver FIFO reset control bit. Setting this bit to a logical "1" resets the receiver FIFO counter to initial state. This bit is self-cleared to "0" after being set to "1". Default is "0".

Bit 0: This bit enables FIFO of Smart Card interface. It should be set to a logical "1" before other bits of SCFR are programmed. Default is "0".

Smart Card Control Register (SCCR at base address + 3)

In contrast to its UART counterpart, Smart Card Control Register only controls parity bit setting because data length is fixed at 8-bit long for Smart Card interface protocol.



Bit 7: BDLAB means baud rate divisor latch access bit. When this bit is set to a logical "1", users may access baud rate divisor (in 16-bit binary format) through divisor latches (BLH and BLL) of baudrate generator during a read/write operation. A special Smart Card ID can also be read at base address + 2 when BDLAB is "1". When this bit is set to "0", accesses to base address + 0, 1 or 2 refer to RBR/TBR, IER or ISR/SCFR respectively.

Bit 6 ~ 5: Reserved.

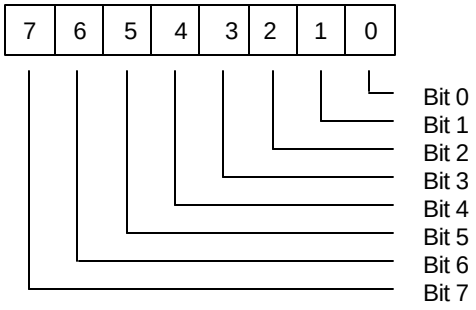
Bit 4: EPE means even parity enable. This bit is only available when bit 3 of SCCR is programmed to "1". It prescribes number of logical 1s in a data word including parity bit. When this bit is set to "1", even parity is required for transmission and reception. Odd parity is demanded when this bit is set to "0".

Bit 3: PBE means parity bit enable. When this bit is set, a parity bit is inserted between last data bit and stop bit for transmission integrity check.

Bit 2 ~ 0: Reserved.

Clock Base Register (CBR at base address + 4, default 0Ch)

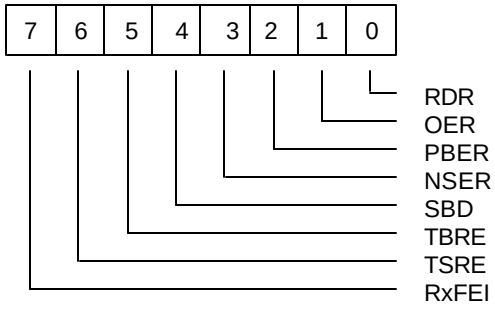
This register combining with BLH and BLL (baud rate latches) determine internal sampling clock frequency. For example, CBR defaults to be 0Ch and BLH, BLL default to be 1Fh which mean SCCLK clock frequency is 372 (12 x 31) times of internal sampling clock frequency. The default values of CBR, BLH and BLL are corresponding to default values of transmission factors F and D specified in ISO/IEC 7816-3. The value of 0Ch of CBR means there're 12 sampling clock pulses to detect a 1-etu (elementary time unit) data bit on SCIO signal. It is recommended that user sets CBR to be around 16 to maintain better data integrity and transmission stability.



Bit 7 ~ 0: Clock base value. It specifies number of internal sampling clock pulses for a data bit. Default to be 0Ch.

Smart Card Status Register (SCSR at base address + 5)

This 8-bit register provides information about status of data transfer during communication.



Bit 7: RxFEI means receiver FIFO error indication. This bit is set to "1" when there is at least one parity bit error, no stop bit error or silent byte detected error in receiver FIFO. It is cleared by reading from SCSR if there is no remaining error left in receiver FIFO.

Bit 6: TSRE means transmitter shift register empty. This bit is set to "1" when transmitter shift register is empty.

Bit 5: TBRE means transmitter buffer register empty. In non-FIFO mode, this bit will be set to a logical 1 when a data byte is transferred from TBR to TSR. If ETBREI of IER is a logical 1, an interrupt is generated to notify host to write the following data bytes. In FIFO mode, this bit is set to "1" when the transmitter FIFO is empty. It is cleared to "0" when host writes data bytes into TBR or FIFO.

Bit 4: SBD means silent byte detected. This bit is set to "1" to indicate that received data byte are kept in silent state for a full byte time, including start bit, data bits, parity bit, and stop bits. In FIFO mode, it indicates the same condition for the data on top of FIFO. When host reads SCSR, it clears this bit to "0".

Bit 3: NSER means no stop bit error. This bit is set to "1" to indicate that received data has no stop bit. In FIFO mode, it indicates the same condition for the data on top of FIFO. When host reads SCSR, it clears this bit to "0".

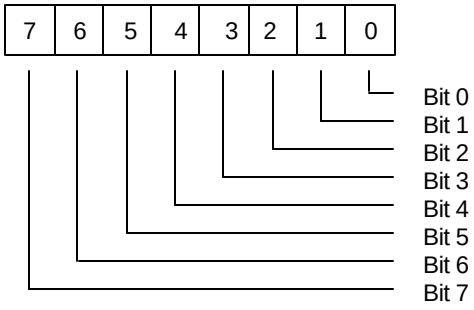
Bit 2: PBER means parity bit error. This bit is set to "1" to indicate that parity bit of received data is wrong. In FIFO mode, it indicates the same condition for the data on top of the FIFO. When host reads SCSR, it clears this bit to "0".

Bit 1: OER means overrun error. This bit is set to "1" to indicate previously received data is overwritten by the next received data before it is read by host. In FIFO mode, it indicates the same condition instead of FIFO full. When host reads SCSR, it clears this bit to "0".

Bit 0: RDR means receiver data ready. This bit is set to "1" to indicate received data is ready to be read by host in RBR or FIFO. If no data are left in RBR or FIFO, the bit is cleared to "0".

Guard Time Register (GTR at base address + 6, default 01h)

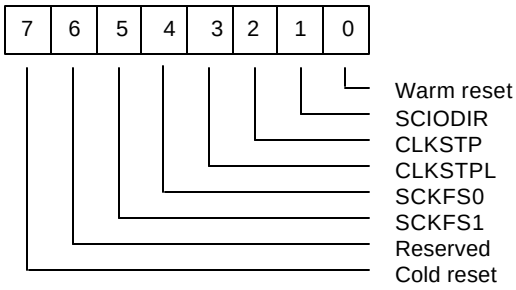
This register specifies number of stop bits appended in the end of data byte.



Bit 7 ~ 0: Guard time values. Default to be 01h.

Extended Control Register (ECR at base address + 7, default 12h)

This register contains reset control bits, clock frequency selection bits, clock stop control bits and SCIO direction control bit.



Bit 7: Cold reset. Setting "1" to this bit turns off power to Smart Card interface by pulling up SCPWR#. SCCLK is stopped, SCRST# kept low, SCIO in input mode and SCLED is inactive. ECR's SCIODIR, SCKFS1 and SCKFS0 control bits and control bits in CBR, GTR, BLH and BLL are cleared to default values. User must write a "0" to this bit to recover to normal state.

Bit 6: Reserved.

Bit 5, 4: SCKFS1 and SCKFS0 means SCCLK frequency selection bit 1 and 0. They selects working clock frequency as following table. Default values are 01h.

SCKFS1, SCKFS0	SCCLK frequency
00	1.5 MHz
01	3.0 MHz
10	6.0 MHz
11	12 MHz

Bit 3: CLKSTP means clock stop control bit. Setting "1" to this bit stops SCCLK at a voltage level specified by CLKSTPL (bit 2 of ECR).

Bit 2: CLKSTPL means clock stop voltage level.

= 0 SCCLK stops at low if CLKSTP is also set to "1".

= 1 SCCLK stops at high if CLKSTP is also set to "1".

Bit 1: SDIODIR means SDIO direction.

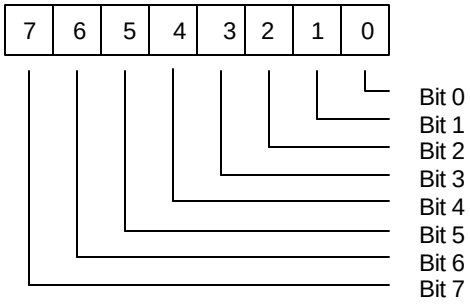
= 0 SDIO is in output mode.

= 1 SDIO is in input mode.

Bit 0: Warm reset. Setting "1" to this bit pulls down SCRST#. SCCLK is stopped, SCIO in input mode and SCLED is inactive. ECR's SCIODIR, SCKFS1 and SCKFS0 control bits and control bits in CBR, GTR, BLH and BLL are cleared to default values. User must write a "0" to this bit to recover to normal state. This bit is similar to cold reset except SCPWR# stays active low.

Baud rate divisor Latch Lower byte (BLL at base address + 0 when BDLAB = 1, default 1Fh)

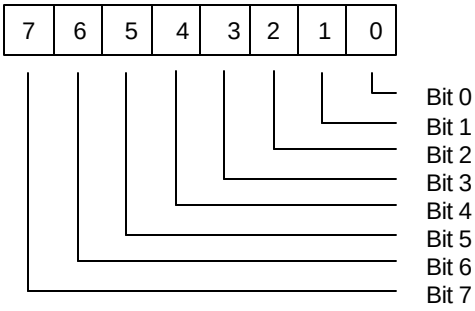
This register combining with BLH and CBR determine internal sampling clock frequency.



Bit 7 ~ 0: Baud rate divisor latch lower byte values. Default to be 1Fh.

Baud rate divisor Latch Higher byte (BLH at base address + 1 when BDLAB = 1, default 00h)

This register combining with BLL and CBR determine internal sampling clock frequency.



Bit 7 ~ 0: Baud rate divisor latch higher byte values. Default to be 00h.

2.3 Smart Card ID number (base address + 2 when BDLAB = 1, fixed at 70h)

This register contains a specific value of 70h for driver to identify Smart Card interface.

2.4 Functional description

The following description uses abbreviations to refer to control/status registers and their contents of Smart Card interface. Also, PnP resources of Smart Card interface are assumed to have been programmed and allocated appropriately by system BIOS.

2.5 Initialization

User needs to program control registers so that ATR (Answer To Reset) data streams can be properly decoded after card insertion. Initialization settings include the following steps where sequential order is irrelevant.

1. BLH, BLL and CBR are written with 00h, 1Fh and 0Ch respectively to comply with default transmission factors Fd and Dd which are 372 and 1 as specified in ISO/IEC 7816-3.
2. GTR is programmed with 01h for one stop bit.
3. Set SCFR bit 1 to "1" to enable FIFO.
4. PBE needs to be "1" for parity bit enable but EPE is optional.
5. Set SDIODIR to "1" to put SDIO in reception mode.
6. Set SCKFS1 and SCKFS0 to "01" to select 3 MHz for SCCLK.

Most default values of above control bits are designed as specified in initialization step but it is recommended that user performs all the initialization sequence to avoid any ambiguity.

The relationship between transmission factors and settings of BLH, BLL and CBR is best described in the following example.

$$1\text{etu} = \frac{F}{D} \times \frac{1}{f} \text{ (f means SCCLK frequency)}$$

Therefore,

$$\frac{Fd}{Dd} = \frac{372}{1} = (BLH, BLL) \times CBR = 31 \times 12$$

2.6 Activation

Card insertion pulls up SCPSNT (assuming SCPSNT is active high with CRF0 bit 0 SCPSNT_POL = 0) and in consequence SCPWR# is pulled down to activate power MOS to supply power to card slot after a delay of about 5 ms. This delay is for card slot mechanism to settle down before power is actually applied.

SCCLK starts to output clocks right after SCPWR# is active while SCIO is in reception mode and pulled up externally. SCRST# keeps low initially to reset card but will output high after 512 clock cycles to meet requirement of tb of more than 400 clock cycles (specified in ISO/IEC 7816-3).

To meet another timing requirement, tc of ISO/IEC 7816-3, a counter based on SCCLK is implemented to start counting on the rising edge of SCRST#. SCPWR# is deactivated if no ATR (Answer To Reset) is detected after 65536 clock cycles from the rising edge of SCRST#.

2.7 Answer-to-Reset

Answer-to-Reset (ATR) is the data streams sent by the card to the interface as an answer to a reset on SCRST# signal. Refer to ISO/IEC 7816-3 for detailed description of ATR.

There're two kind of cards specified in ISO/IEC 7816-3, inverse convention card and direct convention card. Although these two conventions treat logical meanings (0 or 1) of voltage levels (low or high) differently, Winbond's implementation of Smart Card interface decodes a high voltage level data bit as "1" and low voltage level data bit "0" nevertheless and resorts to software to interpret incoming data. Software driver needs to interpret initial character of ATR first to determine which convention is for inserted card and chooses a conversion procedure for it. Subsequent incoming data bytes must be passed through a conversion procedure before actually transfers these data bytes to host. Similar conversion procedure must be applied to outgoing data byte before writing to TBR too.

For example, the raw data byte for initial character of inverse-convention ATR would be 03h. Software driver therefore needs a conversion procedure to reverse bit-significance and polarity to process subsequent raw data bytes. On the other hand, initial character of direct-convention ATR is 3Bh which needs no conversion procedure to process data byte.

2.8 Data transfer

Software driver might need to configure control registers again based on information contained in ATR before process subsequent data transfer. The following guidelines are provided for programming reference.

1. EPE should be set to "1" for direct-convention card and otherwise for inverse-convention card.
2. BLH, BLL and CBR should be set to comply with Fi and Di.
3. GTR is used for various stop bit requirement of different transmission protocols.
4. SCIODIR controls direction of data transfer.
5. Use interrupt resources to control communication sequence.
6. Monitor SCSR for transmission integrity.

2.9 Cold reset and warm reset

Cold reset is achieved by writing a "1" to bit 7 of ECR. It deactivates SCPWR# to high. Consequentially, SCRST# is pulled down and SCCLK is stopped. User must write a "0" to ECR bit 7 to resume Smart Card interface to a normal activation state as described in section 2.3 assuming card is still present.

Writing a "1" to ECR bit 0 triggers a warm reset. This is a self-cleared reset operation unlike cold reset which needs explicit cancellation. Its effect is similar to cold reset except SCPWR# is kept activated and therefore power supply to card stays on.

2.10 Power states

W83697SF employs a sophisticated algorithm to partition Smart Card interface's internal circuits to achieve optimal power utilization. However, users must pay extra care in the design of application circuits following guidelines stated below to prevent potential signal conflict and unnecessary power consumption.

There're four power states: disabled state, active state, idle state and power down state. Disabled state is the default state when power is first applied to the IC. Active state is entered by setting a "1" to enable bits at bit 0 of CR30 in logical device 0 (refer to Configuration Register section for details). Idle state means that I/O pins of deselected socket output a predetermined voltage level to disable power to socket and to prevent leakage from floating connections while Smart Card interface core circuits might still be servicing other selected socket. SCPWD (Smart Card Power Down, bit 7 of CR22 global control register) controls whether in active state (SCPWD = 0) or in power down state (SCPWD = 1).

2.11 Disabled state

Smart Card interface is in disabled state initially. Clock is stopped in this state and therefore it is the least power-consuming state. To prevent current leakage from floating connections, it is designed to output a predetermined voltage level on all the I/O pins of Smart Card interface as follows:

SCPWR# outputs high to disable power supply to socket;

SCRST#, SCCLK, SCIO, SCC4, SCC8 and SCLED output low;

SCPSNT is tri-stated.

These I/O conditions also apply to both socket A and socket B in power down state (SCPWD = 1) or deselected socket in idle state. Designers of application circuits must take extra care so that no contention occurs when Smart Card interface is in those power-saving states. Please refer to Winbond's recommended application circuit for example.

2.12 Active state

Active state is when Smart Card interface is actually performing all its functions: configuration of control and interrupt registers, detection of card insertion/extraction, reception of ATR (Answer To Reset) packet and communication of information between host and card. Refer to section 2.3 for detailed function description.

Smart Card interface enters active state by setting a "1" to bit 0 of CR30 in logical device 0. This is the most power-consuming state and actual power consumption is dependent on traffic of interface.

2.13 Idle state

W83697SF supports up to two Smart Card sockets. Only one socket could be active at a time and the other deselected socket is considered to be in idle state. Selection of active socket is controlled through socket selection bits which are bits 0 at base address + 3. I/O pins of deselected socket also output a predetermined voltage level as described in section 2.4.1. Power consumption in this state is similar to active state because one of the two sockets is selected and core circuit is still functioning.

There is no idle state for W83697SF because only one Smart Card socket is supported and it is always selected.

2.14 Power down state

Transition from active state to power down state is accomplished by setting SCPWD to "1". Clock is stopped for most internal core circuits except detection circuit for SCPSNT toggle (card insertion/extraction). SCPWD could be reset by SCPSNT toggle and through this feature Smart Card interface in power down state can be waken up by card insertion/extraction. User may also directly write a "0" to SCPWD to wake up Smart Card interface.

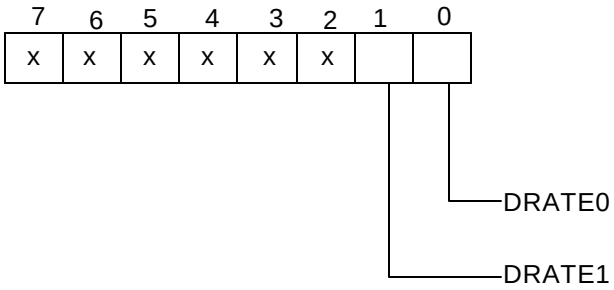
Smart Card interface spends a little bit more power to maintain SCPSNT toggle detection circuit in power down state than in disabled state while spares even more power than in active state by stopping clock to core circuit.

Users must make sure that all on-going transactions are concluded before putting Smart Card interface into power down state to prevent potential miss-operation of internal state machine.

3. CONFIGURATION REGISTER

3.1 Plug and Play Configuration

The W83697SF uses Compatible PNP protocol to access configuration registers for setting up different types of configurations. In W83697SF, there are eleven Logical Devices (from Logical Device 0 to Logical Device B with the exception of logical device 4 for backward compatibility) which correspond to eleven individual functions: FDC (logical device 0), PRT (logical device 1), UART1 (logical device 2), UART2 (logical device 3), CIR (Consumer IR, logical device 6), GPIO1 (logical device 7), GPIO5(logical device 8),GPIO2 ~GPIO4(logical device 9), ACPI ((logical device A), and Hardware monitor (logical device B). Each Logical Device has its own configuration registers (above CR30). Host can access those registers by writing an appropriate logical device number into logical device select register at CR7.



3.2 Compatible PnP

3.2.1 Extended Function Registers

In Compatible PnP, there are two ways to enter Extended Function and read or write the configuration registers. HEFRAS (CR26 bit 6) can be used to select one out of these two methods of entering the Extended Function mode as follows:

HEFRAS	address and value
0	write 87h to the location 2Eh twice
1	write 87h to the location 4Eh twice

After Power-on reset, the value on RTSA# (pin 49) is latched by HEFRAS of CR26. In Compatible PnP, a specific value (87h) must be written twice to the Extended Functions Enable Register (I/O port address 2Eh or 4Eh). Secondly, an index value (02h, 07h-FFh) must be written to the Extended Functions Index Register (I/O port address 2Eh or 4Eh same as Extended Functions Enable Register) to identify which configuration register is to be accessed. The designer can then access the desired configuration register through the Extended Functions Data Register (I/O port address 2Fh or 4Fh).

After programming of the configuration register is finished, an additional value (AAh) should be written to EFERs to exit the Extended Function mode to prevent unintentional access to those configuration

registers. The designer can also set bit 5 of CR26 (LOCKREG) to high to protect the configuration registers against accidental accesses.

The configuration registers can be reset to their default or hardware settings only by a cold reset (pin MR = 1). A warm reset will not affect the configuration registers.

3.2.2 Extended Functions Enable Registers (EFERs)

After a power-on reset, the W83697SF enters the default operating mode. Before the W83697SF enters the extended function mode, a specific value must be programmed into the Extended Function Enable Register (EFER) so that the extended function register can be accessed. The Extended Function Enable Registers are write-only registers. On a PC/AT system, their port addresses are 2Eh or 4Eh (as described in previous section).

3.2.3 Extended Function Index Registers (EFIRs), Extended Function Data Registers(EFDRs)

After the extended function mode is entered, the Extended Function Index Register (EFIR) must be loaded with an index value (02h, 07h-FEh) to access Configuration Register 0 (CR0), Configuration Register 7 (CR07) to Configuration Register FE (CRFE), and so forth through the Extended Function Data Register (EFDR). The EFIRs are write-only registers with port address 2Eh or 4Eh on PC/AT systems; the EFDRs are read/write registers with port address 2Fh or 4Fh on PC/AT systems.

3.3 Configuration Sequence

To program W83697SF configuration registers, the following configuration sequence must be followed:

(1). Enter the extended function mode

(2). Configure the configuration registers

(3). Exit the extended function mode

3.3.1 Enter the extended function mode

To place the chip into the extended function mode, two successive wrtites of 0x87 must be applied to Extended Function Enable Registers(EFERs, i.e. 2Eh or 4Eh).

3.3.2 Configurate the configuration registers

The chip selects the logical device and activates the desired logical devices through Extended Function Index Register(EFIR) and Extended Function Data Register(EFDR). EFIR is located at the same address as EFER, and EFDR is located at address (EFIR+1).
First, write the Logical Device Number (i.e.,0x07) to the EFIR and then write the number of the desired logical device to the EFDR. If accessing the Chip(Global) Control Registers, this step is not required.
Secondly, write the address of the desired configuration register within the logical device to the EFIR and then write (or read) the desired configuration register through EFDR.

3.3.3 Exit the extended function mode

To exit the extended function mode, one write of 0xAA to EFER is required. Once the chip exits the extended function mode, it is in the normal running mode and is ready to enter the configuration mode.

3.3.4 Software programming example

The following example is written in Intel 8086 assembly language. It assumes that the EFER is located at 2Eh, so EFIR is located at 2Eh and EFDR is located at 2Fh. If HEFRAS (CR26 bit 6) is set, 4Eh can be directly replaced by 4Eh and 2Fh replaced by 4Fh.

```
;-------------------------------------------------------------------------------
; Enter the extended function mode ,interruptible double-write    |
;-------------------------------------------------------------------------------
MOV    DX,2EH
MOV AL,87H
OUT    DX,AL
OUT    DX,AL
;-------------------------------------------------------------------------------
; Configurate logical device 1, configuration register CRF0   |
;-------------------------------------------------------------------------------
MOV    DX,2EH
MOV    AL,07H
OUT    DX,AL           ; point to Logical Device Number Reg.
MOV    DX,2FH
MOV    AL,01H
OUT    DX,AL           ; select logical device 1
;
MOV    DX,2EH
MOV    AL,F0H
OUT    DX,AL           ; select CRF0
MOV    DX,2FH
MOV AL,3CH
OUT    DX,AL           ; update CRF0 with value 3CH
;----------------------------------------
; Exit extended function mode    |
;----------------------------------------
MOV    DX,2EH
MOV AL,AAH
OUT    DX,AL
```

3.4 Chip (Global) Control Register

CR02 (Default 0x00) (Write only)

Bit [7:1]: Reserved.

Bit 0 = 1 SWRST --> Soft Reset.

CR07

Bit [7:0]: LDNB7 - LDNB0 --> Logical Device Number Bit 7 - 0

CR20 (read only)

Bit [7:0]: DEVIDB7 - DEBIDB0 --> Device ID Bit 7 - Bit 0

= 0x 68 (for W83697SF)

CR21 (read only)

Bit [7:0]: DEVREVB7 - DEBREVB0 --> Device Rev

= 0x0X (for W83697SF)

X : Version change number. (Bit [3:0]) --> begin from 1

CR22 (Default 0xef)

Bit 7: SCPWD

0 Power down

1 No Power down

Bit 6: Reserved

Bit 5: Reserved

Bit 4: Reserved

Bit 3: URBPWD

0 Power down

1 No Power down

Bit 2: URAPWD

0 Power down

1 No Power down

Bit 1: PRTPWD

0 Power down

1 No Power down

Bit 0: FDCPWD

0 Power down

1 No Power down

CR23 (Default 0xfe)

Bit [7:1]: Reserved.

Bit 0: IPD (Immediate Power Down).

When set to 1, it will put the whole chip into power down mode immediately.

CR24 (Default 0s1000ss)

Bit 7: Flash ROM I/F Address Segment (000F0000h ~ 000FFFFFh) enable/disable

0 Enable

1 Disable

Bit 6: CLKSEL(Enable 48Mhz)

0 The clock input on Pin 1 should be 24 MHz.

1 The clock input on Pin 1 should be 48 MHz.

The corresponding power-on setting pin is SOUTB (pin 61).

Bit [5:4]: ROM size select

00 1M

01 2M

10 4M

11 Reserved

Bit 3: MEMW# Select (PIN97)

0 MEMW# Disable

1 MEMW# Enable

Bit 2: Flash ROM I/F Address Segment (000E0000h ~ 000EFFFFh) enable/disable

0 Enable

1 Disable

Bit 1 : Enable Flash ROM Interface

0 Flash ROM Interface is enabled after hardware reset

1 Flash ROM Interface is disabled after hardware reset

The corresponding power-on setting pin is PENROM#(pin 52)

Bit 0: PNPCSV

0 The Compatible PnP address select registers have default values.

1 The Compatible PnP address select registers have no default value.

The corresponding power-on setting pin is DTRA# (pin 50).

CR25 (Default 0x00)

Bit 7: SCTRI

Bit 6: Reserved

Bit 5: Reserved

Bit 4: Reserved

Bit 3: URBTRI

Bit 2: URATRI

Bit 1: PRTTRI

Bit 0: FDCTRI

CR26 (Default 0x00)

Bit 7: SEL4FDD

0 Select two FDD mode.

1 Select four FDD mode.

Bit 6: HEFRAS

These two bits define how to enable Configuration mode. The corresponding power-on setting pin is RTSA #(pin 49).

HEFRAS Address and Value

0 Write 87h to the location 2E twice.

1 Write 87h to the location 4E twice.

Bit 5: LOCKREG

- 0 Enable R/W Configuration Registers.
- 1 Disable R/W Configuration Registers.

Bit 4: Reserved

Bit 3: DSFDLGRQ

- 0 Enable FDC legacy mode on IRQ and DRQ selection, then DO register bit 3 is effective on selecting IRQ
- 1 Disable FDC legacy mode on IRQ and DRQ selection, then DO register bit 3 is not effective on selecting IRQ

Bit 2: DSPRLGRQ

- 0 Enable PRT legacy mode on IRQ and DRQ selection, then DCR bit 4 is effective on selecting IRQ
- 1 Disable PRT legacy mode on IRQ and DRQ selection, then DCR bit 4 is not effective on selecting IRQ

Bit 1: DSUALGRQ

- 0 Enable UART A/C legacy mode IRQ selecting, then HCR bit 3 is effective on selecting IRQ
- 1 Disable UART A/C legacy mode IRQ selecting, then HCR bit 3 is not effective on selecting IRQ

Bit 0: DSUBLGRQ

- 0 Enable UART B/D legacy mode IRQ selecting, then HCR bit 3 is effective on selecting IRQ
- 1 Disable UART B/D legacy mode IRQ selecting, then HCR bit 3 is not effective on selecting IRQ

CR28 (Default 0x00)

Bit [7:4]: Reserved.

Bit [3]: Flash ROM I/F Address Segment (FFE80000h ~ FFEFFFFFh) enable/disable

- 0 Disable
- 1 Enable

Bit [2:0]: PRTMODS2 - PRTMODS0

- 0xx Parallel Port Mode
- 100 Reserved
- 101 External FDC Mode
- 110 Reserved

111 External two FDC Mode

CR29 (GPIO1,5(50~51) & Game port & MIDI port Select. Default 0x00)

Bit 7: Port Select (select Game Port or General Purpose I/O Port 1)

0 Game Port

1 General Purpose I/O Port 1 (pin121~128 select function GP10~GP17)

Bit [6:5]: (Pin119)

00 MSI

01 Reserved

10 Reserved

11 GP51

Bit [4:3]: (Pin 120)

00 MSO

01 Reserved

10 Reserved

11 GP50

Bit 2: Reserved

Bit [1:0]: Reserved

CR2A(GPIO2 ~ 5& Flash ROM Interface Select,
default 0xFF if PENROM# = 0 during POR,
default 0x00 otherwise)

Bit 7: (PIN 86 ~89 & 91 ~94)

0 GPIO 2

1 Flash IF (xD7 ~ XD0)

Bit 6: (PIN 78 ~ 85)

0 GPIO 3

1 Flash IF (XA7 ~ XA0)

Bit 5: (PIN 69 ~ 74 & 76 ~77)

0 GPIO 4

1 Flash IF (XA15 ~ XA10 & XA9 ~ A8)

Bit 4: (PIN 66 ~ 68 & 95 ~ 97)

0 GPIO 5(GP52 ~ 57)

1 Flash IF(XA18 ~ XA16 , ROMCS#, MEMR #, MEMW#)

Bit [3:0]: Reserved

CR2B(PWM & GPIO8, GPIO6 Select)

Default 0x03

Bit [7]: Reserved.

Bit [6:5]: (Pin115)

00 PWM2

01 PLED

10 Reserved

11 GP83

Bit [4]: (Pin116)

0 PWM1

1 GP82

Bit [3]: (Pin117)

0 PWM0

1 GP81

Bit [2]: (Pin118)

0 WDTO

1 GP80

Bit [1]: (Pin99, Pin100, Pin101, Pin102, Pin105, Pin106)

0 Reserved

1 GPIO6(GP67, GP66, GP65, GP64, GP61, GP60)

Bit [0]: (Pin103, Pin104)

0 Reserved

1 GPIO6(GP63, GP62)

CR2C(SC & GPIO7 Select)

Default 0x30

Bit [7:6]: (Pin107, Pin108, Pin109, Pin110, Pin113)

- 00 SC(SCPSNT, SCIO,SCCLK, SCRST, SCPWR)
- 01 Reserved
- 10 Reserved
- 11 GPIO7(GP77, GP76, GP75, GP74, GP71)

Bit [5:4]: (Pin111)

- 00 Reserved
- 01 Reserved
- 10 Reserved
- 11 GP73

Bit [3:2]: (Pin112)

- 00 SCC8
- 01 Reserved
- 10 Reserved
- 11 GP72

Bit [1:0]: (Pin114)

- 00 SCC4
- 01 Reserved
- 10 Reserved
- 11 GP70

3.5 Logical Device 0 (FDC)

CR30 (Default 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit [7:1]: Reserved.

Bit 0:
- 1 Activates the logical device.
- 0 Logical device is inactive.

CR60, CR61 (Default 0x03, 0xf0 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select FDC I/O base address [0x100:0xFF8] on 8 byte boundary.

CR70 (Default 0x06 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resource for FDC.

CR74 (Default 0x02 if PNPCSV = 0 during POR, default 0x04 otherwise)

Bit [7:3]: Reserved.

Bit [2:0]: These bits select DRQ resource for FDC.

= 0x00 DMA0

= 0x01 DMA1

= 0x02 DMA2

= 0x03 DMA3

= 0x04 - 0x07 No DMA active

CRF0 (Default 0x0E)

FDD Mode Register

Bit 7: FIPURDWN

This bit controls the internal pull-up resistors of the FDC input pins RDATA, INDEX, TRAK0, DSKCHG, and WP.

0 The internal pull-up resistors of FDC are turned on.(Default)

1 The internal pull-up resistors of FDC are turned off.

Bit 6: INTVERTZ

This bit determines the polarity of all FDD interface signals.

0 FDD interface signals are active low.

1 FDD interface signals are active high.

Bit 5: DRV2EN (PS2 mode only)

When this bit is a logic 0, indicates a second drive is installed and is reflected in status register A.

Bit 4: Swap Drive 0, 1 Mode

0 No Swap (Default)

1 Drive and Motor select 0 and 1 are swapped.

Bit 3 - 2 Interface Mode

11 AT Mode (Default)

10 (Reserved)

01 PS/2

00 Model 30

Bit 1: FDC DMA Mode

0 Burst Mode is enabled

1 Non-Burst Mode (Default)

Bit 0 Floppy Mode

0 Normal Floppy Mode (Default)

1 Enhanced 3-mode FDD

CRF1 (Default 0x00)

Bit 7 - 6 Boot Floppy

00 FDD A

01 FDD B

10 FDD C

11 FDD D

Bit [5:4]: Media ID1, Media ID0. These bits will be reflected on FDC's Tape Drive Register bit 7, 6.

Bit [3:2]: Density Select

00 Normal (Default)

01 Normal

10 1 (Forced to logic 1)

11 0 (Forced to logic 0)

Bit 1: DISFDDWR

0 Enable FDD write.

1 Disable FDD write(forces pins WE, WD stay high).

Bit 0: SWWP

0 Normal, use WP to determine whether the FDD is write protected or not.

1 FDD is always write-protected.

CRF2 (Default 0xFF)

Bit [7:6]: FDD D Drive Type

Bit [5:4]: FDD C Drive Type

Bit [3:2]: FDD B Drive Type

Bit [1:0]: FDD A Drive Type

CRF4 (Default 0x00)

FDD0 Selection:

Bit 7: Reserved.

Bit 6: Precomp. Disable.

1 Disable FDC Precompensation.

0 Enable FDC Precompensation.

Bit 5: Reserved.

Bit 4 - 3: DRTS1, DRTS0: Data Rate Table select (Refer to TABLE A).

00 Select Regular drives and 2.88 format

01 3-mode drive

10 2 Meg Tape

11 Reserved

Bit 2: Reserved.

Bit [1:0]: DTYPE0, DTYPE1: Drive Type select (Refer to TABLE B).

CRF5 (Default 0x00)

FDD1 Selection: Same as FDD0 of CRF4.

TABLE A

Drive Rate Table Select		Data Rate		Selected Data Rate		SELDEN
DRTS1	DRTS0	DRATE1	DRATE0	MFM	FM	
0	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	300K	150K	0
		1	0	250K	125K	0
0	1	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	500K	250K	0
		1	0	250K	125K	0
1	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	2Meg	---	0
		1	0	250K	125K	0

TABLE B

DTYPE0	DTYPE1	DRVDEN0(pin 2)	DRVDEN1(pin 3)	DRIVE TYPE
0	0	SELDEN	DRATE0	4/2/1 MB 3.5”“ 2/1 MB 5.25” 2/1.6/1 MB 3.5” (3-MODE)
0	1	DRATE1	DRATE0	
1	0	$\overline{\text{SELDEN}}$	DRATE0	
1	1	DRATE0	DRATE1	

3.6 Logical Device 1 (Parallel Port)

CR30 (Default 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit [7:1]: Reserved.

Bit 0: 1 Activates the logical device.

0 Logical device is inactive.

CR60, CR61 (Default 0x03, 0x78 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select Parallel Port I/O base address.

[0x100:0xFFC] on 4 byte boundary (EPP not supported) or

[0x100:0xFF8] on 8 byte boundary (all modes supported, EPP is only available when the base address is on 8 byte boundary).

CR70 (Default 0x07 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resource for Parallel Port.

CR74 (Default 0x03)

Bit [7:3]: Reserved.

Bit [2:0]: These bits select DRQ resource for Parallel Port.

0x00=DMA0

0x01=DMA1

0x02=DMA2

0x03=DMA3

0x04 - 0x07= No DMA active

CRF0 (Default 0x3F)

Bit 7: Reserved.

Bit [6:3]: ECP FIFO Threshold.

Bit [2:0]: Parallel Port Mode (CR28 PRTMODS2 = 0)

100	Printer Mode
000	Standard and Bi-direction (SPP) mode
001	EPP - 1.9 and SPP mode
101	EPP - 1.7 and SPP mode
010	ECP mode
011	ECP and EPP - 1.9 mode
111	ECP and EPP - 1.7 mode (Default)

3.7 Logical Device 2 (UART A)

CR30 (Default 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit [7:1]: Reserved.

Bit 0: 1 Activates the logical device.

0 Logical device is inactive.

CR60, CR61 (Default 0x03, 0xF8 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select Serial Port 1 I/O base address [0x100:0xFF8] on 8 byte boundary.

CR70 (Default 0x04 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resource for Serial Port 1.

CRF0 (Default 0x00)

Bit 7: Reserved.

Bit 6: 1 Activates the logical device IRQ sharing function.

0 Logical device IRQ sharing is inactive.

Bit [5:2]: Reserved.

Bit [1:0]: SUACLKB1, SUACLKB0

00 UART A clock source is 1.8462 Mhz (24MHz/13)

01 UART A clock source is 2 Mhz (24MHz/12)

10 UART A clock source is 24 Mhz (24MHz/1)

11 UART A clock source is 14.769 Mhz (24mhz/1.625)

3.8 Logical Device 3 (UART B)

CR30 (Default 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit [7:1]: Reserved.

Bit 0: 1 Activates the logical device.

0 Logical device is inactive.

CR60, CR61 (Default 0x02, 0xF8 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select Serial Port 2 I/O base address [0x100:0xFF8] on 8 byte boundary.

CR70 (Default 0x03 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resource for Serial Port 2.

CRF0 (Default 0x00)

Bit 7: Reserved.

Bit 6: 1 Activates the logical device IRQ sharing function.

0 Logical device IRQ sharing is inactive.

Bit [5:4]: Reserved.

Bit 3: RXW4C

0 No reception delay when SIR is changed from TX mode to RX mode.

1 Reception delays 4 characters-time (40 bit-time) when SIR is changed from TX mode to RX mode.

Bit 2: TXW4C

0 No transmission delay when SIR is changed from RX mode to TX mode.

1 Transmission delays 4 characters-time (40 bit-time) when SIR is changed from RX mode to TX mode.

Bit [1:0]: SUBCLKB1, SUBCLKB0

00 UART B clock source is 1.8462 Mhz (24MHz/13)

01 UART B clock source is 2 Mhz (24MHz/12)

10 UART B clock source is 24 Mhz (24MHz/1)

11 UART B clock source is 14.769 Mhz (24mhz/1.625)

CRF1 (Default 0x00)

Bit 7: Reserved.

Bit 6: IRLOCSEL. IR I/O pins' location select.

0 Through SINB/SOUTB.

1 Through IRRX/IRTX.

Bit 5: IRMODE2. IR function mode selection bit 2.

Bit 4: IRMODE1. IR function mode selection bit 1.

Bit 3: IRMODE0. IR function mode selection bit 0.

IR MODE	IR FUNCTION	IRTX	IRRX
00X	Disable	tri-state	high
010*	IrDA	Active pulse 1.6 µS	Demodulation into SINB/IRRX
011*	IrDA	Active pulse 3/16 bit time	Demodulation into SINB/IRRX
100	ASK-IR	Inverting IRTX/SOUTB pin	routed to SINB/IRRX
101	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	routed to SINB/IRRX
110	ASK-IR	Inverting IRTX/SOUTB	Demodulation into SINB/IRRX
111*	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	Demodulation into SINB/IRRX

Note: The notation is normal mode in the IR function.

Bit 2: HDUPLX. IR half/full duplex function select.
- 0 The IR function is Full Duplex.
- 1 The IR function is Half Duplex.

Bit 1: TX2INV.
- 0 the SOUTB pin of UART B function or IRTX pin of IR function in normal condition.
- 1 inverse the SOUTB pin of UART B function or IRTX pin of IR function.

Bit 0: RX2INV.
- 0 the SINB pin of UART B function or IRRX pin of IR function in normal condition.
- 1 inverse the SINB pin of UART B function or IRRX pin of IR function

3.9 Logical Device 7 (Game Port and GPIO Port 1)

CR30 (Default 0x00)

Bit [7:1]: Reserved.

Bit 0:
- 1 Game/GP1 Port is active.
- 0 Game/GP1 Port is inactive.

CR60, CR61 (Default 0x02, 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)

These two registers select the Game Port base address [0x100:0xFFF] on 8 byte boundary.

CR62, CR63 (Default 0x00, 0x00)

These two registers select the GPIO1 base address [0x100:0xFFF] on 1 byte boundary

IO address : CRF1 base address

CRF0 (GP10-GP17 I/O selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CRF1 (GP10-GP17 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written

If a port is programmed to be an input port, then its respective bit can only be read.

CRF2 (GP10-GP17 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

3.10 Logical Device 8 (MIDI Port and GPIO Port 5)

CR30 (MIDI Port Default 0x00)

Bit [7:1]: Reserved.

Bit 0: 1 MIDI/GP5 port is activate

0 MIDI/GP5 port is inactive.

CR60, CR61 (Default 0x03, 0x30 if PNPCSV = 0 during POR, default 0x00 otherwise)

These two registers select the MIDI Port base address [0x100:0xFFF] on 2byte boundary.

CR62, CR63 (Default 0x00, 0x00)

These two registers select the GPIO5 base address [0x100:0xFFF] on 4byte boundary.

IO address : CRF1 base address

IO address + 1 : CRF3 base address

IO address + 2 : CRF4 base address

IO address + 3 : CRF5 base address

CR70 (Default 0x09 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resource for MIDI Port .

CRF0 (GP5 selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CRF1 (GP5 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written.

If a port is programmed to be an input port, then its respective bit can only be read.

CRF2 (GP5 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

CRF3 (PLED mode register. Default 0x00)

Bit [7:3] Reserved .
:

Bit 2: select WDTO count mode.

0 second

1 minute

Bit [1:0]: select PLED mode

00 Power LED pin is tri-stated.

01 Power LED pin is droved low.

10 Power LED pin is a 1Hz toggle pulse with 50 duty cycle.

11 Power LED pin is a 1/4Hz toggle pulse with 50 duty cycle.

CRF4 (Default 0x00)

Watch Dog Timer Time-out value. Writing a non-zero value to this register causes the counter to load the value to Watch Dog Counter and start counting down. Reading this register returns current value in Watch Dog Counter instead of Watch Dog Timer Time-out value.

Bit [7:0]: = 0x00 Time-out Disable

= 0x01 Time-out occurs after 1 second/minute

= 0x02 Time-out occurs after 2 second/minutes

= 0x03 Time-out occurs after 3 second/minutes

.....

= 0xFF Time-out occurs after 255 second/minutes

CRF5 (Default 0x00)

Bit [7] : Reserved .

Bit [6] : invert Watch Dog Timer Status

Bit 5: Force Watch Dog Timer Time-out, Write only*

1 Force Watch Dog Timer time-out event; this bit is self-clearing.

Bit 4: Watch Dog Timer Status, R/W

1 Watch Dog Timer time-out occurred.

0 Watch Dog Timer counting

Bit [3:0]: These bits select IRQ resource for Watch Dog. Setting of 2 selects SMI.

3.11 Logical Device 9 (GPIO Port 2 ~ GPIO Port 4)

CR30 (Default 0x00)

Bit [7:3]: Reserved.

Bit 2: 1 GP4 port is active.
0 GP4 port is inactive

Bit 1: 1 GP3 port is active.
0 GP3 port is inactive

Bit 0: 1 GP2 port is active.
0 GP2 port is inactive.

CR60,CR61(Default 0x00,0x00).

These two registers select the GP2,3,4 base address(0x100:FFF) ON 3 bytes boundary.

IO address: CRF1 base address

IO address + 1 : CRF4 base address

IO address + 2 : CRF7 base address

CRF0 (GP2 I/O selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CRF1 (GP2 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written.

If a port is programmed to be an input port, then its respective bit can only be read.

CRF2 (GP2 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

CRF3 (GP3 I/O selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CRF4 (GP3 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written.

If a port is programmed to be an input port, then its respective bit can only be read.

CRF5 (GP3 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

CRF6 (GP4 I/O selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CRF7 (GP4 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written.

If a port is programmed to be an input port, then its respective bit can only be read.

CRF8 (GP4 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

3.12 Logical Device A (ACPI)

CR30 (Default 0x00)

Bit [7:1]: Reserved.

Bit 0: 1 Activates the logical device.

0 Logical device is inactive.

CR70 (Default 0x00)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resources for $\overline{SMI}$ / $\overline{PME}$

CRF0 (Default 0x00)

Bit 7: CHIPPME. Chip level auto power management enable.

0 disable the auto power management functions

1 enable the auto power management functions.

Bit 6: Reserved. (Return zero when read)

Bit 5: MIDIPME. MIDI port auto power management enable.

0 disable the auto power management functions

1 enable the auto power management functions

Bit 4: Reserved. (Return zero when read)

Bit 3: PRTPME. PRT auto power management enable.

0 disable the auto power management functions.

1 enable the auto power management functions.

Bit 2: FDCPME. FDC auto power management enable.

0 disable the auto power management functions.

1 enable the auto power management functions.

Bit 1: URAPME. UART A auto power management enable.

0 disable the auto power management functions.

1 enable the auto power management functions.

Bit 0: URBPME. UART B auto power management enable.

0 disable the auto power management functions.

1 enable the auto power management functions.

CRF1 (Default 0x00)

Bit 7: WAK_STS. This bit is set when the chip is in the sleeping state and an enabled resume event occurs. Upon setting this bit, the sleeping/working state machine will transition the system to the working state. This bit is only set by hardware and is cleared by writing a 1 to this bit position or by the sleeping/working state machine automatically when the global standby timer expires.

0 the chip is in the sleeping state.

1 the chip is in the working state.

Bit 6: Reserved. (Return zero when read)

Bit 5: MIDI's trap status.

Bit 4: Reserved. (Return zero when read)

Bit 3: PRT's trap status.

Bit 2: FDC's trap status.

Bit 1: URA's trap status.

Bit 0: URB's trap status.

CRF2 (Default 0x00)

Bit [7:3]: Reserved. (Return zero when read)

Bit 2: SC's trap status.

Bit 1: Reserved

Bit 0: Reserved

CRF3 (Default 0x00)

These bits indicate the IRQ status of the individual device respectively. The device's IRQ status bit is set by their source device and is cleared by writing a 1. Writing a 0 has no effect.

Bit 7: Reserved

Bit 6: Reserved

Bit [5:4]: Reserved. (Return zero when read)

Bit 3: PRTIRQSTS. PRT IRQ status.

Bit 2: FDCIRQSTS. FDC IRQ status.

Bit 1: URAIRQSTS. UART A IRQ status.

Bit 0: URBIRQSTS. UART B IRQ status.

CRF4 (Default 0x00)

These bits indicate the IRQ status of the individual GPIO function or logical device respectively. The status bit is set by their source function or device and is cleared by writing a 1. Writing a 0 has no effect.

Bit 7: Reserved. (Return zero when read)

Bit 6: SCIRQSTS. SC IRQ status.

Bit [5:3]: Reserved. (Return zero when read)

Bit 2: WDTIRQSTS. Watch dog timer IRQ status.

Bit 1: Reserved. (Return zero when read).

Bit 0: MIDIIRQSTS. MIDI IRQ status.

CRF6 (Default 0x00)

These bits enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to any IRQ of the devices.

$\overline{SMI}/\overline{PME}$ logic output = (PRTIRQEN and PRTIRQSTS) or (FDCIRQEN and FDCIRQSTS)
or (URAIRQEN and URAIRQSTS) or (URBIRQEN and URBIRQSTS)
or (WDTIRQEN and WDTIRQSTS) or (MIDIIRQEN and MIDIIRQEN)
or (SCIRQEN and SCIRQEN)

Bit 7: Reserved

0 disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to URD's IRQ.

1 enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to URD's IRQ.

Bit 6: Reserved

0 disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to URC's IRQ.

1 enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to URC's IRQ.

Bit [5:4]: Reserved (Return zero when read)

Bit 3: PRTIRQEN.

0 disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to PRT's IRQ.

1 enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to PRT's IRQ.

Bit 2: FDCIRQEN.

0 disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to FDC's IRQ.

1 enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to FDC's IRQ.

Bit 1: URAIRQEN.

0 disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to UART A's IRQ.

1 enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to UART A's IRQ.

Bit 0: URBIRQEN.

0 disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to UART B's IRQ.

1 enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to UART B's IRQ.

CRF7 (Default 0x00)

These bits enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to any IRQ of the devices.

Bit 7: Reserved. (Return zero when read)

Bit 6: SCIRQEN.

0 disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to SC timer's IRQ.

1 enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to SC timer's IRQ.

Bit [5:3]: Reserved. (Return zero when read)

Bit 2: WDTIRQEN.

0 disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to watch dog timer's IRQ.

1 enable the generation of an $\overline{SMI}/\overline{SMI}$ interrupt due to watch dog timer's IRQ.

Bit 1: Reserved. (Return zero when read)

Bit 0: MIDIIRQEN.

0 disable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to MIDI's IRQ.

1 enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to MIDI's IRQ.

CRF9 (Default 0x00)

Bit [7:3]: Reserved. Return zero when read.

Bit 2: PME_EN: Select the power management events to be either an $\overline{PME}$ or $\overline{SMI}$ interrupt for the IRQ events. Note that: this bit is valid only when SMIPME_OE = 1.

0 the power management events will generate an $\overline{SMI}$ event.

1 the power management events will generate an $\overline{PME}$ event.

Bit 1: FSLEEP: This bit selects the fast expiry time of individual devices.

0 1 S

1 8 mS

Bit 0: SMIPME_OE: This is the $\overline{SMI}$ and $\overline{PME}$ output enable bit.

0 neither $\overline{SMI}$ nor $\overline{PME}$ will be generated. Only the IRQ status bit is set.

1 an $\overline{SMI}$ or $\overline{PME}$ event will be generated.

CRFA (Default 0x00)

Bit [7:3]: Reserved. (Return zero when read)

Bit 2: SCPME. SC auto power management enable.

0 disable the auto power management functions.

1 enable the auto power management functions.

Bit 1: Reserved

Bit 0: Reserved

3.13 Logical Device B (PWM)

CR30 (Default 0x00)

Bit [7:1]: Reserved.

Bit 0: 1 Activates the logical device.

0 Logical device is inactive.

CR60, CR61 (Default 0x00, 0x00)

These two registers select Pulse Width Modulation base address [0x100:0xFFF] on 8-byte boundary.

3.14 Logical Device C (SMART CARD)

CR30 (Default 0x00)

Bit [7:1]: Reserved.

Bit 0: 1 Activates the logical device.

0 Logical device is inactive.

CR60, CR61 (Default 0x00, 0x00)

These two registers select Smart Card base address [0x100:0xFFF] on 8-byte boundary.

CR70 (Default 0x00)

Bit [7:4]: Reserved.

Bit [3:0]: These bit select IRQ resource for Smart Card interface.

CRF0 (Default 0x00)

Bit [7:1]: Reserved.

Bit 0: 1 Smart Card present signal (SCPSNT) is LOW active.

0 SCPSNT is HIGH active.

3.15 Logical Device D (GPIO Port 6)

CR30 (Default 0x00)

Bit [7:2]: Reserved.

Bit 1: 1 Activate GPIO6.

0 GPIO6 is inactive

Bit 0: Reserved

CR60, CR61 (Default 0x03, 0xE8 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select the Serial Port 3 I/O base address [0x100:0xFF8] on 8yte boundary.

CR62, CR63 (Default 0x00)

These two registers select the GPIO6 base address [0x100:0xFFF] on 4byte boundary.

IO address: CRF2 base address

CR70 (Default 0x00)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resource for Serial Port 3.

CRF0 (Default 0x00)

Bit 7: Reserved.

Bit 6: 1 Activates the logical device IRQ sharing function.

0 Logical device IRQ sharing is inactive.

Bit [5:2]: Reserved.

Bit [1:0]: SUCCLKB1, SUCCLKB0

00 UART C clock source is 1.8462 Mhz (24MHz/13)

01 UART C clock source is 2 Mhz (24MHz/12)

10 UART C clock source is 24 Mhz (24MHz/1)

11 UART C clock source is 14.769 Mhz (24mhz/1.625)

CRF1 (GP6 selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CRF2 (GP6 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written.

If a port is programmed to be an input port, then its respective bit can only be read.

CRF3 (GP6 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

CRF4 (GP6 output style register. Default 0x00)

When set to a '1', the outgoing port is pulse mode.

When set to a '0', the outgoing port is level mode.

3.16 Logical Device E (GPIO Port 7)

CR30 (Default 0x00)

Bit [7:2]: Reserved.

Bit 1: 1 Activate GPIO7.

0 GPIO7 is inactive

Bit 0: Reserved

CR60, CR61 (Default 0x02, 0xE8 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select the Serial Port 4 I/O base address [0x100:0xFF8] on 8yte boundary.

CR62, CR63 (Default 0x00)

These two registers select the GPIO7 base address [0x100:0xFFF] on 4byte boundary.

IO address : CRF2 base address

CR70(Default 0x00)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resource for Serial Port 4.

CRF0 (Default 0x00)

Bit 7: Reserved.

Bit 6: 1 Activates the logical device IRQ sharing function.

0 Logical device IRQ sharing is inactive.

Bit [5:2]: Reserved.

Bit [1:0]: SUDCLKB1, SUDCLKB0

00 UART D clock source is 1.8462 Mhz (24MHz/13)

01 UART D clock source is 2 Mhz (24MHz/12)

10 UART D clock source is 24 Mhz (24MHz/1)

11 UART D clock source is 14.769 Mhz (24mhz/1.625)

CRF1 (GP7 selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CRF2 (GP7 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written.

If a port is programmed to be an input port, then its respective bit can only be read.

CRF3 (GP7 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

3.17 Logical Device F (GPIO Port 8)

CR30 (Default 0x00)

Bit [7:1]: Reserved.

Bit 0: 1 Activate GPIO8.

0 PIO8 is inactive.

CR60, CR61 (Default 0x00)

These two registers select the GPIO8 base address [0x100:0xFFF] on 2byte boundary.

IO address : CRF1 base address

CRF0 (GP8 selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CRF1 (GP8 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written.

If a port is programmed to be an input port, then its respective bit can only be read.

CRF2 (GP8 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

4. SPECIFICATIONS

4.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage (5V)	-0.5 to 7.0	V
Input Voltage	-0.5 to V_{DD}+0.5	V
RTC Battery Voltage V_{BAT}	2.2 to 4.0	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to +150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

4.2 DC CHARACTERISTICS

(Ta = 0° C to 70° C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
RTC Battery Quiescent Current	I_{BAT}			2.4	uA	V_{BAT} = 2.5 V
ACPI Stand-by Power Supply Quiescent Current	I_{BAT}			2.0	mA	V_{SB} = 5.0 V, All ACPI pins are not connected.
I/O_{8t} - TTL level bi-directional pin with 8mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = - 8 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{12t} - TTL level bi-directional pin with 12mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V

4.2 DC CHARACTERISTICS, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{24t} - TTL level bi-directional pin with 24mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{12tp3} – 3.3V TTL level bi-directional pin with 12mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{12ts} - TTL level Schmitt-trigger bi-directional pin with 12mA source-sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{DD}=5V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{24ts} - TTL level Schmitt-trigger bi-directional pin with 24mA source-sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{DD}=5V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 Ma

4.2 DC CHARACTERISTICS, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{24tsp3} – 3.3V TTL level Schmitt-trigger bi-directional pin with 24mA source-sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{DD}=3.3V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/OD_{12t} - TTL level bi-directional pin and open-drain output with 12mA sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/OD_{24t} - TTL level bi-directional pin and open-drain output with 24mA sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
$I/OD24_{c}$ - CMOS level bi-directional pin and open drain output with 24mA sink capability						
Input Low Voltage	V_{IL}			1.5	V	
Input High Voltage	V_{IH}	3.5			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V

4.2 DC CHARACTERISTICS, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/OD_{24a} - Bi-directional pin with analog input and open-drain output with 24mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/OD_{12ts} - TTL level Schmitt-trigger bi-directional pin and open drain output with 12mA sink capability						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{DD}=5V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/OD_{24ts} - TTL level Schmitt-trigger bi-directional pin and open drain output with 24mA sink capability						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{DD}=5V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
$I/OD12_{cs}$ - CMOS level Schmitt-trigger bi-directional pin and open drain output with 12mA sink capability						
Input Low Threshold Voltage	Vt-	1.3	1.5	1.7	V	V_{DD} = 5 V
Input High Threshold Voltage	Vt+	3.2	3.5	3.8	V	V_{DD} = 5 V
Hystersis	V_{TH}	1.5	2		V	V_{DD} = 5 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V

4.2 DC CHARACTERISTICS, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/OD16$_{cs}$ - CMOS level Schmitt-trigger bi-directional pin and open drain output with 16mA sink capability						
Input Low Threshold Voltage	V_{t-}	1.3	1.5	1.7	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	3.2	3.5	3.8	V	V_{DD} = 5 V
Hystersis	V_{TH}	1.5	2		V	V_{DD} = 5 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 16 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
I/OD24$_{cs}$ - CMOS level Schmitt-trigger bi-directional pin and open drain output with 24mA sink capability						
Input Low Threshold Voltage	V_{t-}	1.3	1.5	1.7	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	3.2	3.5	3.8	V	V_{DD} = 5 V
Hystersis	V_{TH}	1.5	2		V	V_{DD} = 5 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
I/OD12$_{csd}$ - CMOS level Schmitt-trigger bi-directional pin with internal pull down resistor and open drain output with 12mA sink capability						
Input Low Threshold Voltage	V_{t-}	1.3	1.5	1.7	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	3.2	3.5	3.8	V	V_{DD} = 5 V
Hystersis	V_{TH}	1.5	2		V	V_{DD} = 5 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
I/OD12$_{csu}$ - CMOS level Schmitt-trigger bi-directional pin with internal pull up resistor and open drain output with 12mA sink capability						
Input Low Threshold Voltage	V_{t-}	1.3	1.5	1.7	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	3.2	3.5	3.8	V	V_{DD} = 5 V
Hystersis	V_{TH}	1.5	2		V	V_{DD} = 5 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA

Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V

4.2 DC CHARACTERISTICS, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
O_4 - Output pin with 4mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -4 mA
O_8 - Output pin with 8mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -8 mA
O_{12} - Output pin with 12mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
O_{16} - Output pin with 16mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 16 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -16 mA
O_{24} - Output pin with 24mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
O_{12p3} - 3.3V output pin with 12mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
O_{24p3} - 3.3V output pin with 24mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
OD_{12} - Open drain output pin with 12mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
OD_{24} - Open drain output pin with 24mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
OD_{12p3} - 3.3V open drain output pin with 12mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
IN_t - TTL level input pin						
Input Low Voltage	V_{IL}			0.8	V	

3.2 DC CHARACTERISTICS, continued

4.2 DC CHARACTERISTICS, continued

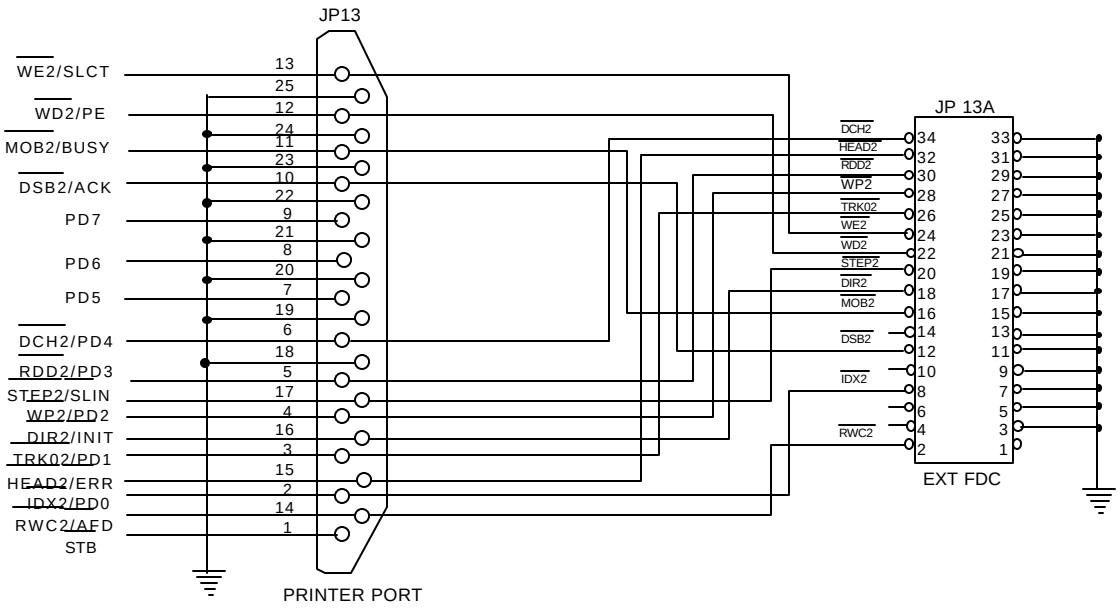
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{tp3} - 3.3V TTL level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{td} - TTL level input pin with internal pull down resistor						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{tu} - TTL level input pin with internal pull up resistor						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{ts} - TTL level Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	0.8	0.9	1.0	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	1.8	1.9	2.0	V	V_{DD} = 5 V
Hystersis	V_{TH}	0.8	1.0		V	V_{DD} = 5 V
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{tsp3} - 3.3 V TTL level Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	0.8	0.9	1.0	V	V_{DD} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.8	1.9	2.0	V	V_{DD} = 3.3 V
Hystersis	V_{TH}	0.8	1.0		V	V_{DD} = 3.3 V
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V

4.2 DC CHARACTERISTICS, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
IN_c - CMOS level input pin						
Input Low Voltage	V_{IL}			1.5	V	
Input High Voltage	V_{IH}	3.5			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{cu} - CMOS level input pin with internal pull up resistor						
Input Low Voltage	V_{IL}			1.5	V	
Input High Voltage	V_{IH}	3.5			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{cd} - CMOS level input pin with internal pull down resistor						
Input Low Voltage	V_{IL}			1.5	V	
Input High Voltage	V_{IH}	3.5			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{cs} - CMOS level Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	1.3	1.5	1.7	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	3.2	3.5	3.8	V	V_{DD} = 5 V
Hystersis	V_{TH}	1.5	2		V	V_{DD} = 5 V
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{csu} - CMOS level Schmitt-trigger input pin with internal pull up resistor						
Input Low Threshold Voltage	V_{t-}	1.3	1.5	1.7	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	3.2	3.5	3.8	V	V_{DD} = 5 V
Hystersis	V_{TH}	1.5	2		V	V_{DD} = 5 V
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V

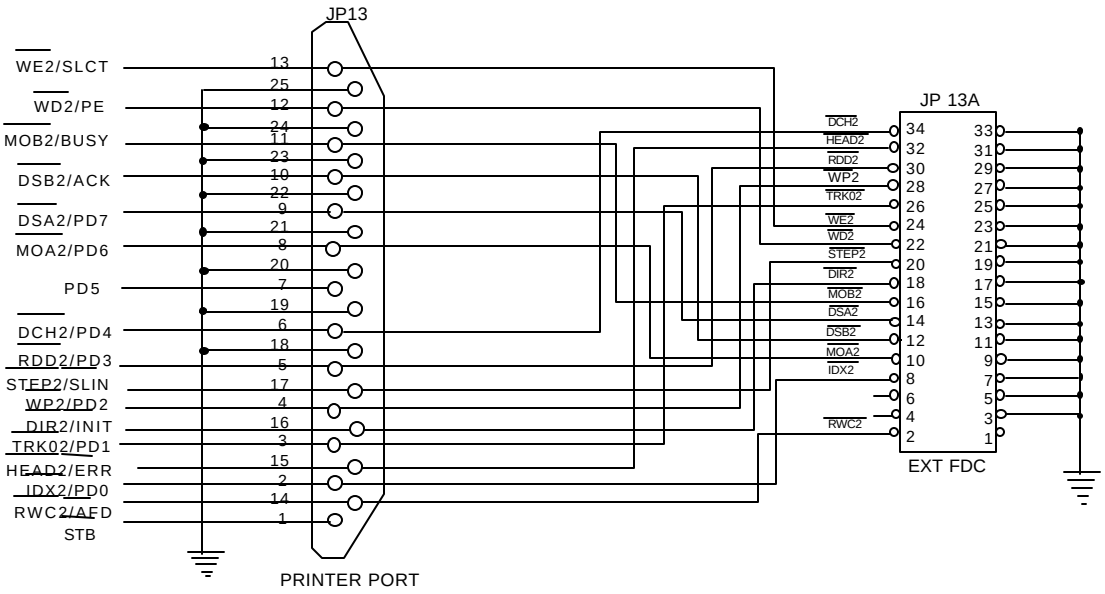
5. APPLICATION CIRCUITS

5.1 Parallel Port Extension FDD



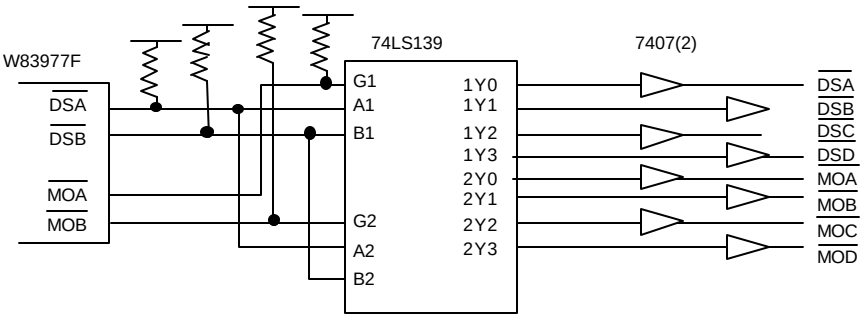
Parallel Port Extension FDD Mode Connection Diagran

5.2 Parallel Port Extension 2FDD



Parallel Port Extension 2FDD Connection Diagran

5.3 Four FDD Mode



6. ORDERING INSTRUCTION

PART NO.	PACKAGE	REMARKS
W83697SF	128-pin QFP	

7. HOW TO READ THE TOP MARKING

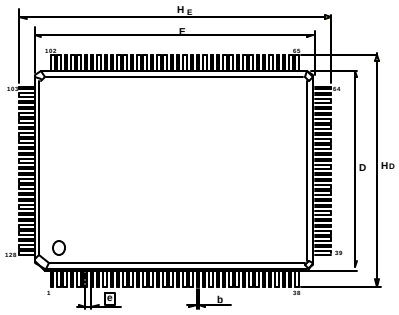
Example: The top marking of W83697SF

1st line: Winbond logo & SMART@IO
2nd line: the type number: W83697SF
3th line: the tracking code 109 G 5B B BA

109: packages made in 2001, week 09
G: assembly house ID; A means ASE, S means SPIL, G means GR, etc.
5B: Winbond internal use.
B: IC revision; A means version A, B means version B
BA: Winbond internal use.

8. PACKAGE DIMENSIONS

(128-pin PQFP)



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A_1	0.25	0.35	0.45	0.010	0.014	0.018
A_2	2.57	2.72	2.87	0.101	0.107	0.113
b	0.10	0.20	0.30	0.004	0.008	0.012
c	0.10	0.15	0.20	0.004	0.006	0.008
D	13.90	14.00	14.10	0.547	0.551	0.555
E	19.90	20.00	20.10	0.783	0.787	0.791
e	—	0.50	—	—	0.020	—
H_D	17.00	17.20	17.40	0.669	0.677	0.685
H_E	23.00	23.20	23.40	0.905	0.913	0.921
L	0.65	0.80	0.95	0.025	0.031	0.037
L_1	—	1.60	—	—	0.063	—
y	—	—	0.08	—	—	0.003
θ	0	—	7	0	—	7

Note:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion .
3. Controlling dimension : Millimeter
4. General appearance spec. should be based on final visual inspection spec.
5. PCB layout please use the "mm".

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San Jose, CA 95134 U.S.A.
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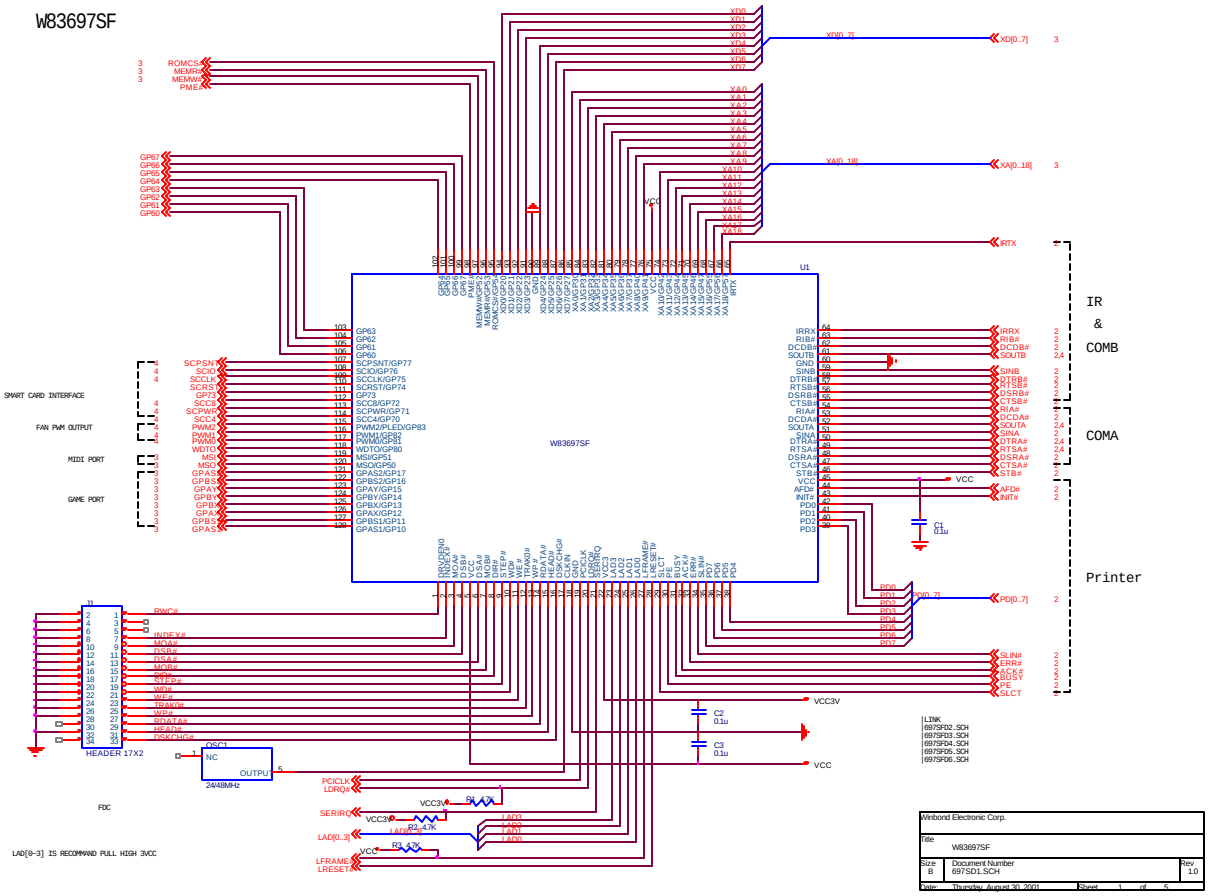
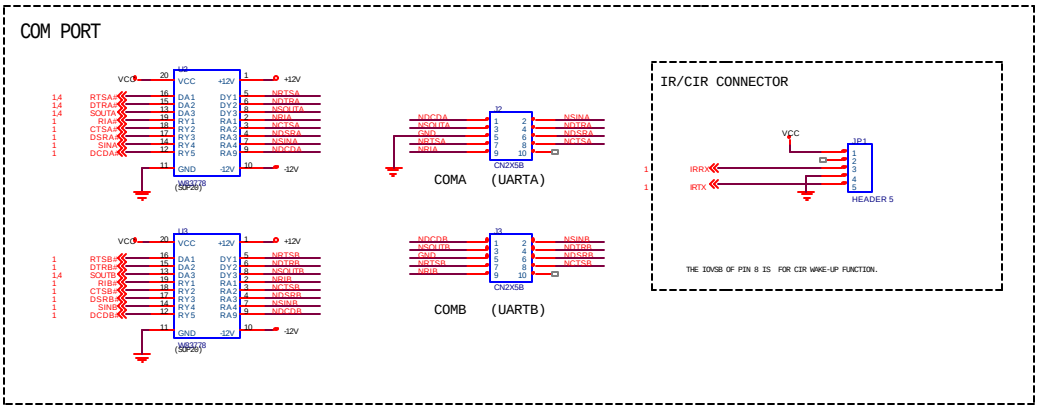
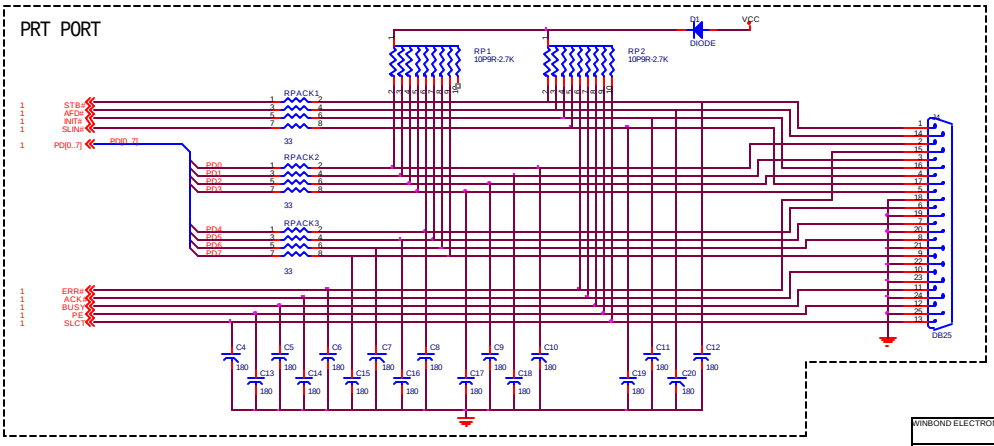
FAX: 1-408-9436668

APPENDIX A : DEMO CIRCUIT







WINBOND ELECTRONICS CORP.		
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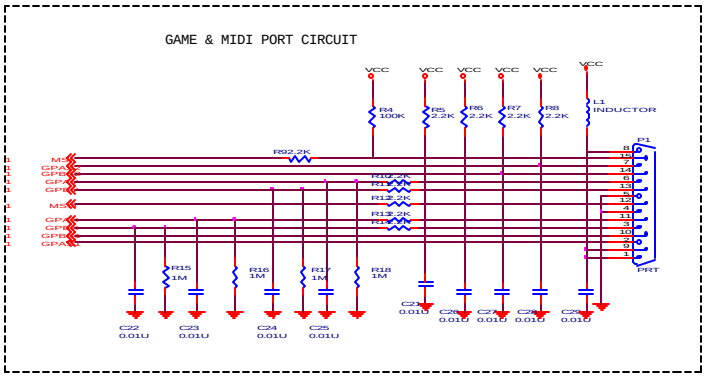
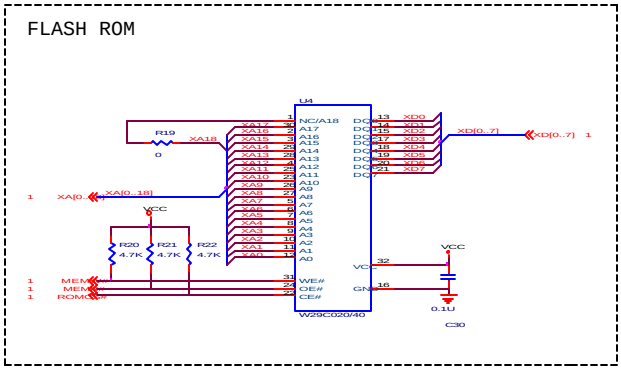
Size: B	Document Number: 697SD2.SCH	Rev: 1.0
Date: Thursday, August 30, 2001	Sheet 2 of 5	





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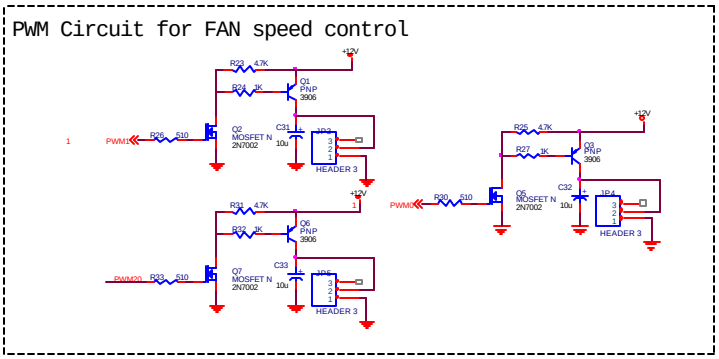
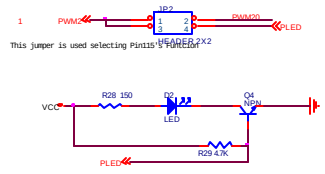
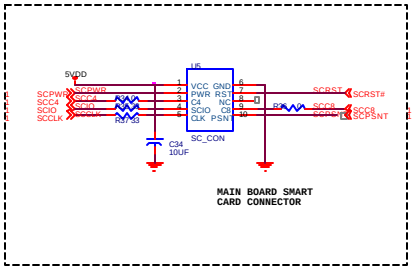
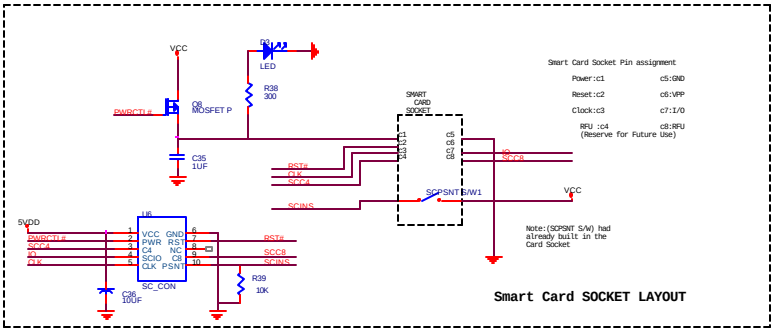
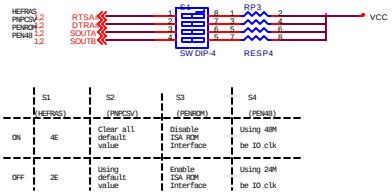
Size: B	Document Number: 697SD3.SCH	Rev: 1.0
Date: Thursday, August 30, 2001	Sheet 3 of 5	











	S1 (HEFRAS)	S2 (PNPCSV)	S3 (PENROM)	S4 (PENAB)
ON	4E	Clear all default value	Disable ISA ROM Interface	Using 48M be IO clk
OFF	2E	Using default value	Enable ISA ROM Interface	Using 24M be IO clk

Winbond Electronic Corp.			
Title: W83697SF			
Size: B	Document Number: 697SD4.SCH		Rev: 1.0
Date: Thursday, August 30, 2001		Sheet 4 of 5	

697SF DEMO CIRCUIT VERSION CHANG NOTICE

1. 30/8/2001 DEMO CIRCUIT VERSION 1.0 RELEASE

WINBOND ELECTRONICS CORP.		
Title: W83697SF		
Size: B	Document Number: 697SD5.SCH	Rev: 0.2
Date: Thursday, August 30, 2001	Sheet 5 of 5	