Spread Aware™, Zero Delay Buffer

Features

- **Spread Aware™—designed to work with SSFTG reference signals**
- **Two banks of four outputs, plus the fed back output**
- **Outputs may be three-stated**
- **Available in 16-pin SOIC or SSOP package**
- **Extra strength output drive available (-19 version)**
- **Internal feedback**

Key Specifications

Operating Voltage: ..... 3.3V±10%

Operating Range: .....15 < f_{OUT} < 133 MHz

Cycle-to-Cycle Jitter: ..... 250 ps

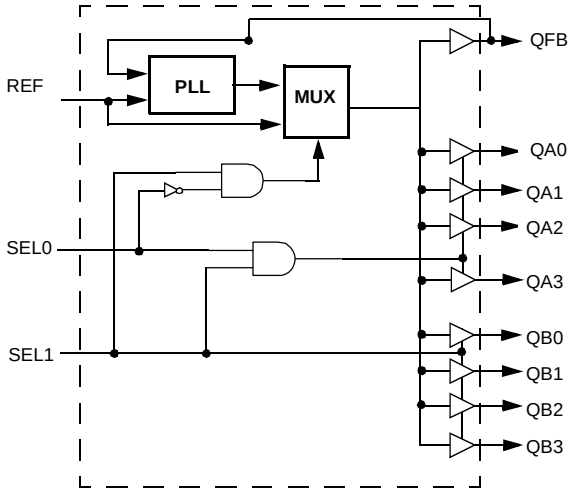
Output to Output Skew: ..... 150 ps

Propagation Delay: ..... 150 ps

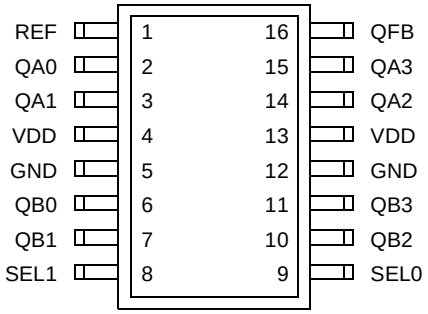
Table 1. Input Logic

SEL1	SEL0	QA0:3	QB0:3	PLL	QFB
0	0	Three-State	Three-State	Shutdown	Active
0	1	Active	Three-State	Active, Utilized	Active
1	0	Active	Active	Shutdown, Bypassed	Active
1	1	Active	Active	Active, Utilized	Active

Block Diagram



Pin Configuration



Spread Aware is a trademark of Cypress Semiconductor Corporation.

Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
REF	1	I	***Reference Input:*** The output signals QA0:3 through QB0:3 will be synchronized to this signal unless the device is programmed to bypass the PLL.
QFB	16	O	***Feedback Output:*** This signal is used as the feedback internally to establish the propagation delay of nearly 0.
QA0:3	2, 3, 14, 15	O	***Outputs from Bank A:*** The frequency of the signals provided by these pins is equal to the signal connected to REF.
QB0:3	6, 7, 10, 11	O	***Outputs from Bank B:*** The frequency of the signals provided by these pins is equal to the signal connected to REF.
VDD	4, 13	P	***Power Connections:*** Connect to 3.3V. Use ferrite beads to help reduce noise for optimal jitter performance.
GND	5, 12	P	***Ground Connections:*** Connect all grounds to the common system ground plane.
SEL0:1	9, 8	I	***Function Select Inputs:*** Tie to V_{DD} (HIGH, 1) or GND (LOW, 0) as desired per *Table 1*.

Overview

The W162 products are nine-output zero delay buffers. A Phase-Locked Loop (PLL) is used to take a time-varying signal and provide eight copies of that same signal out.

Internal feedback is used to maximize the number of output signals provided in the 16-pin package.

Spread Aware

Many systems being designed now utilize a technology called Spread Spectrum Frequency Timing Generation. Cypress has been one of the pioneers of SSFTG development, and we designed this product so as not to filter off the Spread Spectrum feature of the Reference input, assuming it exists. When a zero delay buffer is not designed to pass the SS feature through, the result is a significant amount of tracking skew which may cause problems in systems requiring synchronization.

For more details on Spread Spectrum timing technology, please see the Cypress Application note titled, “EMI Suppression Techniques with Spread Spectrum Frequency Timing Generator (SSFTG) ICs.”

Functional Description

Logic inputs provide the user the ability to turn off one or both banks of clocks when not in use, as described in *Table 1*. Disabling a bank of unused outputs will reduce jitter and power consumption, and will also reduce the amount of EMI generated by the W162.

These same inputs allow the user to bypass the PLL entirely if so desired. When this is done, the device no longer acts as a zero delay buffer, it simply reverts to a standard nine-output clock driver.

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +70	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
P_D	Power Dissipation	0.5	W

DC Electrical Characteristics: T_A =0°C to 70°C, V_{DD} = 3.3V ±10%

Parameter	Description	Test Condition	Min	Typ	Max	Unit
I_{DD}	Supply Current	Unloaded, 100 MHz			40	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA (-19) I_{OL} = 8 mA (-9)			0.4	V
V_{OH}	Output High Voltage	I_{OL} = 12 mA (-19) I_{OL} = 8 mA (-9)	2.4			V
I_{IL}	Input Low Current	V_{IN} = 0V	–500			µA
I_{IH}	Input High Current	V_{IN} = V_{DD}			10	µA

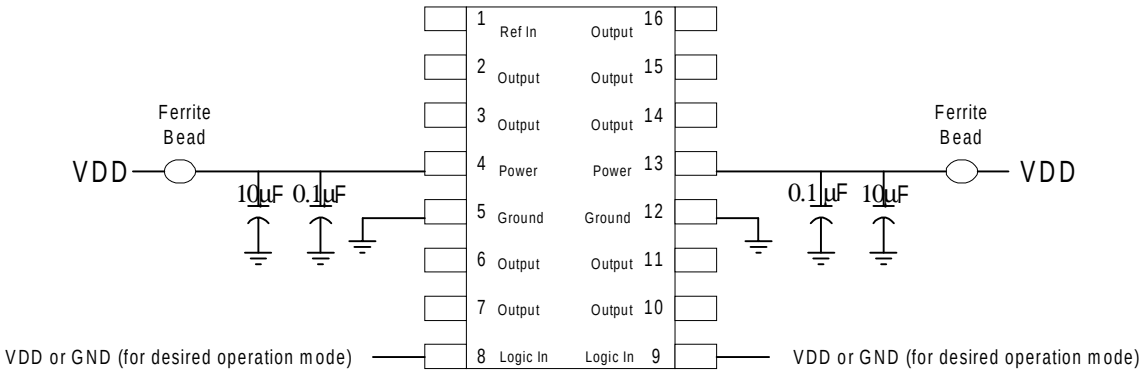
AC Electrical Characteristics: T_A = 0°C to +70°C, V_{DD} = 3.3V ±10%

Parameter	Description	Test Condition	Min	Typ	Max	Unit
f_{IN}	Input Frequency		15		133	MHz
f_{OUT}	Output Frequency	15-pF load[5]	15		133	MHz
t_R	Output Rise Time (-09)[1]	2.0 to 0.8V, 15-pF load		2	2.5	ns
	Output Rise Time (-19)[1]	2.0 to 0.8V, 20-pF load			1.5	ns
t_F	Output Fall Time (-09)[1]	2.0 to 0.8V, 15-pF load		2	2.5	ns
	Output Rise Time (-19)[1]	2.0 to 0.8V, 20-pF load			1.5	ns
t_{PD}	FBIN to REF Skew[2, 3]	Measured at V_{DD}/2			150	ps
t_{SK}	Output to Output Skew	All outputs loaded equally			150	ps
t_D	Duty Cycle	15-pF load[4]	45	50	55	%
t_{LOCK}	PLL Lock Time	Power supply stable			1.0	ms
t_{JC}	Jitter, Cycle-to-Cycle				250	ps

Notes:

1. Long input rise and fall time will degrade skew and jitter performance.
2. All AC specifications are measured with a 50Ω transmission line, load terminated with 50Ω to 1.4V.
3. Skew is measured at V_{DD}/2 on rising edges.
4. Duty cycle is measured at V_{DD}/2
5. For the higher drive -19, the load is 20 pF.

Schematic



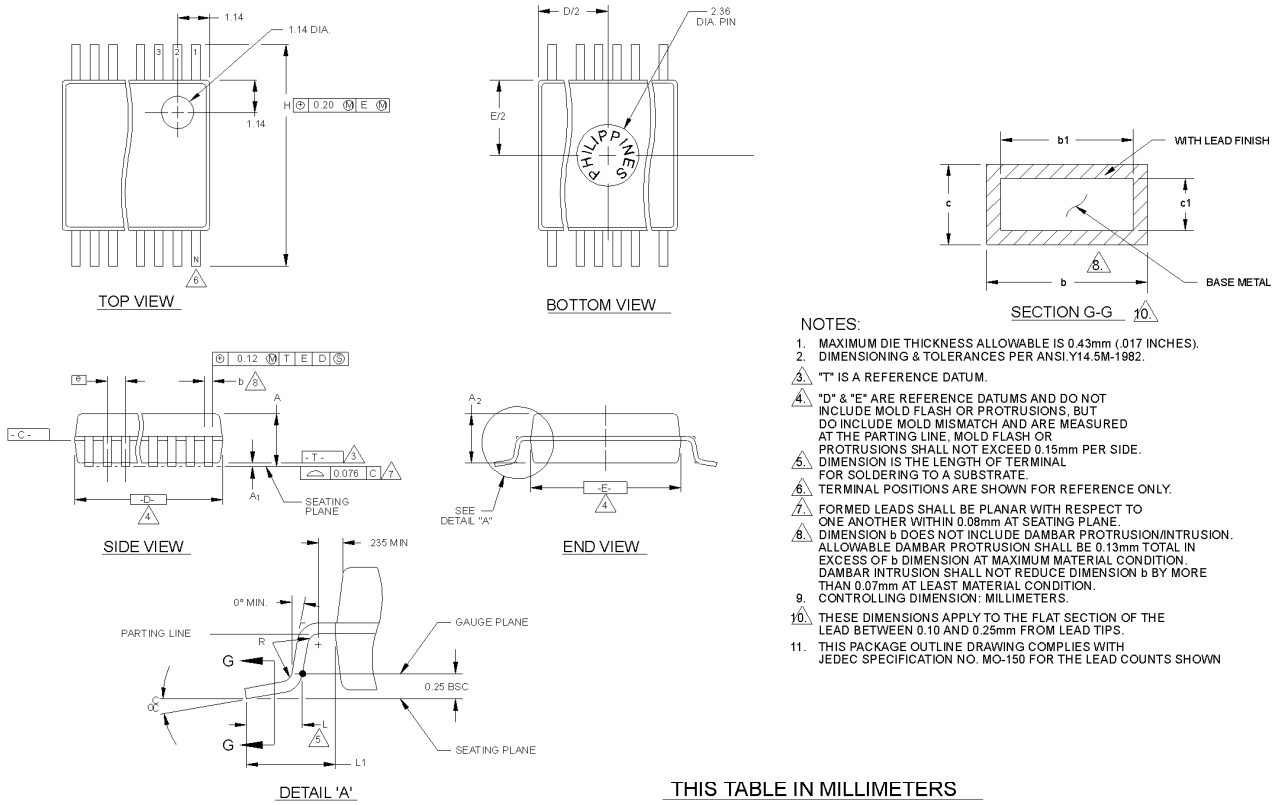
Ordering Information

Ordering Code	Option	Package Name	Package Type
W162	-09, -19	G H	16-pin Plastic SOIC (150-mil) 16-pin Plastic SSOP (209-mil)

Document #: 38-00788-A

Package Diagram

16-pin SSOP Small Shrunk Outline Package (SSOP,209-mil)



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS 0.43mm (.017 INCHES).
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M-1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE PARTING LINE, MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
7. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.08mm AT SEATING PLANE.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13mm TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN 0.07mm AT LEAST MATERIAL CONDITION.
9. CONTROLLING DIMENSION: MILLIMETERS.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25mm FROM LEAD TIPS.
11. THIS PACKAGE OUTLINE DRAWING COMPLIES WITH JEDEC SPECIFICATION NO. MO-150 FOR THE LEAD COUNTS SHOWN

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE 4 VARIATIONS	D			N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	1.73	1.86	1.99		AA	6.07	6.20	6.33	14
A_1	0.05	0.13	0.21		AB	6.07	6.20	6.33	16
A_2	1.68	1.73	1.78		AC	7.07	7.20	7.33	20
b	0.25	-	0.38	8,10	AD	8.07	8.20	8.33	24
b1	0.25	0.30	0.33	10	AE	10.07	10.20	10.33	28
c	0.09	-	0.20	10	AF	10.07	10.20	10.33	30
c1	0.09	0.15	0.16	10					
D	SEE VARIATIONS			4					
E	5.20	5.30	5.38	4					
e	0.65 BSC								
H	7.65	7.80	7.90						
L	0.63	0.75	0.95	5					
L1	1.25 REF.								
N	SEE VARIATIONS			6					
OC	0°	4°	8°						
R	0.09	0.15							

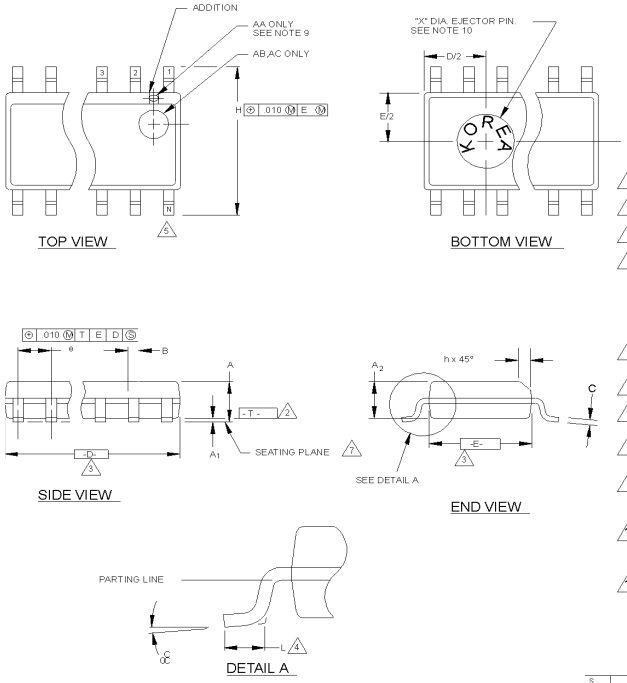
VARIATION AF
IS DESIGNED BUT NOT TOOLED

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE 4 VARIATIONS	D			N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	.068	.073	.078		AA	.239	.244	.249	14
A_1	.002	.005	.008		AB	.239	.244	.249	16
A_2	.066	.068	.070		AC	.278	.284	.289	20
b	.010	-	.015	8,10	AD	.318	.323	.328	24
b1	.010	.012	.013	10	AE	.397	.402	.407	28
c	.004	-	.008	10	AF	.397	.402	.407	30
c1	.004	.006	.006	10					
D	SEE VARIATIONS			4					
E	.205	.209	.212	4					
e	.0256 BSC								
H	.301	.307	.311						
L	.025	.030	.037	5					
L1	.049 REF.								
N	SEE VARIATIONS			6					
OC	0°	4°	8°						
R	.004	.006							

Package Diagram

16-Pin Small Outlined Integrated Circuit (SOIC, 150-mil)



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .015.
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. THE APPEARANCE OF PIN #1 I.D ON THE 8 LD IS OPTIONAL, ROUND TYPE ON SINGLE LEADFRAME AND RECTANGULAR TYPE ON MATRIX LEADFRAME.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPEND ON ASSEMBLY LOCATION.
11. CONTROLLING DIMENSION: INCHES.

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARIATIONS	3 D			5 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	.061	.064	.068		AA	.189	.194	.196	8
A_1	.004	.006	.0098		AB	.337	.342	.344	14
A_2	.055	.058	.061		AC	.386	.391	.393	16
B	.0138	.016	.0192						
C	.0075	.008	.0098						
D	SEE VARIATIONS			3					
E	.150	.155	.157						
e	.050 BSC								
H	.230	.236	.244						
h	.010	.013	.016						
L	.016	.025	.035						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	.085	.093	.100						

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARIATIONS	3 D			5 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	1.55	1.63	1.73		AA	4.80	4.93	4.98	8
A_1	0.127	0.15	0.25		AB	8.58	8.69	8.74	14
A_2	1.40	1.47	1.55		AC	9.80	9.93	9.98	16
B	0.35	0.41	0.49						
C	0.19	0.20	0.25						
D	SEE VARIATIONS			3					
E	3.81	3.94	3.99						
e	1.27 BSC								
H	5.84	5.99	6.20						
h	0.25	0.33	0.41						
L	0.41	0.64	0.89						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	2.16	2.36	2.54						