

Evaluation Unit of THS8083

1. Overview and main components of the evaluation circuit board.

The evaluation unit is designed to fully evaluate all the functions of the THS8083 device, meanwhile the design of the print circuit board can be used as a reference when customers try to design a system by using THS8083.

The figure 2 is block diagram of the PC board. Based on the diagram, the PC board consists of following main parts.

- THS8083 device. The package of this device is implemented in the power-pad package. So the PCB area directly under THS8083 is exposed cooper. The exposed bottom of the die of the device should be soldered to this area of the board. This will dramatically help the heat dissipation of the device, and increase the reliability of the system.
- The ALTERA FPGA contains all the control logic of the panel display. It has I2C slave module with device address 80H, display data formatter, and display timing generator.
- Two voltage regulators are U16 and U20. Both of them are TPS73HD301, each has dual voltage outputs. This is the power pad package also, the bottom of the device is soldered on the PCB board's ground plan to help the heat dissipation.

2. Connectors and their usage

Following are the connectors that will be used for THS8083 function evaluation. There may be more connectors than the ones are shown in the block diagram or in schematics. But they will not be used for THS8083 evaluation. Please ignore those that are not on the schematics.

- The power supply of the evaluation unit is provided by a single external power supply, which should be connected to a DIN-5 connector of the unit.
- Video input signals from PC graphics card can be connected to the DB15 VGA connector, or to the five separated SMA connectors on the board. For the best performance, these SMA connectors should be used. A video cable with five separated BNC connectors is shipped with the evaluation unit to fully explore the THS8083. There are no jumper selections on the board to connect or disconnect the video-input signal from the DB15 or SMAs. Only one of the two connectors (DB15 or SMA) can be connected to input signals at the same time.
- DB25 is used to connect to a PC's parallel port. A window program in the PC will control the THS8083 and FPGA on the board via this connection. For details, please refer to the software manual.
- A 60-pin connector is used to connect to the LCD panel display via a ribbon-cable. The other end of a ribbon cable is an adapter on a small PCB, which is used for connecting to back of a LCD panel.
- A 6-pin connector is used to connect to a back-light module of the LCD panel. Associated with this connector, there is a potentiometer for the brightness adjustment.

Note: The Black-color wire of the back-light cable is corresponding to pin 1 of the header (U14) on the PC board. Make sure this connection is right before turn on the power.

Following figure dictated the orientation of this connection.

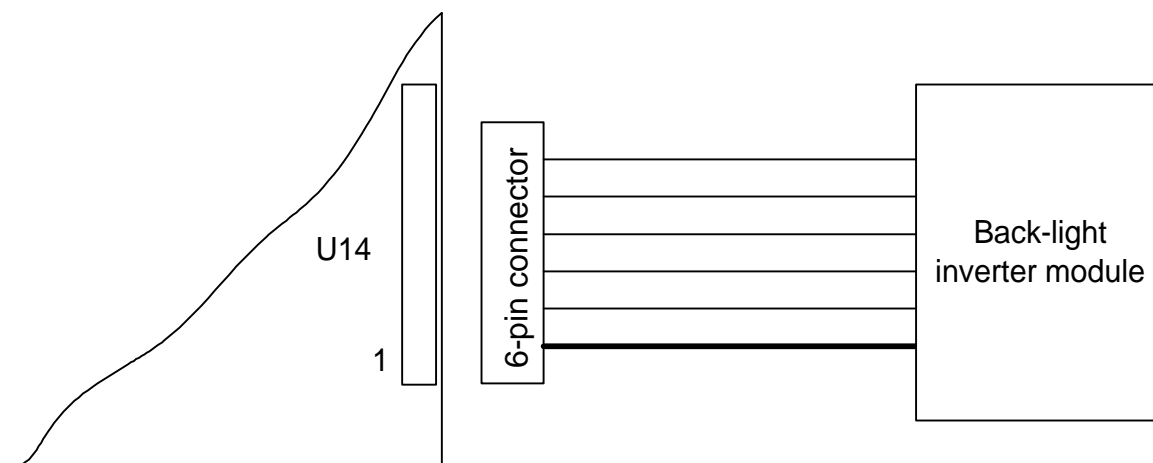


Figure 2. The power cable connection of back-light inverter module to THS8083 EVM board.

3. FPGA Controller

Figure3 is the top-level design schematic of the ALTERA FPGA. Figure4 is the block diagram of this design. These diagrams present a good overview of the functions of the FPGA controller. If the design of the FPGA is needed, please contact your TI local sales office. Following are the main module inside this FPGA.

- I2C slave module has been implemented. This allows a PC to control all the devices on board through a single interface.
- Timing generator generates the HS, VS timing for display module interface
- Data path manager controls interfacing different modes from THS8083 output data to LCD panel
- Register bank stores all the register settings from PC via I2C

For programmable setting, please refer to the software Manuel.

4. Jumper setting table

The order of jumpers in following table is arranged according to their physical location on the PCB. Starting from the left-up corner of the board, then goes to right-down of the board.

Jumper name	Setting	Description
JP22	OPEN	Not used, always open
JP5	Close	Digital 3.3V supply, always close
JP52	Close	Digital 3.3V supply for digital data buffer, always close
JP2	Close	3.3V of digital PLL of THS8083
JP62	Open	These two pins are for the I2C testing, always open
JP57	Close	The THS8083 I2C address selection. When it is closed, the I2C address of THS8083 is 40H for writing and 41H for reading. When it is open, the I2C address of THS8083 is 42H for writing and 43H for reading.
JP1	Close	Analog 3.3V power supply for the PLL in THS8083

JP61	Close	When the middle pin is connected to the 'PC' mark, the input vertical sync signal comes from a PC graphics card. When the middle pin is connected to the 'PLD' mark, the vertical sync signal is generated by the ALTERA FPGA.
JP21	Open	Not used for this version PCB
JP35	Open	Not used for this version PCB
JP20	Open	Not used for this version PCB
JP43	Close	FPGA 3.3V power supply, always closed
JP40	Open	Not used for this version PCB
JP41	Open	Not used for this version PCB
JP42	Open	Not used for this version PCB
JP23	Close	Enable/disable the data bus buffer, middle pin connected 'EN' pin will enable the bus buffer.
JP26	Close	Enable/disable the data bus buffer, middle pin connected 'EN' pin will enable the bus buffer.
JP68	Open	Always open, this is the test point of vertical sync signal.
JP67	Open	Always open, this is the test point of PLL locking signal of THS8083.
JP9	Open	Not used for this version PCB
JP69	Open	Not used for this version PCB
JP70	Open	Not used for this version PCB
JP71	Open	Not used for this version PCB
JP46	Open	Not used for this version PCB
JP50	Open	Not used for this version PCB
JP12	Open	Not used for this version PCB
JP17	Open	Not used for this version PCB
JP38	Close	FPGA output enable, always close to enable
JP39	Open	Not used for this version PCB
JP13	Open	Test point of ADCCLK1 of THS8083
JP47	Open	Test point of ACDCLK1 of THS8083
JP48	Open	Test point of ADCCLK2 of THS8083
JP49	Open	Test point of DTOCLK3 of THS8083
JP60	Close	Output enable of THS8083, always close to enable it
JP25	Open	Not used for this version PCB
JP27	Open	Not used for this version PCB
JP4	Open	Not used for this version PCB
JP16	Open	Not used for this version PCB
JP15	Open	Not used for this version PCB
JP33	Close	When middle pin is connected to 'SW', the reset signal comes from the U22(TLC7703, voltage supervising device)
JP36	Close	ADCCLK1 is selected for the input clock of FPGA
JP34	Open	If it is closed, the DTOCLK3 will be selected as the clock of FPGA
JP37	Open	Not used for this version PCB
JP29	Close	The middle pin is connected to 'EN' to enable video data output to LCD panel
JP30	Close	The middle pin is connected to 'EN' to enable video data output to LCD panel
JP3	Close	Analog 3.3V power supply, always close
JP32	Close	Analog 3.3V power supply, always close
JP53	Close	Analog 3.3V power supply, always close
JP7	Open	Not used for this version PCB
JP8	Open	Not used for this version PCB
JP10	Open	Not used for this version PCB
JP11	Open	Not used for this version PCB
JP14	Open	Not used for this version PCB

JP19	Open	Not used for this version PCB
JP18	Open	Not used for this version PCB

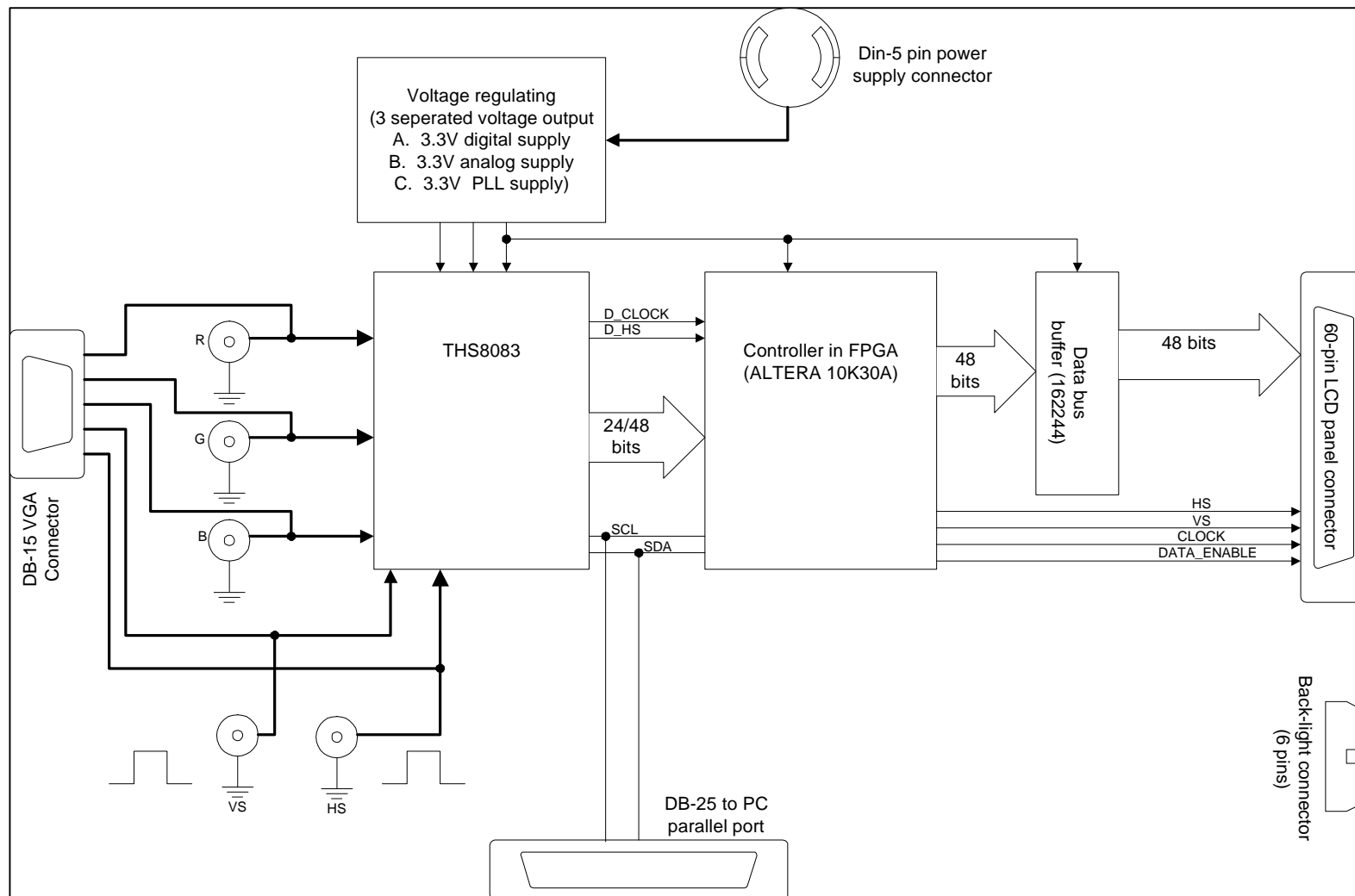
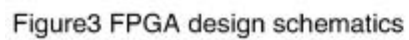


Figure2 Block diagram of the THS8083 evaluation circuit board



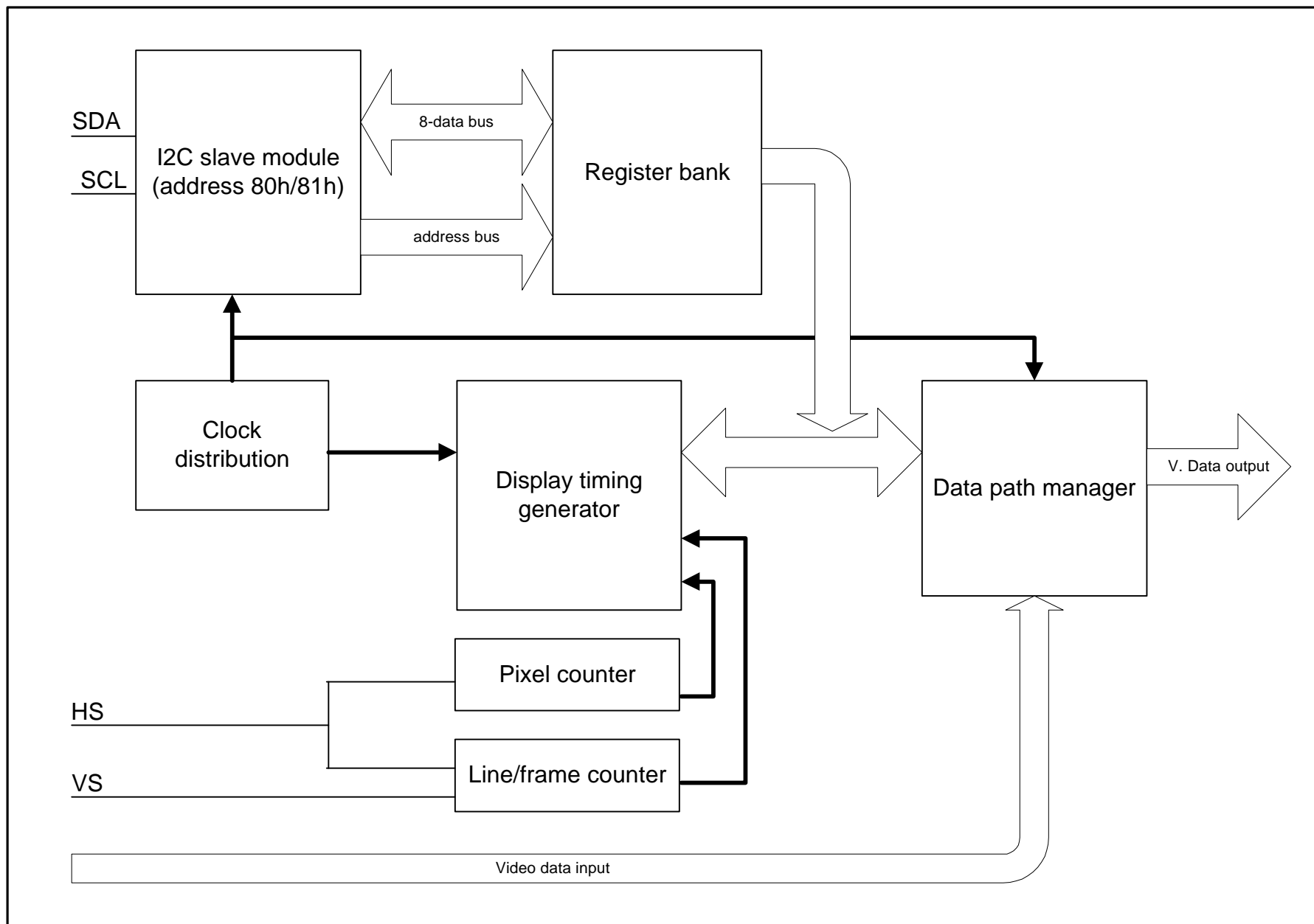
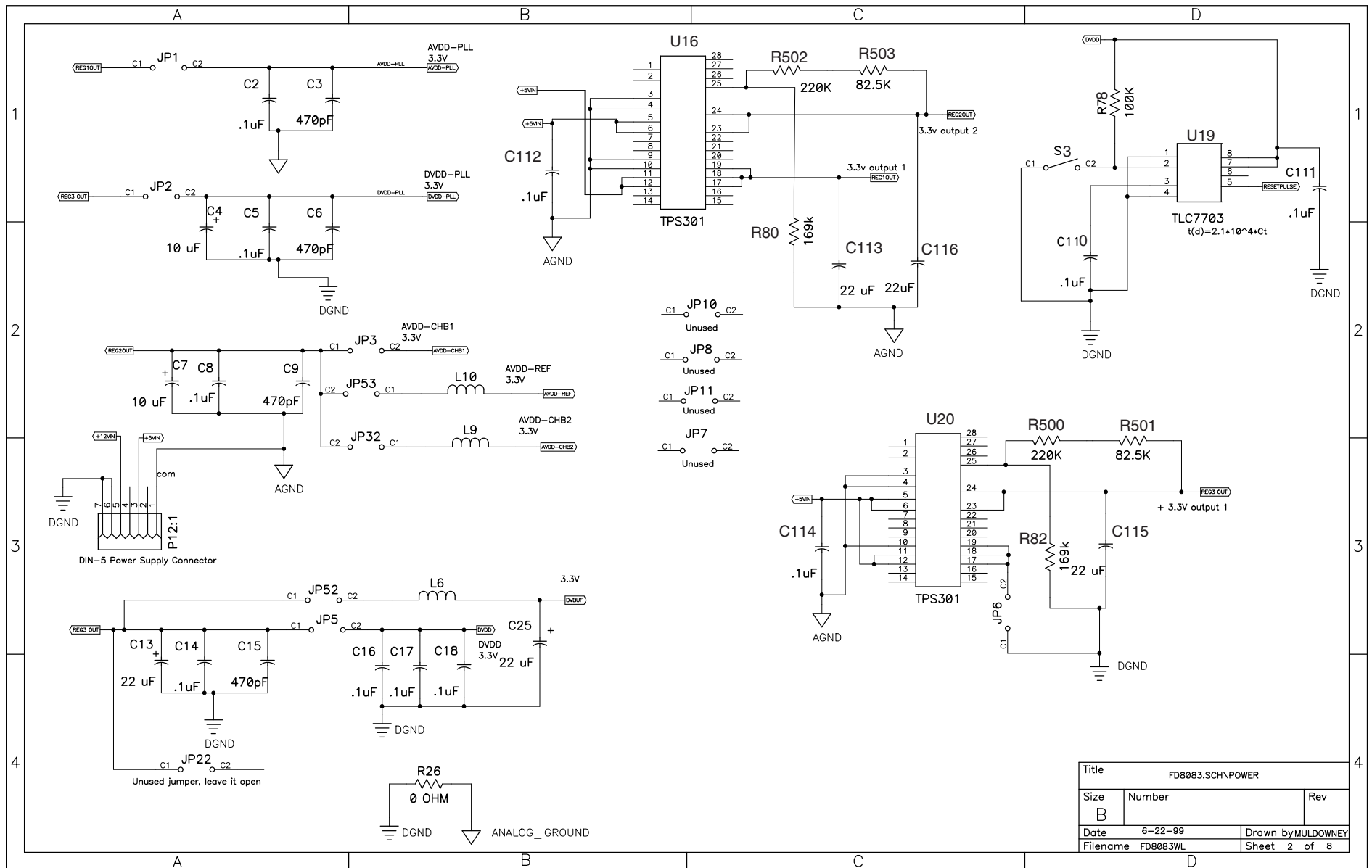
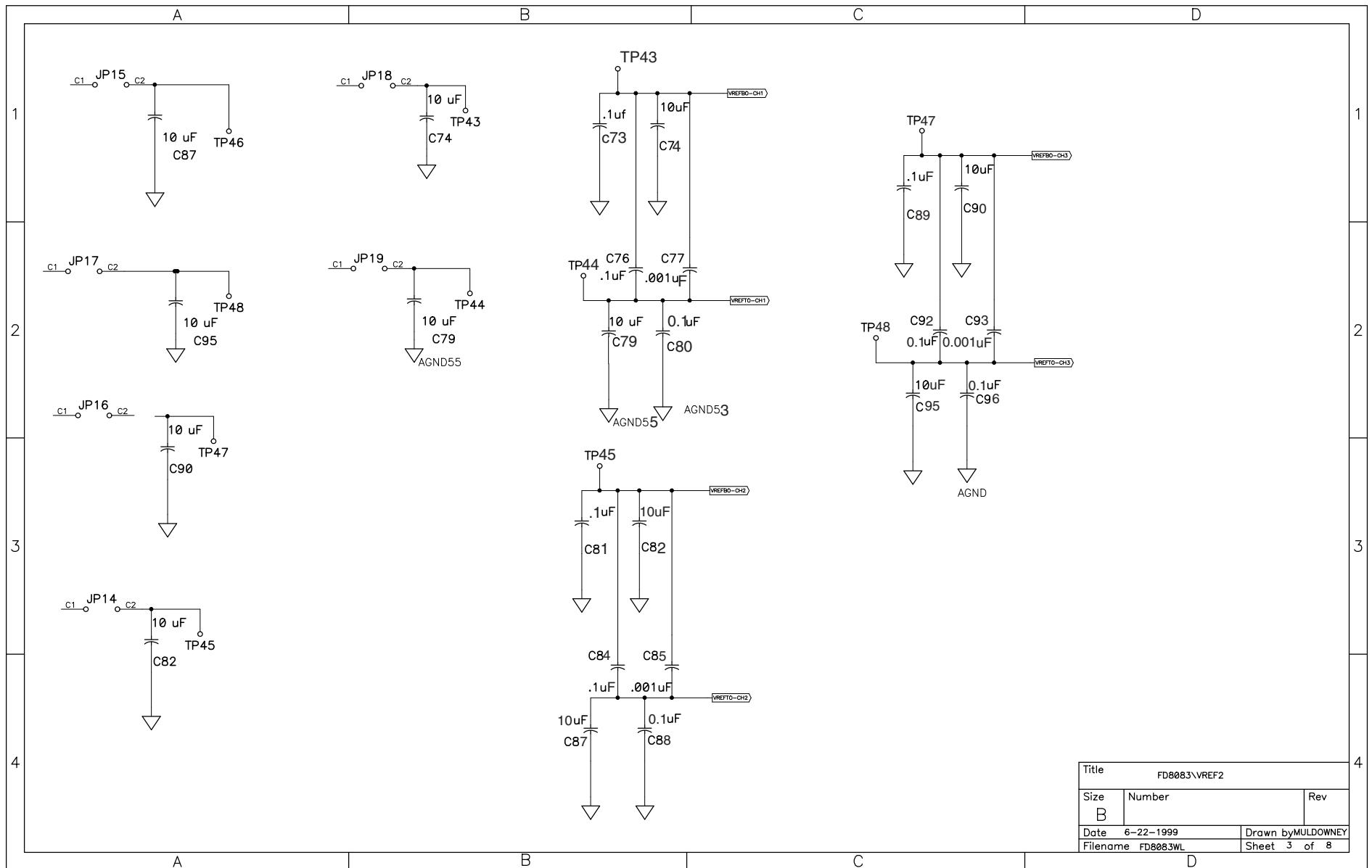


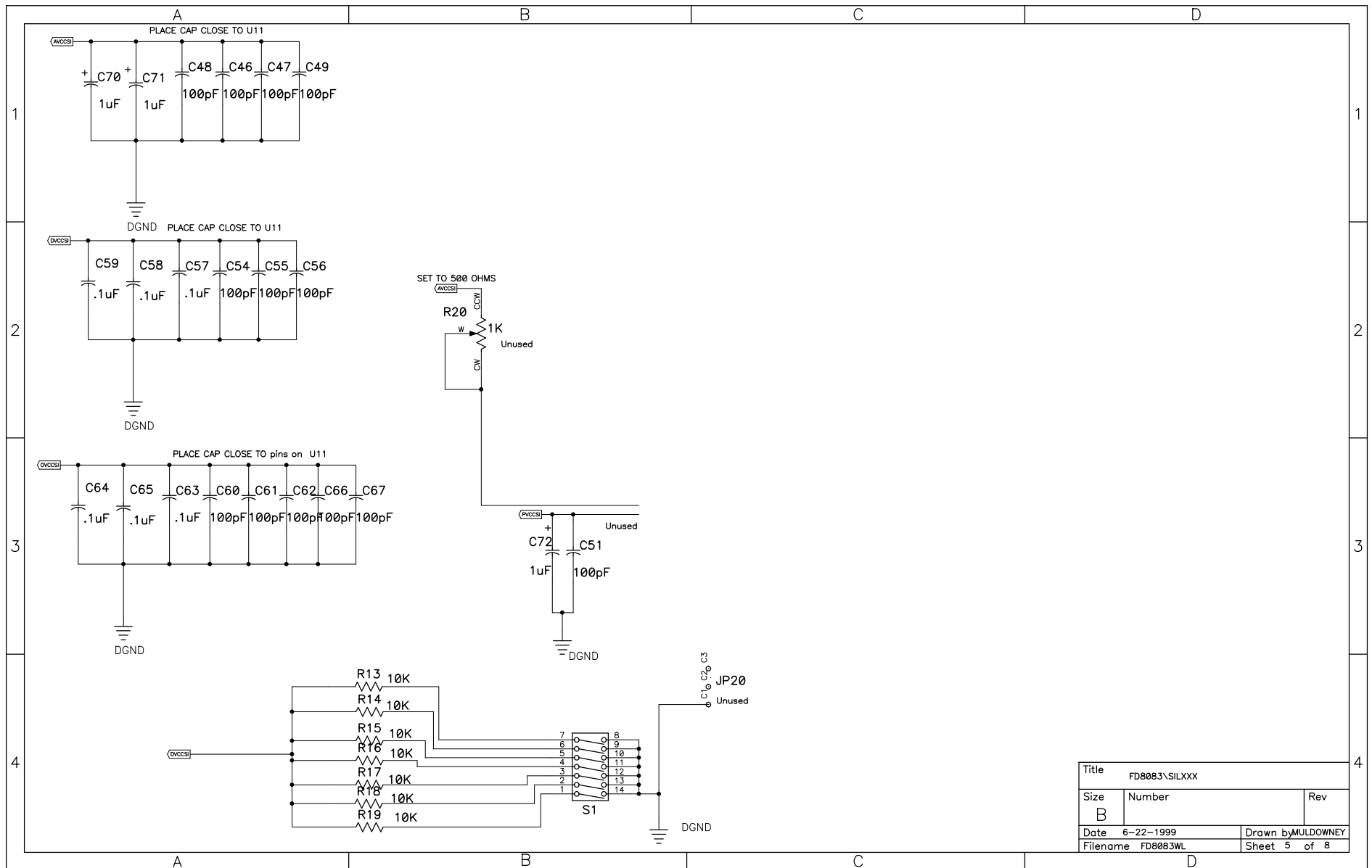
Figure4 Block diagram FPGA design



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FD8083.SCH\POWER		
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Date	6-22-99	Drawn by MULDOWNNEY
Filename	FD8083.WL	Sheet 2 of 8



Title		
FD8083\VREF2		
Size	Number	Rev
B		
Date	6-22-1999	Drawn byMULDOWNNEY
Filename	FD8083WL	Sheet 3 of 8



Title		
FD8083\SILXXX		
Size	Number	Rev
B		
Date	6-22-1999	Drawn by
Filename	FD8083WL	Sheet 5 of 8

