PLESSEY
Semiconductors

SL2541B

800MHz HIGH SLEW RATE OP-AMP

The Plessey SL2541B combines high slew rate and fast settling times with the flexibility of standard operational amplifier configurations.

To cover the many requirements of high speed op-amp applications the SL2541 has been designed such that many of its important parameters can be externally programmed. These include open loop gain, output current, supply voltage range and output DC offset. Included within the device is a band gap reference for good temperature stability and a separate video speed buffer.

The SL2541 is capable of driving directly into 50Ω with bandwidths in excess of 800MHz.

FEATURES

- 1400/μs Slew Rate (Rising)
- 900V/μs Slew Rate (Falling)
- Fast Settling Time, 30ns to 0.5%
- Full Power Bandwidth of 40MHz
- ±15mA Output Current (Programmable)
- Linear Phase Response

APPLICATIONS

- Radar, Sonar Processors
- Fast Settling Pulse Amplifiers
- Digital and Wideband Analog Communications
- Base Band and Video Communications
- Fast A to D, D to A Conversion

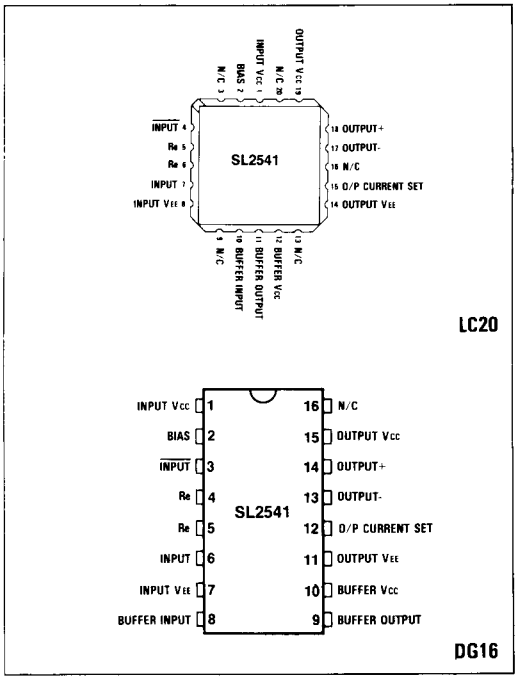

Fig.1 Pin connections - top view

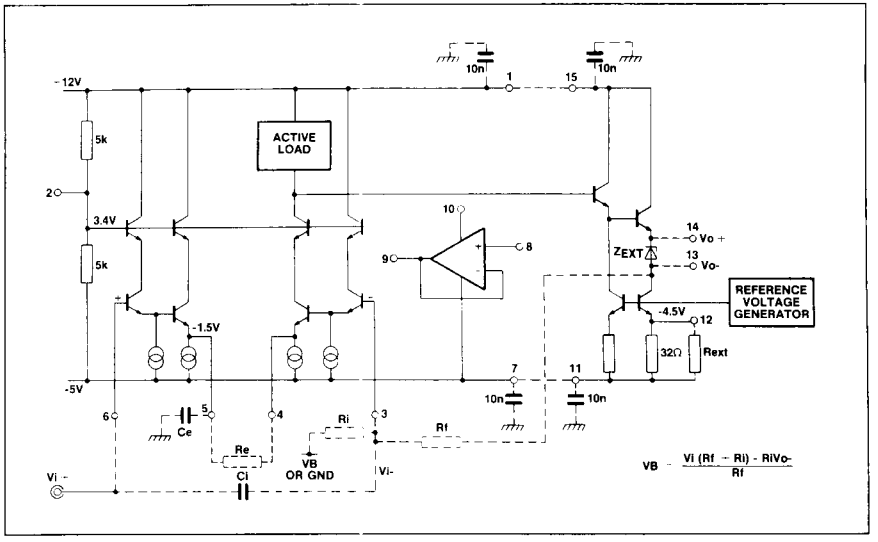

Fig.2 Equivalent circuit with standard external components for non-inverting mode of operation

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 25°C, V_{CC} = +12V, V_{EE} = -5V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input characteristics					
Input offset voltage (Note 1)		10		mV	R_L = 1.2kΩ, R_e = 39Ω
Input offset voltage drift		20		μV/°C	R_L = 1.2kΩ, R_e = 390Ω (Note 1)
Input bias current			20	μA	
Input resistance		250		Ω	Open loop impedance at 500MHz
Input capacitance		3.5		pF	(C and R in parallel)
Input signal handling (p-p)			20	V	V_{CC} = +15V, V_{EE} = -15V.See Biasing Conditions.
Transfer characteristics					
Common mode rejection ratio	47			dB	At DC
Gain bandwidth product		2.5		GHz	R_L = 50Ω, V_{out} = 100mV, x10 gain
Open loop gain	45	70		dB	Single ended drive
Non-inverting bandwidth		800		MHz	x2 gain, 50Ω load
Inverting bandwidth		220		MHz	x10 gain, 50Ω load
On-chip buffer bandwidth		60		MHz	R_L = 1kΩ to V_{EE}
Noise figure		8		dB	x2 gain non-inverting, R_S = 50Ω at f = 100MHz
Output characteristics					
Output current		±10	±15	mA	See biasing conditions, programmable
Full power bandwidth		40		MHz	x10 inverting, 10V p-p, R_L = 1.2kΩ
Output resistance		10		Ω	Open loop measurement
Output signal handling (p-p)		-	12	V	V_{CC} = +15V, V_{EE} = -15V
Transient response					
Rise time		1.6		ns	
Fall time		3.2		ns	
Overshoot		10		%	R_L = 1.2kΩ
Slew rate (rising edge)		1400		V/μs	x2 gain non-inverting
Slew rate (falling edge)		900		V/μs	10% to 90% measurement
Settling time to 0.5 %		30		ns	
Settling time to 0.1 %		40		ns	
Power requirements					
Supply voltage V_{EE} to V_{CC}	14		30	V	
Supply voltage range V_{CC}	+9		+15	V	
V_{EE}	-5		-15	V	
Supply current		25		mA	No load, V_{EE} = -5V, V_{CC} = +12V
Power supply rejection ratio		40		dB	
Buffer output current		15		mA	Pull-down resistor required

NOTE
1. Input offset is dependent on R_e. For lowest offset R_e = 10 ohms

ORDERING INFORMATION

SL2541B DG -30°C to +85°C
SL2541B LC -30°C to +85°C
SL2541AC DG -55°C to +125°C To MIL-883C
SL2541AC LC -55°C to +125°C Class B

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE})	35V
Input Voltage (Inv I/P to Non-Inv I/P)	±10V
Storage Temperature	-65° C to +175° C
Chip Operating Temperature	+175° C
Operating Temperature: DIL	-55° C to +125° C
Thermal Resistances:	
Chip-to-Ambient: DIL	125° C/W
Chip-to-Case: DIL	40° C/W

APPLICATION NOTES

The SL2541 may be used as a high frequency, non-saturating amplifier in any of the usual op-amp configurations (amplifiers, integrators). In most applications, the output of the SL2541 is taken from pin 13 (V_{out-}), but DC level shifting can be obtained by applying feedback from pin 13 to pin 3 and taking the output from pin 14 (V_{out+}), see Fig.2. Alternatively, a DC offset can be applied through the low-drift on-chip buffer (pins 8 and 9) to V_B.

The Zener diode between pins 13 and 14 can also be divided into smaller value Zeners or resistors to give different DC levels at the output.

Biasing Conditions (25° C)

For undistorted outputs the peak signal voltages on Vo+, Vo-, and the inputs should comply with the following conditions:

A. $Vo+_{(MIN)} \geq \frac{V_{CC} + V_{EE}}{2} - 1.4V$

B. $Vo+_{(MAX)} \leq V_{CC} - 4.0V$

C. $Vo-_{(MIN)} \geq V_{EE} + 1.4V$

D. $Vi+ \text{ and } Vi- \leq \frac{V_{CC} + V_{EE}}{2} - 0.9V$

E. $Vi+ \text{ and } Vi- \geq V_{EE} + 3.2V$

For applications using symmetrical supplies, the peak input voltage should be below ground by 0.9V. If this is not acceptable then pin 12 of the device can be redefined externally. See Fig.2 and Biasing Condition D.

Rx is used to balance the offset voltage between the two inputs (see Fig.3).

Bias voltage values at several nodes are indicated on Fig.2.

R_{ext} is connected from pin 12 to pin 11 (V_{EE}) to increase output bias current I_{out}. This current should not exceed 30mA. The value of R_{ext} is calculated as follows:

$$R_{ext} = \left[\frac{500}{I_{out} - 10}\right]\Omega$$

where I_{out} is in mA.

Buffer

The on-chip buffer has a small-signal bandwidth of 60MHz with 1kΩ load, and has an input/output signal handling capability of 8V. The output can deliver 15mA; an external pull-down resistor is required.

High Frequency Stability

All component leads should be kept as short as possible, particularly at the summing junction. A ground plane should be used to minimise any earth induced currents between the input and output circuits. The use of good power supply bypass capacitors (10nF Ceramic) will improve the overall performance. They should be located close to the device supply pins. Signal source and load should be located close to the circuit with good termination. For 50Ω source use a 50Ω bead resistor. Other resistors should be carbon composition type.

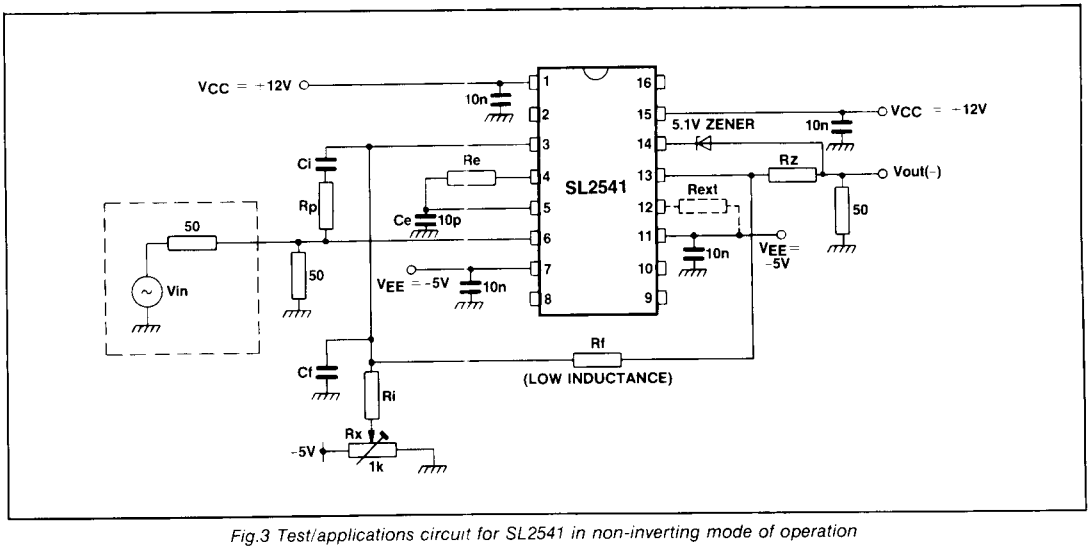

Fig.3 Test/applications circuit for SL2541 in non-inverting mode of operation

Voltage Gain

Stable closed loop operation is ensured by changing the value of the degeneration resistor (R_e) between pins 4 and 5 according to the selected closed loop gain. As closed loop gain is decreased the value of R_e should be increased. A graph of recommended value of R_e with gain is given in Fig 8.

Power Dissipation

A Zener diode is used between pins 13 and 14 to dissipate power externally and provide DC offset at the output. Although some power is dissipated in the external Zener, a heatsink on the SL2541 will be necessary if the power exceeds 800mW dissipation.

Bandwidth Compensation

When operated at inverting mode any peaking due to board and component strays can be compensated by the following methods.

A. A capacitor of small value between the two inputs will roll off high frequency pass band region e.g. 1.8pF is used for x1 and x10 gain settings with PCB layout shown in Fig.18.

B. A capacitor of suitable value across the input resistor to compensate for any strays from the other input to ground. e.g. 10pF used for x10 gain frequency response.

C. A resistor of suitable value (R_Z) in series with the Zener diode does reduce the high frequency peak and also adjusts the output voltage swing. (See Fig.3) e.g. a 56Ω resistor used for x20 gain frequency response.

In non-inverting mode of operation when using method **A** a resistor of suitable value in series with a small capacitor used is to compensate the bandwidth. e.g. a 680Ω resistor with 1.8pF capacitor in series is used to increase the passband region to 800MHz at x2 gain settings.

Generally, a combination of these three methods will keep the response stable and eliminate the peaking at other operating conditions.

Also in inverting mode a decoupling capacitor from pin 5 will increase the first pole roll off and hence reduce the noise bandwidth. For example a 10pF capacitor will increase the roll off from 38dB/dec to 63dB/dec.

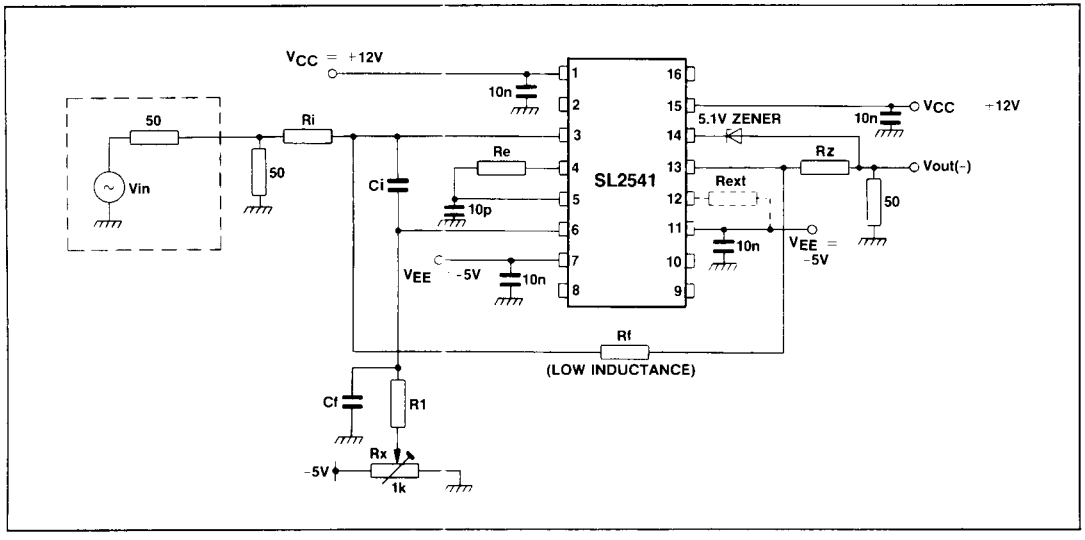

Fig.4 Test/applications circuit for SL2541 in inverting mode of operation

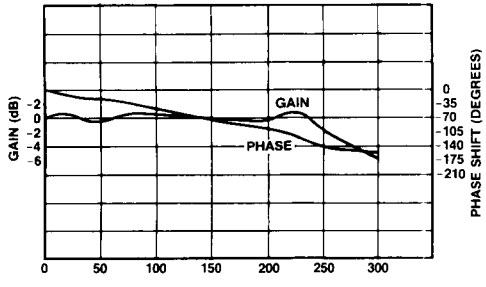

Fig.5 Typical frequency/phase performance graphs for circuit of Fig.4. Inverting, 50Ω load, V_{CC} = +12V, V_{EE} = -5V

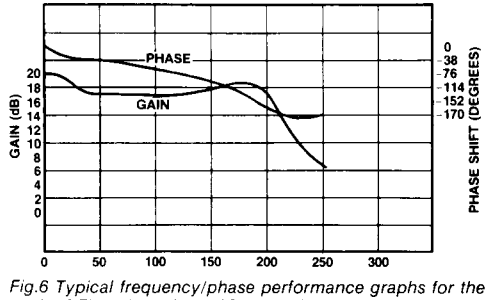

Fig.6 Typical frequency/phase performance graphs for the circuit of Fig.4. Inverting, 50Ω load, V_{CC} = +12V, V_{EE} = -5V

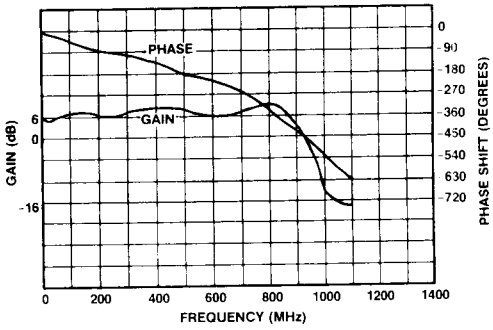

Fig.7 Typical frequency/phase performance graphs for the circuit of Fig.3, non-inverting, x2 gain, 50Ω load, V_{CC} = +12V, V_{EE} = -5V

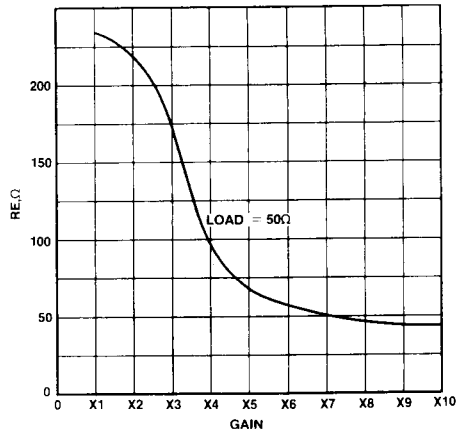

Fig.8 Typical closed loop gain v. typical values of the degeneration resistor R_e

Response	Gain	R_f(Ω)	R_i(Ω)	R_1(Ω)	Zener	R_z	R_e(Ω)	C_f(pF)	R_p(Ω)	C_l(pF) load	V_{out} (p-p) into 1.2kΩ
Fig.5	x1	470	470	470	5.1V	56	220	1.8	-	10	8V
Fig.6	x10	4.7k	470	470	5.1V	56	39	-	-	3.3	7V
Fig.7	x2	560	560	-	5.1V	100	220	1.8	680	-	5V

Table 1 Recommended component values for the applications circuits of Figs. 3 and 4

NOTE
C_i, C_1, R_p, R_z are compensation network components and are partly dependent on layout and board strays.

TIME DOMAIN RESPONSE GRAPHS FOR THE TEST CIRCUIT OF FIG.3. NON-INVERTING, x2, LOAD 1.2kΩ

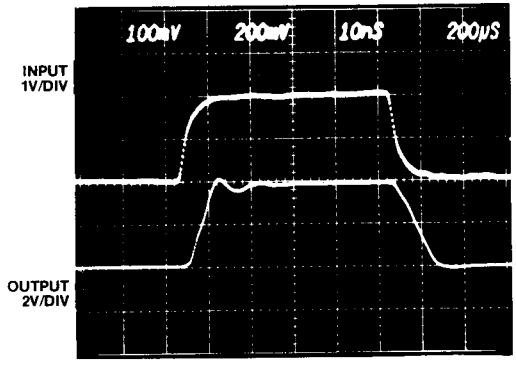

Fig.9 Large signal pulse response

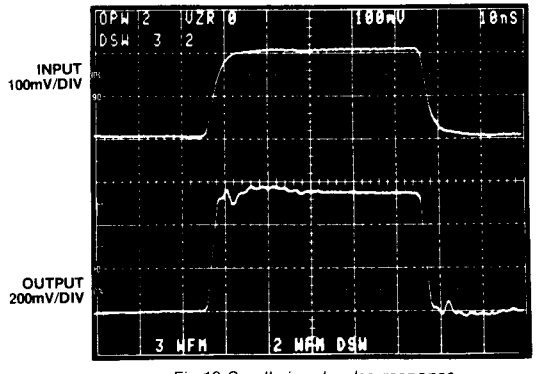

Fig.10 Small signal pulse response

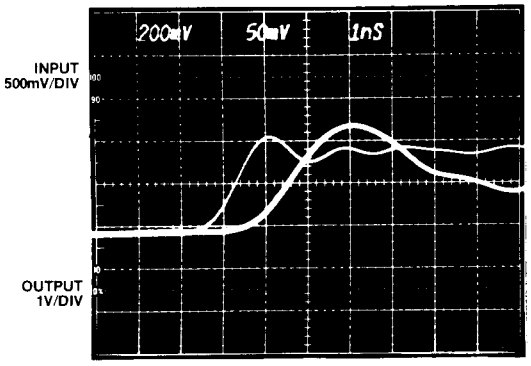

Fig.11 Propagation delay

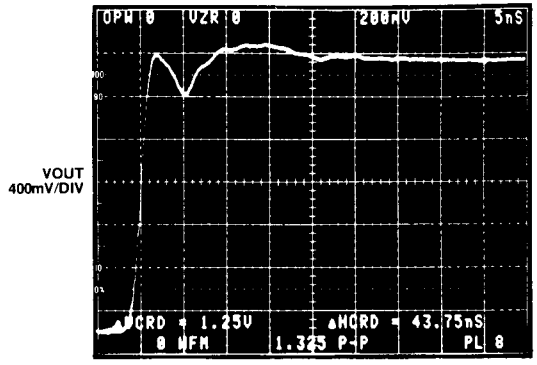

Fig.12 Settling time 2.6V step, 30ns to 0.5%, 40ns to 0.1%

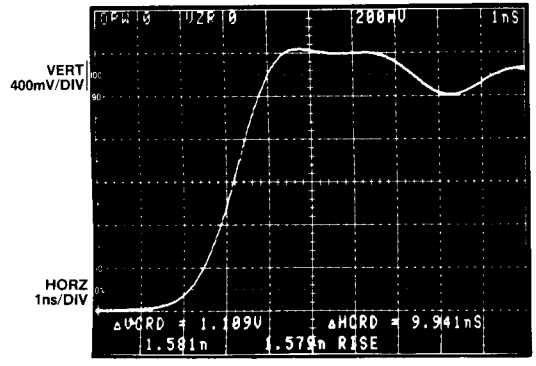

Fig.13 Typical slew rate at the rising edge, 1400V/μs

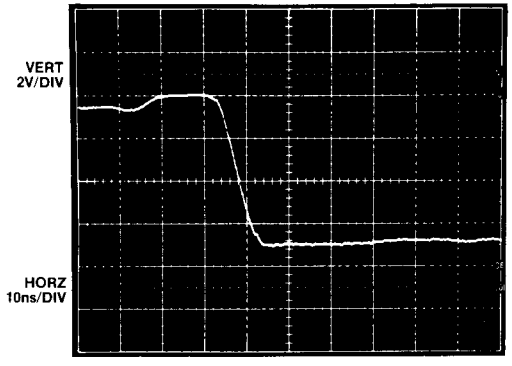

Fig.14 Typical slew rate at the falling edge, 900V/μs

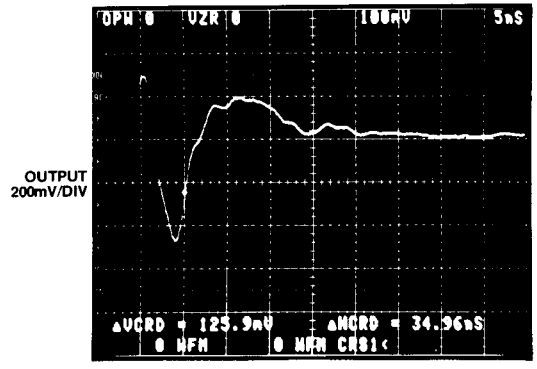

Fig.15 Overshoot <12%, 2.6V p-p step

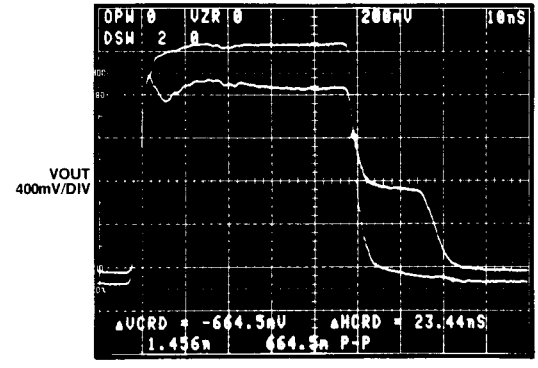

Fig.16 Overload recovery 23ns for 200% overdrive

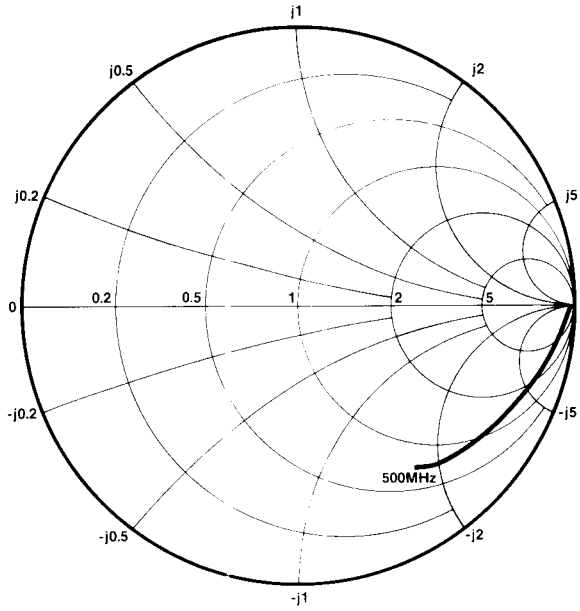

Fig.17 SL2541 open circuit dynamic input impedance normalised to 50Ω. 100MHz frequency markers (see Electrical Characteristics table).

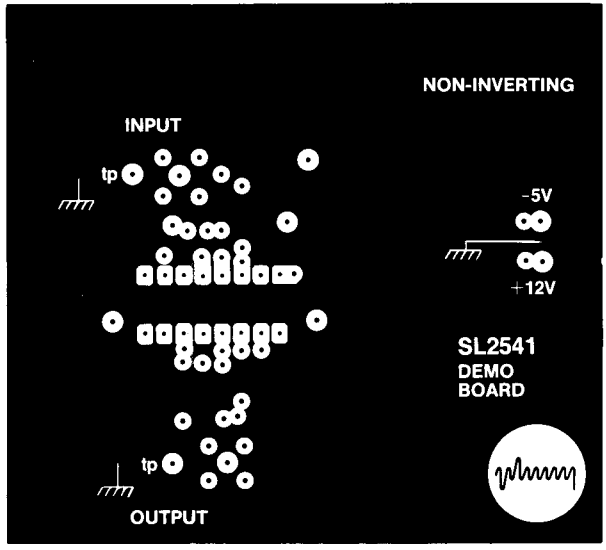

Fig.18(a) SL2541 ground plane (component side)

NOTE: Input and output are sub-vis type 50-ohm connectors. RF is on the track side. Gold socket pins are used to mount the SL2541 for test circuit

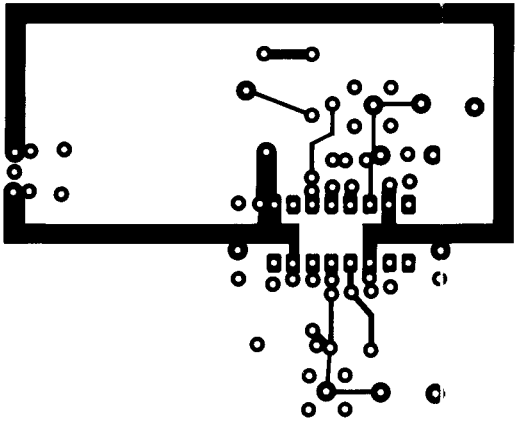

Fig.18(b) SL2541 PCB, track side

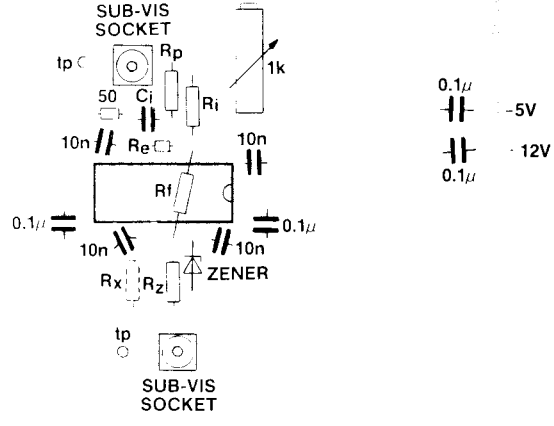

Fig 18(c) SL2541 PCB, component location

Fig.18 PCB layout of SL2541 demonstration board for the circuit of Fig.3 (scale 1:1)