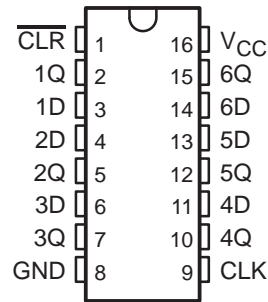


# SN54AHC174, SN74AHC174 HEX D-TYPE FLIP-FLOPS WITH CLEAR

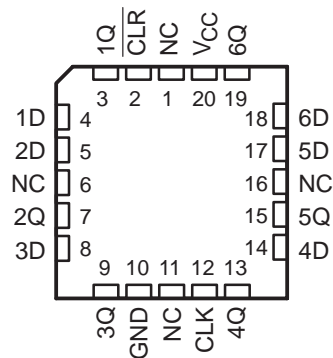
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- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- Operating Range 2-V to 5.5-V  $V_{CC}$
- Contain Six Flip-Flops With Single-Rail Outputs
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs

SN54AHC174 ... J OR W PACKAGE  
SN74AHC174 ... D, DB, DGV, N, OR PW PACKAGE  
(TOP VIEW)



SN54AHC174 ... FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description

The 'AHC174 devices are positive-edge-triggered D-type flip-flops with a direct clear ( $\overline{\text{CLR}}$ ) input and are designed for 2-V to 5.5-V  $V_{CC}$  operation.

Information at the data (D) inputs that meets the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

The SN54AHC174 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74AHC174 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUT Q
$\overline{\text{CLR}}$	CLK	D	
L	X	X	L
H	$\uparrow$	H	H
H	$\uparrow$	L	L
H	L	X	$Q_0$



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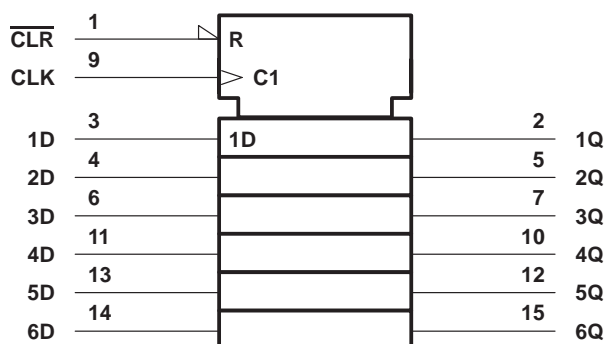
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# SN54AHC174, SN74AHC174 HEX D-TYPE FLIP-FLOPS WITH CLEAR

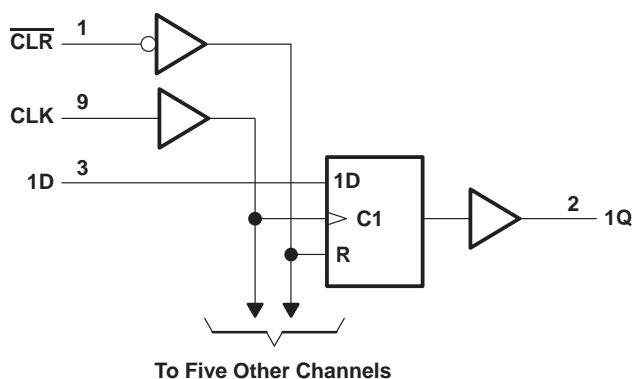
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

## logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

# SN54AHC174, SN74AHC174 HEX D-TYPE FLIP-FLOPS WITH CLEAR

SCLS425E – JUNE 1998 – REVISED JANUARY 2000

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package	73°C/W
DB package	82°C/W
DGV package	120°C/W
N package	67°C/W
PW package	108°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 3)

			SN54AHC174		SN74AHC174		UNIT
			MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage		2	5.5	2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5		1.5		V
		$V_{CC} = 3$ V	2.1		2.1		
		$V_{CC} = 5.5$ V	3.85		3.85		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V		0.5		0.5	V
		$V_{CC} = 3$ V		0.9		0.9	
		$V_{CC} = 5.5$ V		1.65		1.65	
$V_I$	Input voltage		0	5.5	0	5.5	V
$V_O$	Output voltage		0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2$ V		–50		–50	µA
		$V_{CC} = 3.3$ V ± 0.3 V		–4		–4	mA
		$V_{CC} = 5$ V ± 0.5 V		–8		–8	
$I_{OL}$	Low-level output current	$V_{CC} = 2$ V		50		50	µA
		$V_{CC} = 3.3$ V ± 0.3 V		4		4	mA
		$V_{CC} = 5$ V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3$ V ± 0.3 V		100		100	ns/V
		$V_{CC} = 5$ V ± 0.5 V		20		20	
$T_A$	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54AHC174, SN74AHC174

## HEX D-TYPE FLIP-FLOPS

### WITH CLEAR

SCLS425E – JUNE 1998 – REVISED JANUARY 2000

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHC174		SN74AHC174		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 µA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		2.48		
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.5		0.44	
	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.5		0.44	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	0 V to 5.5 V			± 0.1		± 1*		± 1	µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		40		40	µA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		1.7	10				10	pF

\* On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

**timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted)**

			T <sub>A</sub> = 25°C		SN54AHC174		SN74AHC174		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration	CLR low	5		5		5		ns
		CLK high or low	5		5		5		
t <sub>su</sub>	Setup time before CLK↑	Data	5		6		6		ns
		CLR inactive	3		3		3		
t <sub>h</sub>	Hold time, data after CLK↑		0		0		0		ns

**timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted)**

			T <sub>A</sub> = 25°C		SN54AHC174		SN74AHC174		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration	CLR low	5		5		5		ns
		CLK high or low	5		5		5		
t <sub>su</sub>	Setup time before CLK↑	Data	4.5		4.5		4.5		ns
		CLR inactive	2.5		2.5		2.5		
t <sub>h</sub>	Hold time, data after CLK↑		0.5		0.5		0.5		ns

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# SN54AHC174, SN74AHC174 HEX D-TYPE FLIP-FLOPS WITH CLEAR

SCLS425E – JUNE 1998 – REVISED JANUARY 2000

**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC174		SN74AHC174		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			$C_L = 15\text{ pF}$	95*	170*		80*		80		MHz
			$C_L = 50\text{ pF}$	55	130		50		50		
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Any Q	$C_L = 15\text{ pF}$		4.5*	11.4*	1*	13.5*	1	13.5	ns
$t_{\text{PLH}}$	CLK	Any Q	$C_L = 15\text{ pF}$		5.8*	11*	1*	13*	1	13	ns
$t_{\text{PHL}}$					5.8*	11*	1*	13*	1	13	
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Any Q	$C_L = 50\text{ pF}$		6	14.9	1	17	1	17	ns
$t_{\text{PLH}}$	CLK	Any Q	$C_L = 50\text{ pF}$		7.5	14.5	1	16.5	1	16.5	ns
$t_{\text{PHL}}$					7.5	14.5	1	16.5	1	16.5	
$t_{\text{sk(o)}}$			$C_L = 50\text{ pF}$			1.5**				1.5	ns

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

\*\* On products compliant to MIL-PRF-38535, this parameter does not apply.

**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC174		SN74AHC174		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			$C_L = 15\text{ pF}$	130*	240*		110*		110		MHz
			$C_L = 50\text{ pF}$	90	180		80		80		
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Any Q	$C_L = 15\text{ pF}$		3*	7.6*	1*	9*	1	9	ns
$t_{\text{PLH}}$	CLK	Any Q	$C_L = 15\text{ pF}$		4.1*	7.2*	1*	8.5*	1	8.5	ns
$t_{\text{PHL}}$					4.1*	7.2*	1*	8.5*	1	8.5	
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Any Q	$C_L = 50\text{ pF}$		4.2	9.6	1	11	1	11	ns
$t_{\text{PLH}}$	CLK	Any Q	$C_L = 50\text{ pF}$		5.5	9.2	1	10.5	1	10.5	ns
$t_{\text{PHL}}$					5.5	9.2	1	10.5	1	10.5	
$t_{\text{sk(o)}}$			$C_L = 50\text{ pF}$			1**				1	ns

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

\*\* On products compliant to MIL-PRF-38535, this parameter does not apply.

**operating characteristics,  $T_A = 25^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{\text{pd}}$ Power dissipation capacitance	No load, $f = 1\text{ MHz}$	15.2	pF

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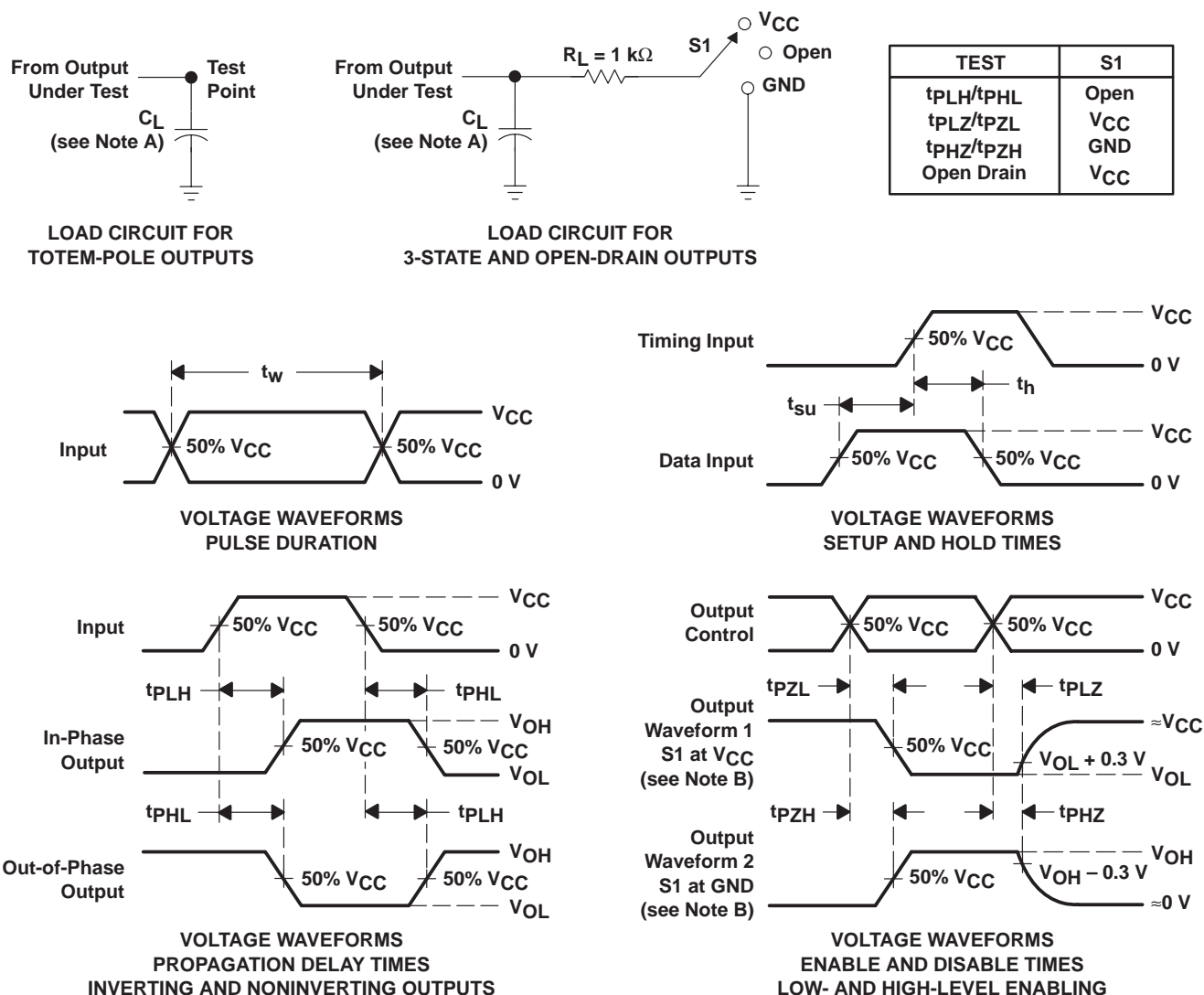


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# SN54AHC174, SN74AHC174 HEX D-TYPE FLIP-FLOPS WITH CLEAR

SCLS425E – JUNE 1998 – REVISED JANUARY 2000

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .  
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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