

SN54ABT657A, SN74ABT657A OCTAL TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS

SCBS192E – JANUARY 1991 – REVISED JUNE 1997

- State-of-the-Art *EPIC-II^B*™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs

description

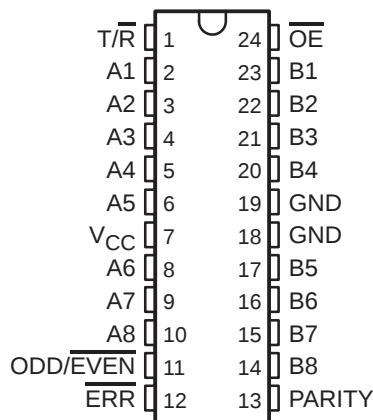
The 'ABT657A transceivers have eight noninverting buffers with parity-generator/checker circuits and control signals. The transmit/receive ($T/\bar{R}$) input determines the direction of data flow. When $T/\bar{R}$ is high, data flows from the A port to the B port (transmit mode); when $T/\bar{R}$ is low, data flows from the B port to the A port (receive mode). When the output-enable ($\overline{OE}$) input is high, both the A and B ports are in the high-impedance state.

Odd or even parity is selected by a logic high or low level on the $ODD/\overline{EVEN}$ input. $PARITY$ carries the parity-bit value; it is an output from the parity generator/checker in the transmit mode and an input to the parity generator/checker in the receive mode.

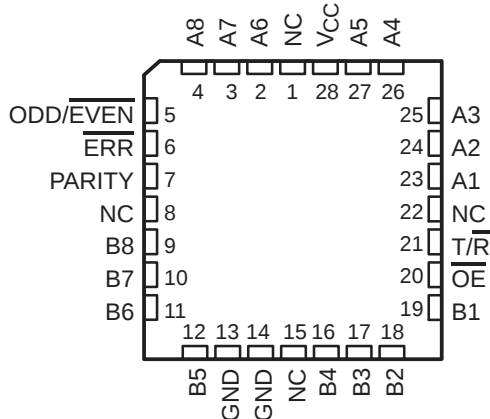
In the transmit mode, after the A bus is polled to determine the number of high bits, $PARITY$ is set to the logic level that maintains the parity sense selected by the level at $ODD/\overline{EVEN}$. For example, if $ODD/\overline{EVEN}$ is low (even parity selected) and there are five high bits on the A bus, $PARITY$ is set to the logic high level so that an even number of the nine total bits (eight A-bus bits plus parity bit) are high.

In the receive mode, after the B bus is polled to determine the number of high bits, the error ($\overline{ERR}$) output logic level indicates whether or not the data to be received exhibits the correct parity sense. For example, if $ODD/\overline{EVEN}$ is high (odd parity selected), $PARITY$ is high, and there are three high bits on the B bus, $\overline{ERR}$ is low, indicating a parity error.

SN54ABT657A . . . JT PACKAGE
SN74ABT657A . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ABT657A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



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INSTRUMENTS**

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SN54ABT657A, SN74ABT657A

OCTAL TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS

AND 3-STATE OUTPUTS

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description (continued)

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT657A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT657A is characterized for operation from -40°C to 85°C .

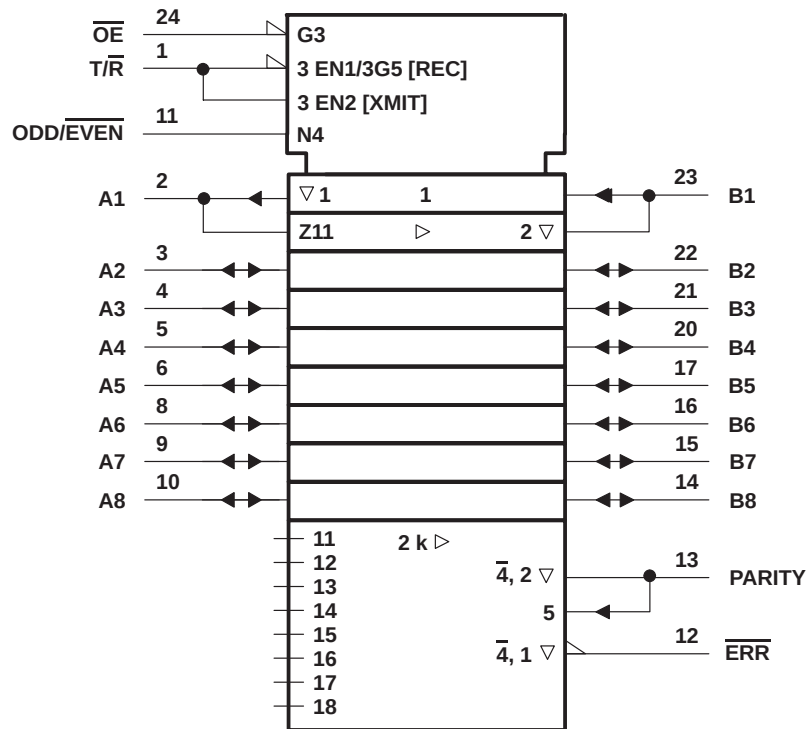
FUNCTION TABLE

NUMBER OF A OR B INPUTS THAT ARE HIGH	INPUTS			I/O PARITY	OUTPUTS	
	$\overline{OE}$	$\overline{TI/R}$	ODD/ $\overline{EVEN}$		$\overline{ERR}$	OUTPUT MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	Z

SN54ABT657A, SN74ABT657A OCTAL TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS

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logic symbol[†]



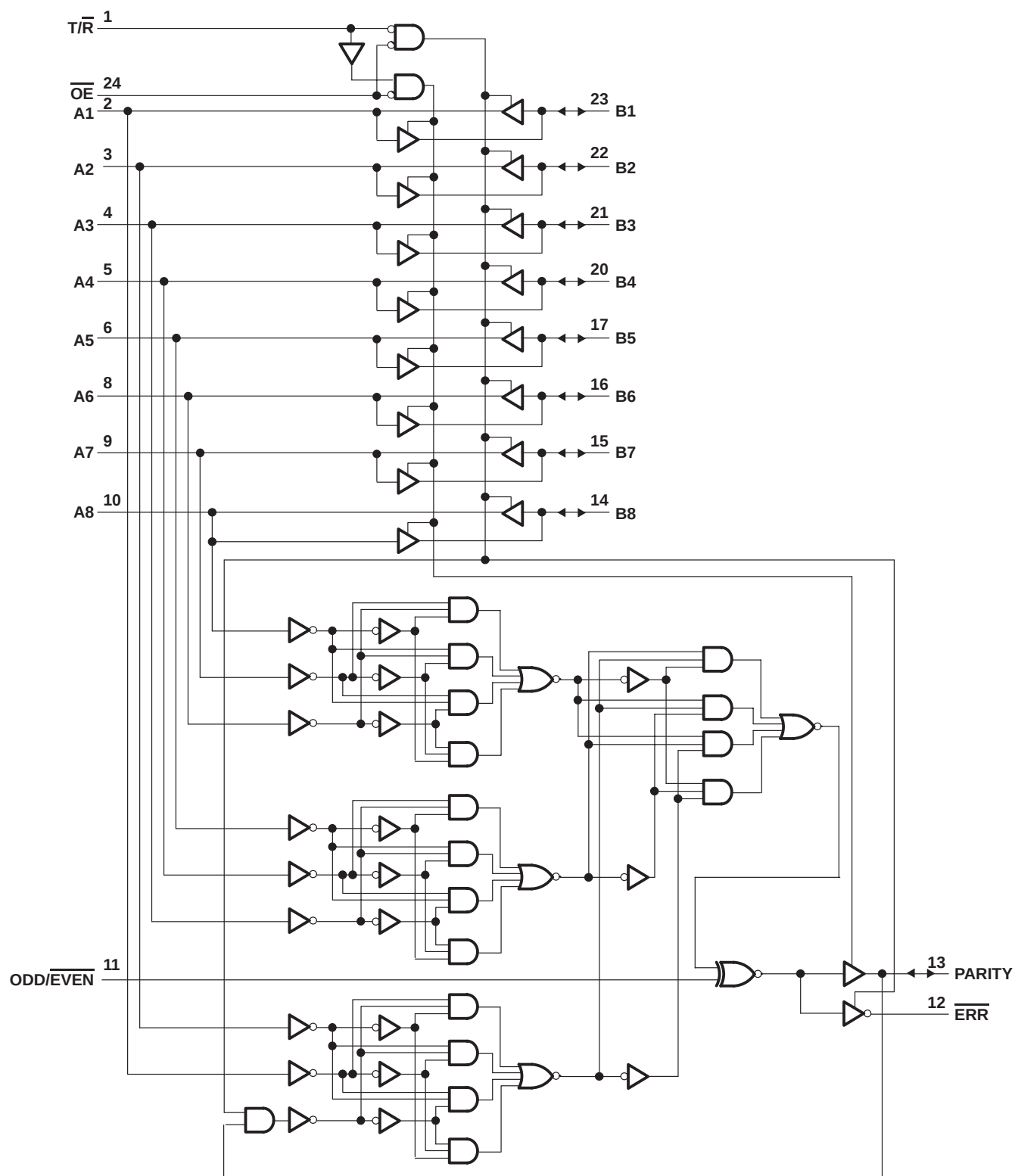
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

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OCTAL TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS

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logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT657A	96 mA
SN74ABT657A	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package	81°C/W
NT package	67°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

		SN54ABT657A		SN74ABT657A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			5	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

SN54ABT657A, SN74ABT657A

OCTAL TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A = 25°C			SN54ABT657A		SN74ABT657A		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = –18 mA		–1.2			–1.2		–1.2		V
V _{OH}		V _{CC} = 4.5 V, I _{OH} = –3 mA		2.5			2.5		2.5		V
		V _{CC} = 5 V, I _{OH} = –3 mA		3			3		3		
		V _{CC} = 4.5 V	I _{OH} = –24 mA	2			2				
			I _{OH} = –32 mA	2*					2		
V _{OL}		V _{CC} = 4.5 V	I _{OL} = 48 mA	0.55			0.55				V
			I _{OL} = 64 mA	0.55*					0.55		
V _{hys}				100							mV
I _I	Control inputs	V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND		±1			±1		±1		μA
	A or B ports	V _{CC} = 2.1 V to 5.5 V, V _I = V _{CC} or GND		±20			±20		±20		
I _{OZPU} ‡		V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, OE = X		±50			±50		±50		μA
I _{OZPD} ‡		V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, OE = X		±50			±50		±50		μA
I _{OZH} §		V _{CC} = 2.1 V to 5.5 V, V _O = 2.7 V, OE ≥ 2 V		10			10		10		μA
I _{OZL} §		V _{CC} = 2.1 V to 5.5 V, V _O = 0.5 V, OE ≥ 2 V		–10			–10		–10		μA
I _{off}		V _{CC} = 0, V _I or V _O ≤ 4.5 V		±100					±100		μA
I _{CEX}		V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high	50			50		50		μA
I _O ¶		V _{CC} = 5.5 V, V _O = 2.5 V		–50	–100	–200	–50	–200	–50	–200	mA
I _{CC}		V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high	250			250		250		μA
			Outputs low	40			40		40		mA
			Outputs disabled	250			250		250		μA
ΔI _{CC} #	Data inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND	Outputs enabled	1.5			1.5		1.5		mA
			Outputs disabled	0.25			0.25		0.25		
	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND		1.5			1.5		1.5		
C _i	Control inputs	V _I = 2.5 V or 0.5 V		4							pF
C _{i0}	A or B ports	V _O = 2.5 V or 0.5 V		10							pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ This parameter is characterized, but not production tested.

§ The parameters I_{OZH} and I_{OZL} include the input leakage current.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$			SN54ABT657A		SN74ABT657A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	3.2	4.2	1	5	1	4.6	ns
t_{PHL}			1	2.8	3.8	1	4.5	1	4.3	
t_{PLH}	A	PARITY	1.8	4.8	6.3	1.8	8.5	1.8	8.1	ns
t_{PHL}			2.3	4.9	6.4	2.3	8.1	2.3	7.7	
t_{PLH}	ODD/ $\overline{\text{EVEN}}$	PARITY, $\overline{\text{ERR}}$	1.1	3.3	4.2	1.1	5.3	1.1	4.9	ns
t_{PHL}			1.3	3.4	4.5	1.3	5.1	1.3	4.9	
t_{PLH}	B	$\overline{\text{ERR}}$	1.6	4.7	6.5	1.6	8.4	1.6	7.9	ns
t_{PHL}			2.1	4.9	6.9	2.1	8	2.1	7.8	
t_{PLH}	PARITY	$\overline{\text{ERR}}$	2	4.8	6.3	2	8.1	2	7.7	ns
t_{PHL}			2.1	4.9	6.7	2.1	8	2.1	7.5	
t_{PZH}	$\overline{\text{OE}}$	A, B, PARITY	1.4	4	5.4	1.4	6.8	1.4	6.5	ns
t_{PZL}			1.7	4.1	5.8	1.7	6.7	1.7	6.5	
t_{PZH}	$\overline{\text{OE}}$	$\overline{\text{ERR}}$	1.8	4.1	5.4	1.8	6.9	1.8	6.6	ns
t_{PZL}			3.3	6.2	7.6	3.3	9.7	3.3	9.2	
t_{PHZ}	$\overline{\text{OE}}$	A, B, PARITY, or $\overline{\text{ERR}}$	2.4	4.2	5.6	2.4	6.3	2.4	6.2	ns
t_{PLZ}			1.8	4.2	6.2	1.8	8.9	1.8	7.8	

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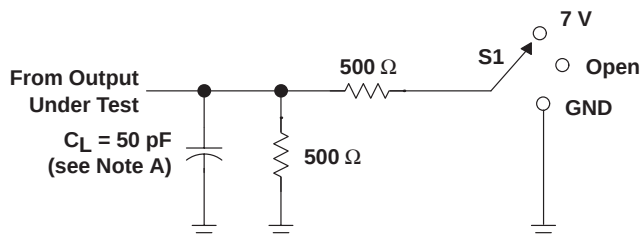


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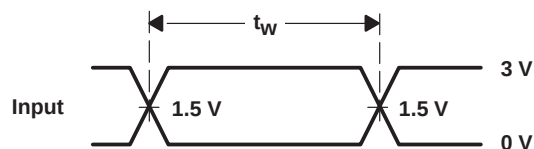
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PARAMETER MEASUREMENT INFORMATION

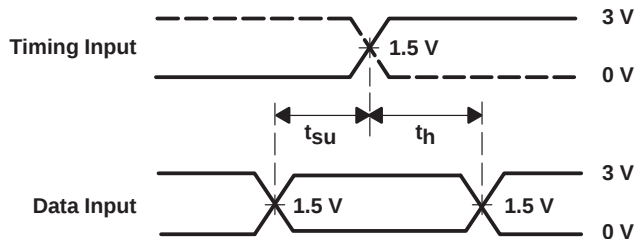


LOAD CIRCUIT

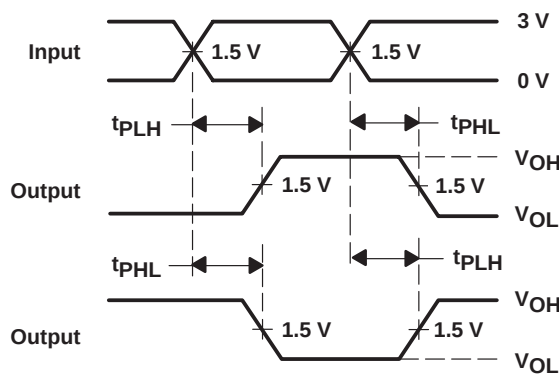
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



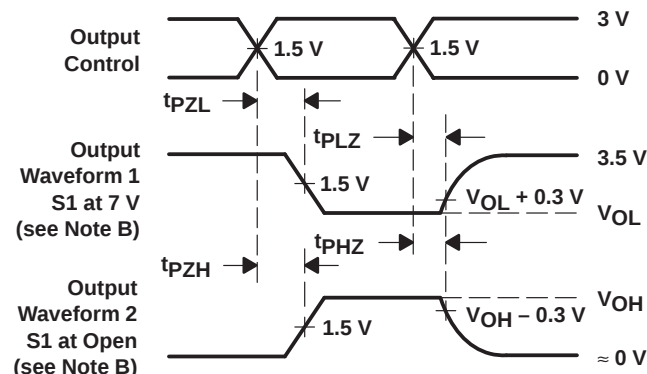
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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