- **State-of-the-Art *EPIC-*II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**

- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**

- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**

- **High-Drive Outputs (−32-mA I_{OH}, 64-mA I_{OL})**

- **Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK), and Plastic (N) and Ceramic (J) DIPs**

SN54ABT241 . . . J PACKAGE
SN74ABT241 . . . DB, DW, OR N PACKAGE
(TOP VIEW)

1$\overline{OE}$	1	20	V_{CC}
1A1	2	19	2OE
2Y4	3	18	1Y1
1A2	4	17	2A4
2Y3	5	16	1Y2
1A3	6	15	2A3
2Y2	7	14	1Y3
1A4	8	13	2A2
2Y1	9	12	1Y4
GND	10	11	2A1

SN54ABT241 . . . FK PACKAGE
(TOP VIEW)

Top pins: 2Y4, 1A1, 1$\overline{OE}$, V_{CC}, 2OE (pins 3, 2, 1, 20, 19)

1A2 4	18 1Y1
2Y3 5	17 2A4
1A3 6	16 1Y2
2Y2 7	15 2A3
1A4 8	14 1Y3

Bottom pins: 2Y1, GND, 2A1, 1Y4, 2A2 (pins 9, 10, 11, 12, 13)

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the ′ABT240 and ′ABT244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable ($\overline{OE}$) inputs, and complementary OE and $\overline{OE}$ inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74ABT241 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54ABT241 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ABT241 is characterized for operation from −40°C to 85°C.

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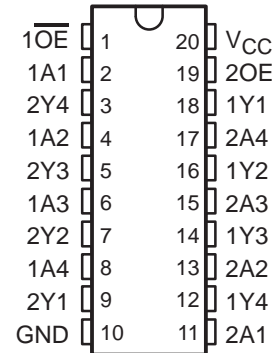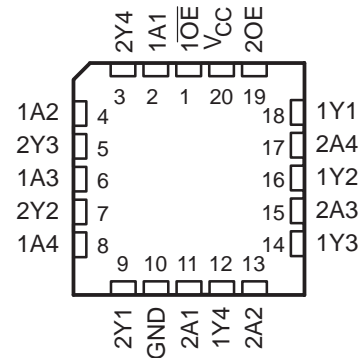
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SN54ABT241, SN74ABT241
OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

SCBS184A – JANUARY 1991 – REVISED JULY 1994

FUNCTION TABLES

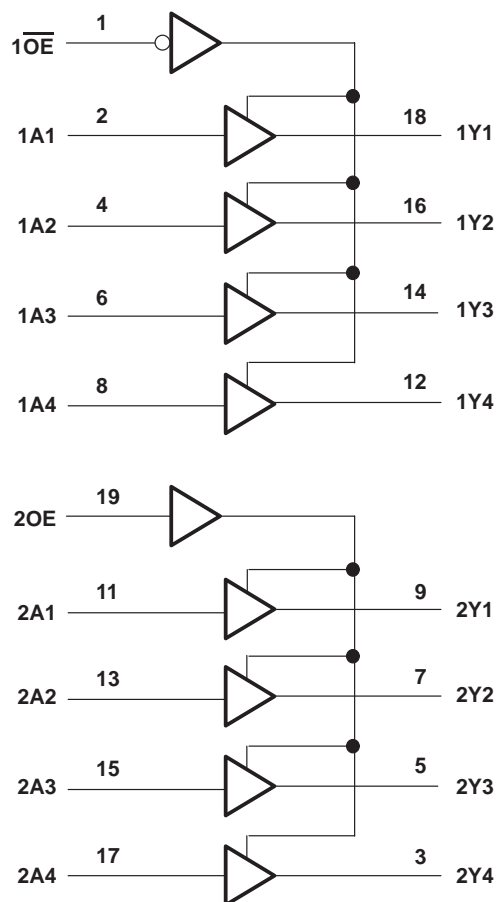| INPUTS		OUTPUT
1$\overline{\text{OE}}$	1A	1Y
L	H	H
L	L	L
H	X	Z

INPUTS		OUTPUT
2OE	2A	2Y
H	H	H
H	L	L
L	X	Z

logic symbol†

logic diagram (positive logic)
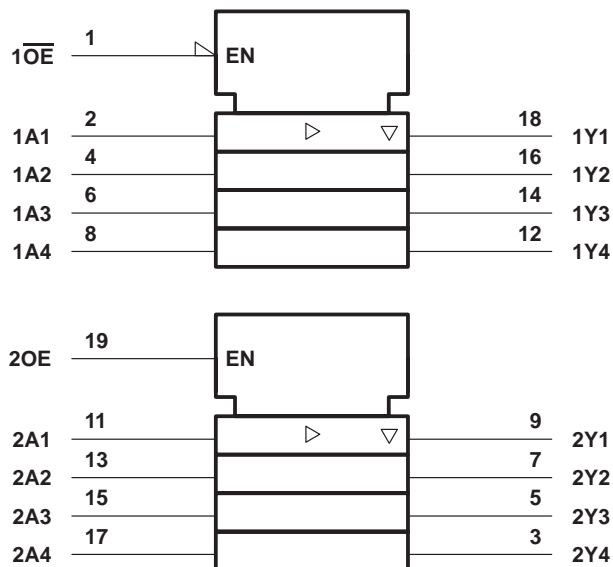
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O .... −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT241 .... 96 mA
SN74ABT241 .... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) .... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) .... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DB package .... 0.6 W
DW package .... 1.6 W
N package .... 1.3 W
Storage temperature range .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
   functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
   implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
        2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils,
            except for the N package, which has a trace length of zero. For more information, refer to the *Package Thermal Considerations*
            application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 3)

			SN54ABT241		SN74ABT241		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3:   Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			$T_A = 25°C$			SN54ABT241		SN74ABT241		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	$V_{CC} = 4.5$ V,	$I_I = -18$ mA				−1.2		−1.2		−1.2	V
V_{OH}	$V_{CC} = 4.5$ V,	$I_{OH} = -3$ mA		2.5			2.5		2.5		V
	$V_{CC} = 5$ V,	$I_{OH} = -3$ mA		3			3		3		
	$V_{CC} = 4.5$ V	$I_{OH} = -24$ mA		2			2				
		$I_{OH} = -32$ mA		2*					2		
V_{OL}	$V_{CC} = 4.5$ V	$I_{OL} = 48$ mA				0.55		0.55			V
		$I_{OL} = 64$ mA				0.55*				0.55	
I_I	$V_{CC} = 5.5$ V,	$V_I = V_{CC}$ or GND				±1		±1		±1	µA
I_{OZH}	$V_{CC} = 5.5$ V,	$V_O = 2.7$ V				50		10		50	µA
I_{OZL}	$V_{CC} = 5.5$ V,	$V_O = 0.5$ V				−50		−10		−50	µA
I_{off}	$V_{CC} = 0$,	V_I or $V_O \le 4.5$ V				±100				±100	µA
I_{CEX}	$V_{CC} = 5.5$ V,	$V_O = 5.5$ V	Outputs high			50		50		50	µA
$I_O‡$	$V_{CC} = 5.5$ V,	$V_O = 2.5$ V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	$V_{CC} = 5.5$ V, $V_I = V_{CC}$ or GND	$I_O = 0$,	Outputs high		1	250		250		250	µA
			Outputs low		24	30		30		30	mA
			Outputs disabled		0.5	250		250		250	µA
$\Delta I_{CC}§$	$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND	Data inputs	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			0.05		0.05		0.05	
		Control inputs				1.5		1.5		1.5	
C_i	$V_I = 2.5$ V or 0.5 V				3						pF
C_o	$V_O = 2.5$ V or 0.5 V				8						pF

* On products compliant to MIL-STD-883, Class B, this parameter does not apply.
† All typical values are at $V_{CC} = 5$ V.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT241		SN74ABT241		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.6	4.1	0.8	5.3	1	4.6	ns
t_{PHL}			1	2.9	4.2	0.8	5	1	4.6	
t_{PZH}	$\overline{OE}$ or OE	Y	1.1	4.8	6.3	1	7	1.1	6.8	ns
t_{PZL}			1.3	4.3	5.8	1	7	1.3	6.8	
t_{PHZ}	$\overline{OE}$ or OE	Y	1.6	4.6	6.1	0.8	7.9	1.6	7.1	ns
t_{PLZ}			1	3.9	5.4	0.8	6.2	1	5.9	

PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT FOR OUTPUTS

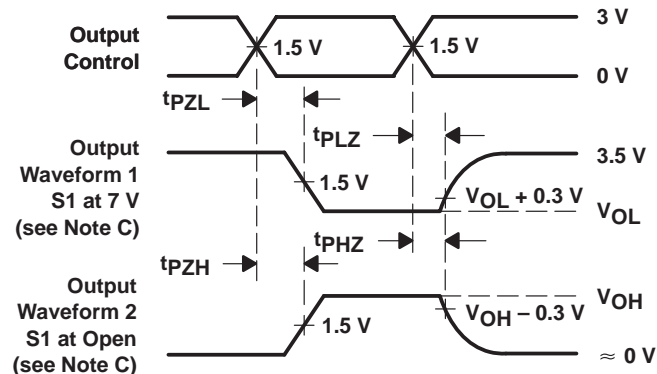| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open
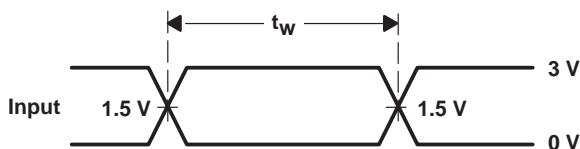
VOLTAGE WAVEFORMS
PULSE DURATION
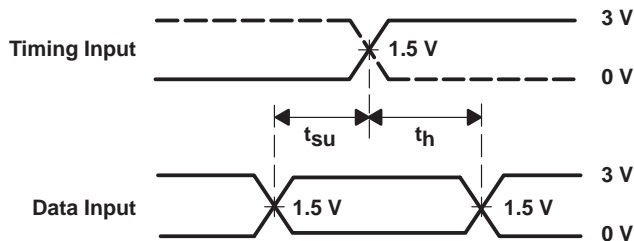
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
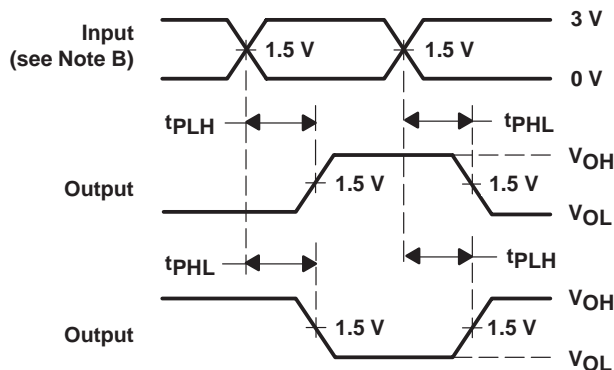
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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