

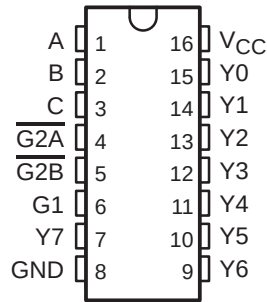
SN74LVC137A

3-LINE TO 8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCHES

SCAS340E – MARCH 1994 – REVISED JUNE 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This 3-line to 8-line decoder/demultiplexer with latches on three address inputs is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC137A is designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

When the latch-enable ($\overline{G2A}$) input is low, the SN74LVC137A acts as a decoder/demultiplexer. When $\overline{G2A}$ transitions from low to high, the address present at the inputs (A, B, and C) is stored in the latches. Further address changes are ignored, provided $\overline{G2A}$ remains high. The output-enable (G1 and $\overline{G2B}$) inputs control the outputs independently of the select or latch-enable inputs. All of the outputs are forced high if G1 is low or $\overline{G2B}$ is high.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC137A is characterized for operation from -40°C to 85°C .

PRODUCT PREVIEW



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**TEXAS
INSTRUMENTS**

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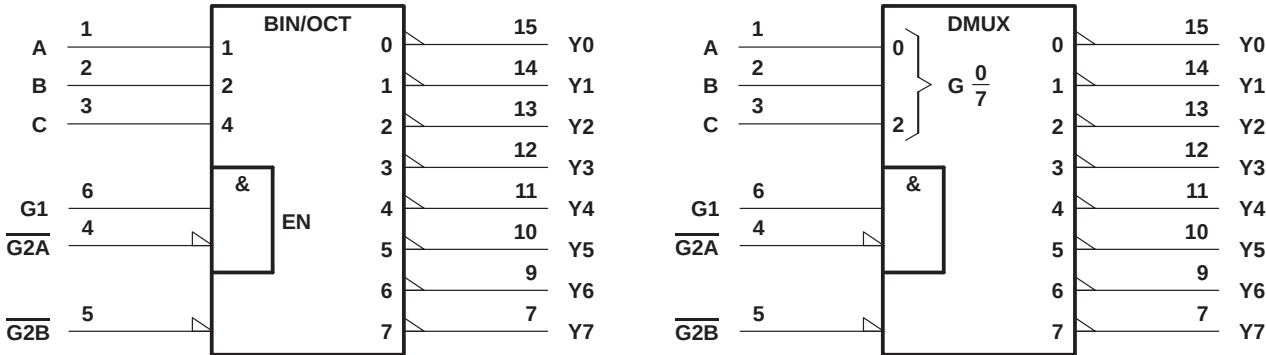
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SCAS340E – MARCH 1994 – REVISED JUNE 1998

FUNCTION TABLE

INPUTS						OUTPUTS							
LATCH ENABLE	OUTPUT ENABLE		SELECT										
$\overline{G2A}$	G1	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Outputs corresponding to stored address = L; all other outputs = H							

logic symbols (alternatives)[†]



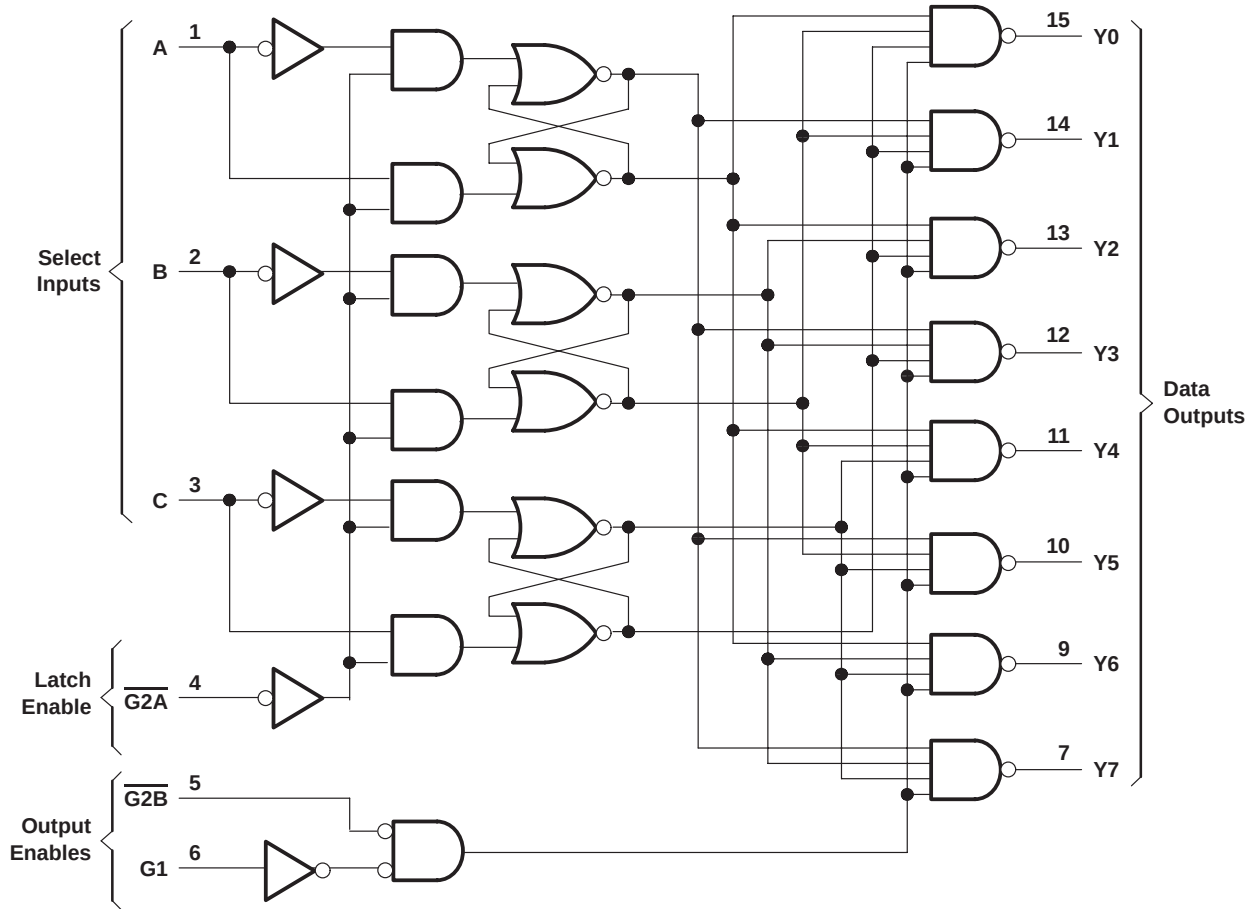
[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74LVC137A

3-LINE TO 8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCHES

SCAS340E – MARCH 1994 – REVISED JUNE 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	113°C/W
DB package	131°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51.



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PRODUCT PREVIEW

SN74LVC137A

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SCAS340E – MARCH 1994 – REVISED JUNE 1998

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	V
	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
V_I Input voltage		0	5.5	V
V_O Output voltage		0	V_{CC}	V
I_{OH} High-level output current	$V_{CC} = 1.65 \text{ V}$		–4	mA
	$V_{CC} = 2.3 \text{ V}$		–8	
	$V_{CC} = 2.7 \text{ V}$		–12	
	$V_{CC} = 3 \text{ V}$		–24	
I_{OL} Low-level output current	$V_{CC} = 1.65 \text{ V}$		4	mA
	$V_{CC} = 2.3 \text{ V}$		8	
	$V_{CC} = 2.7 \text{ V}$		12	
	$V_{CC} = 3 \text{ V}$		24	
$\Delta t/\Delta v$ Input transition rise or fall rate		0	10	ns/V
T_A Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}	$I_{OH} = -100 \mu\text{A}$	1.65 V to 3.6 V	$V_{CC}-0.2$			V
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
	$I_{OH} = -8 \text{ mA}$	2.3 V	1.7			
	$I_{OH} = -12 \text{ mA}$	2.7 V	2.2			
		3 V	2.4			
	$I_{OH} = -24 \text{ mA}$	3 V	2.2			
V_{OL}	$I_{OL} = 100 \mu\text{A}$	1.65 V to 3.6 V			0.2	V
	$I_{OL} = 4 \text{ mA}$	1.65 V			0.45	
	$I_{OL} = 8 \text{ mA}$	2.3 V			0.7	
	$I_{OL} = 12 \text{ mA}$	2.7 V			0.4	
	$I_{OL} = 24 \text{ mA}$	3 V			0.55	
I_I	$V_I = 5.5 \text{ V or GND}$	3.6 V			± 5	μA
I_{CC}	$V_I = V_{CC} \text{ or GND, } I_O = 0$	3.6 V			10	μA
ΔI_{CC}	One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at $V_{CC} \text{ or GND}$	2.7 V to 3.6 V			500	μA
C_i	$V_I = V_{CC} \text{ or GND}$	3.3 V				pF
C_o	$V_O = V_{CC} \text{ or GND}$	3.3 V				pF

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.



SN74LVC137A
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SCAS340E – MARCH 1994 – REVISED JUNE 1998

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B or C	Y									ns
	$\overline{G2A}$ or $\overline{G2B}$										
	G1										
$t_{sk(o)}^\dagger$											ns

[†] Skew between any two outputs of the same package switching in the same direction

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	UNIT
			TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	$f = 10\text{ MHz}$				pF

PRODUCT PREVIEW



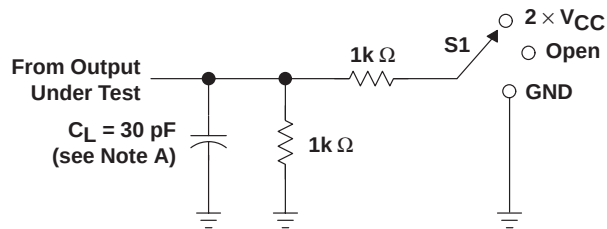
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SCAS340E – MARCH 1994 – REVISED JUNE 1998

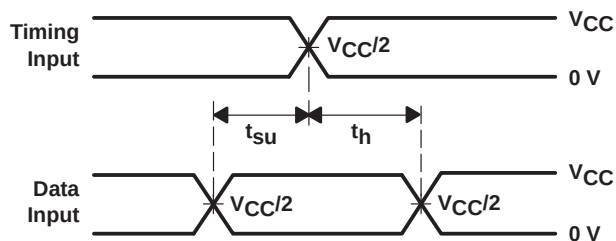
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

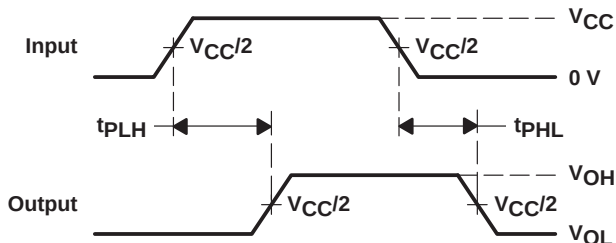


LOAD CIRCUIT

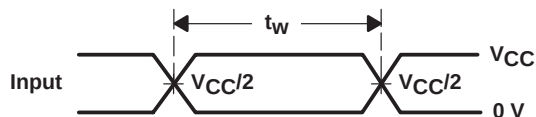
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PHZ}	Open



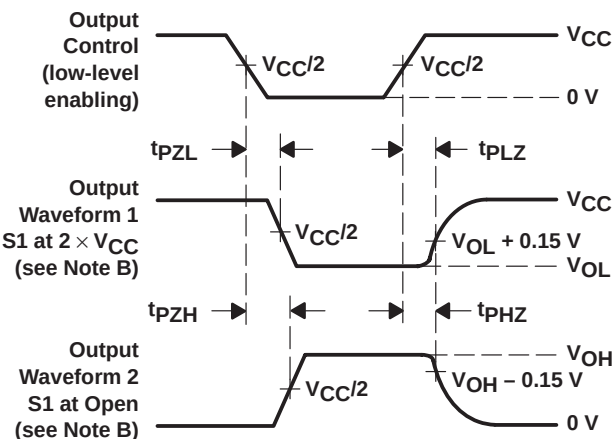
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

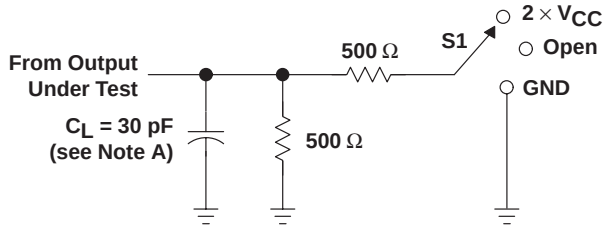
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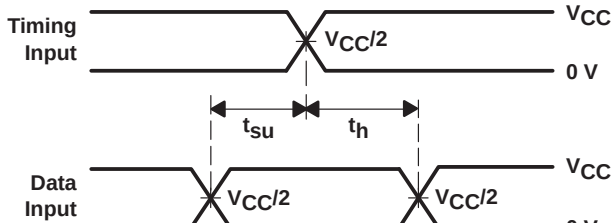
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

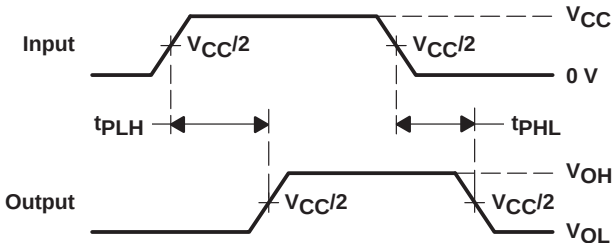


LOAD CIRCUIT

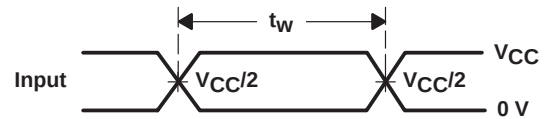
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



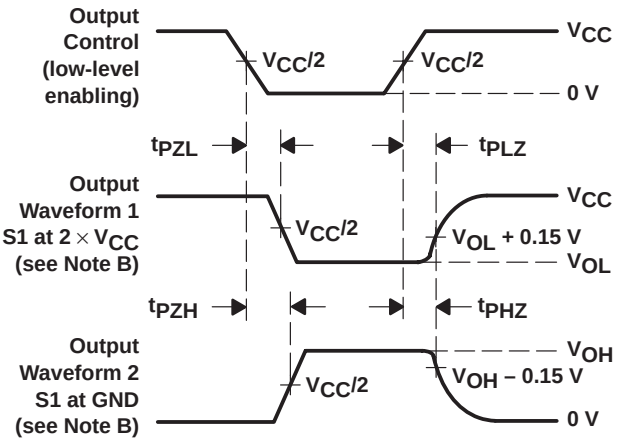
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 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

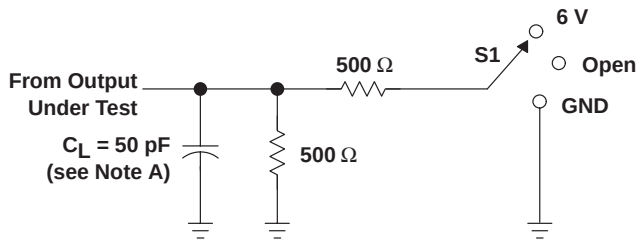
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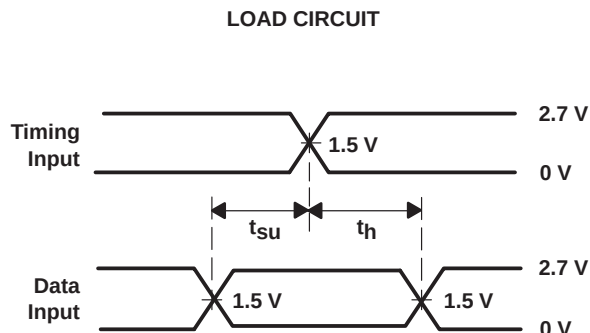
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V} \pm 0.3 \text{ V}$

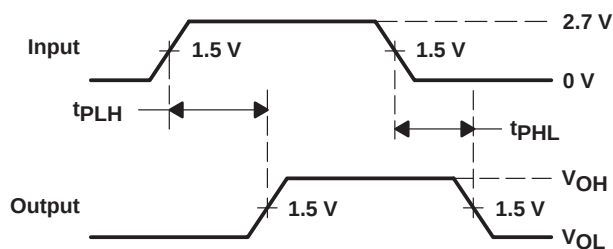


LOAD CIRCUIT

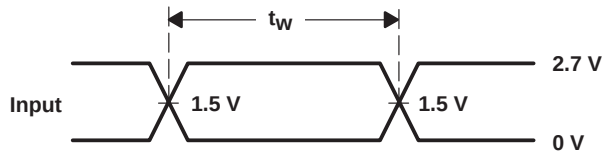
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



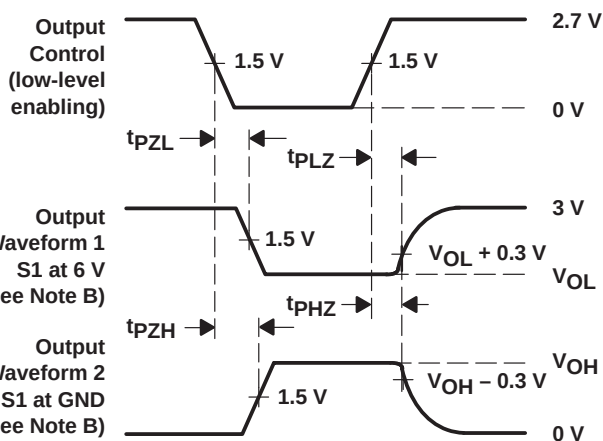
VOLTAGE WAVEFORMS
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PROPAGATION DELAY TIMES



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PULSE DURATION



VOLTAGE WAVEFORMS
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 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

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