S25FL Family (Serial Peripheral Interface)

64 Megabit CMOS 3.0 Volt Flash Memory with 50 Mhz SPI Bus Interface

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S25FL Family (Serial Peripheral Interface)
S25FL064A

64 Megabit CMOS 3.0 Volt Flash Memory with 50 Mhz SPI Bus Interface

Data Sheet

ADVANCE INFORMATION

Distinctive Characteristics

Architectural Advantages

- **Single power supply operation**
  - Full voltage range: 2.7 to 3.6 V read and program operations
- **Memory Architecture**
  - 128 sectors with 512 Kb each
- **Program**
  - Page Program (up to 256 bytes) in 1.5 ms (typical)
  - Program cycles are on a page by page basis
- **Erase**
  - 1.5 s typical sector erase time
  - Bulk Erase
- **Cycling Endurance**
  - 100,000 cycles per sector typical
- **Data Retention**
  - 20 years typical
- **Device ID**
  - JEDEC standard two-byte electronic signature
  - RES instruction one-byte electronic signature for backward compatibility
- **Process Technology**
  - Manufactured on 0.20 µm MirrorBit™ process technology
- **Package Option**
  - Industry Standard Pinouts
  - 16-pin SO package (300 mils)

Performance Characteristics

- **Speed**
  - 50 MHz clock rate (maximum)
- **Power Saving**
  - Standby Mode 50 µA (max)
  - Deep Power Down Mode 1 µA (typical)

Memory Protection Features

- **Memory Protection**
  - W# pin works in conjunction with Status Register Bits to protect specified memory areas
  - Status Register Block Protection bits (BP2, BP1, BP0) in status register configure parts of memory as read-only

Software Features

- **SPI Bus Compatible Serial Interface**

General Description

The S25FL064A device is a 3.0 Volt (2.7 V to 3.6 V) single power supply Flash memory device. S25FL064A consists of 128 sectors, each with 512 Kb memory.

Data appears on SI input pin when inputting data into the memory and on the SO output pin when outputting data from the memory. The devices are designed to be programmed in-system with the standard system 3.0 Volt V_{CC} supply.

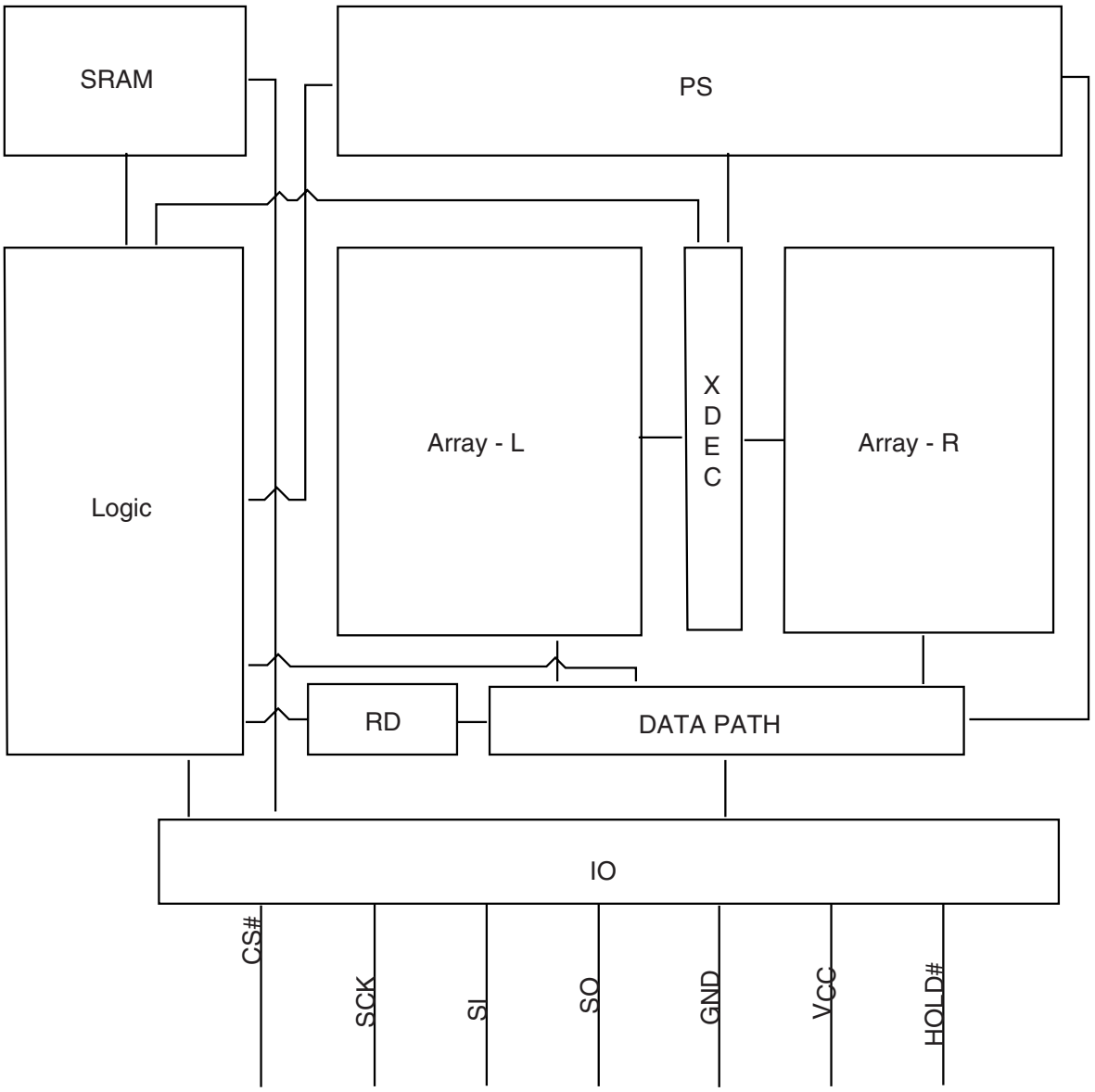
The memory can be programmed 1 to 256 bytes at a time, using the Page Program instruction.

The memory supports Sector Erase and Bulk Erase instructions.

Each device requires only a 3.0 Volt power supply (2.7 V to 3.6 V) for both read and write functions. Internally generated and regulated voltages are provided for the program operations. This device does not require V_{PP} supply.

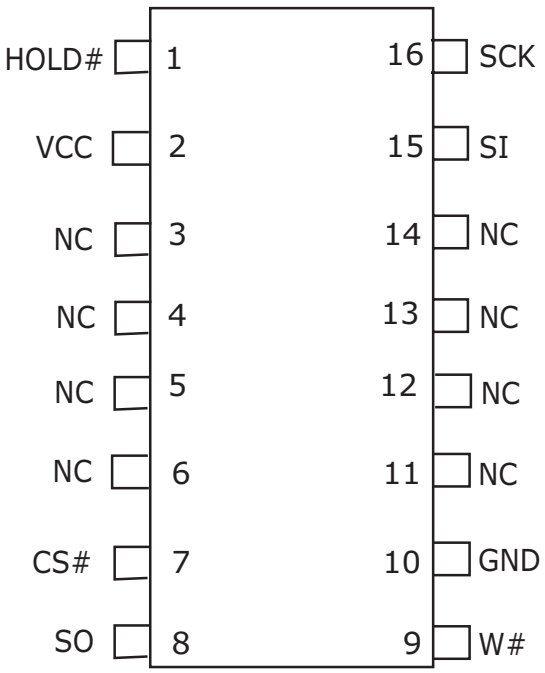
Table of Contents

Block Diagram



Connection Diagrams

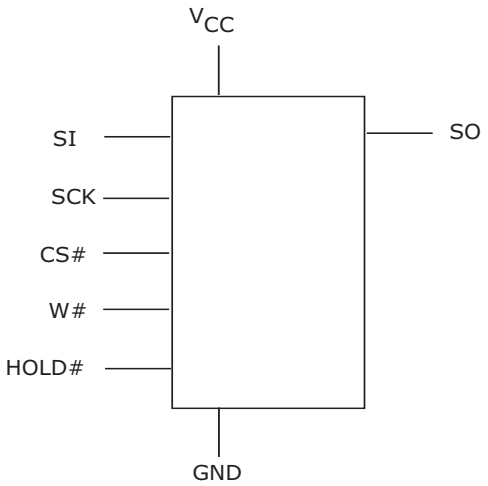
16-pin Plastic Small Outline Package (SO)



Input/Output Descriptions

SCK	=	Serial Clock Input
SI	=	Serial Data Input
SO	=	Serial Data Output
CS#	=	Chip Select Input
W#	=	Write Protect Input
HOLD#	=	Hold Input
V_{CC}	=	Supply Voltage Input
GND	=	Ground Input

Logic Symbol



Ordering Information

The ordering part number is formed by a valid combination of the following:

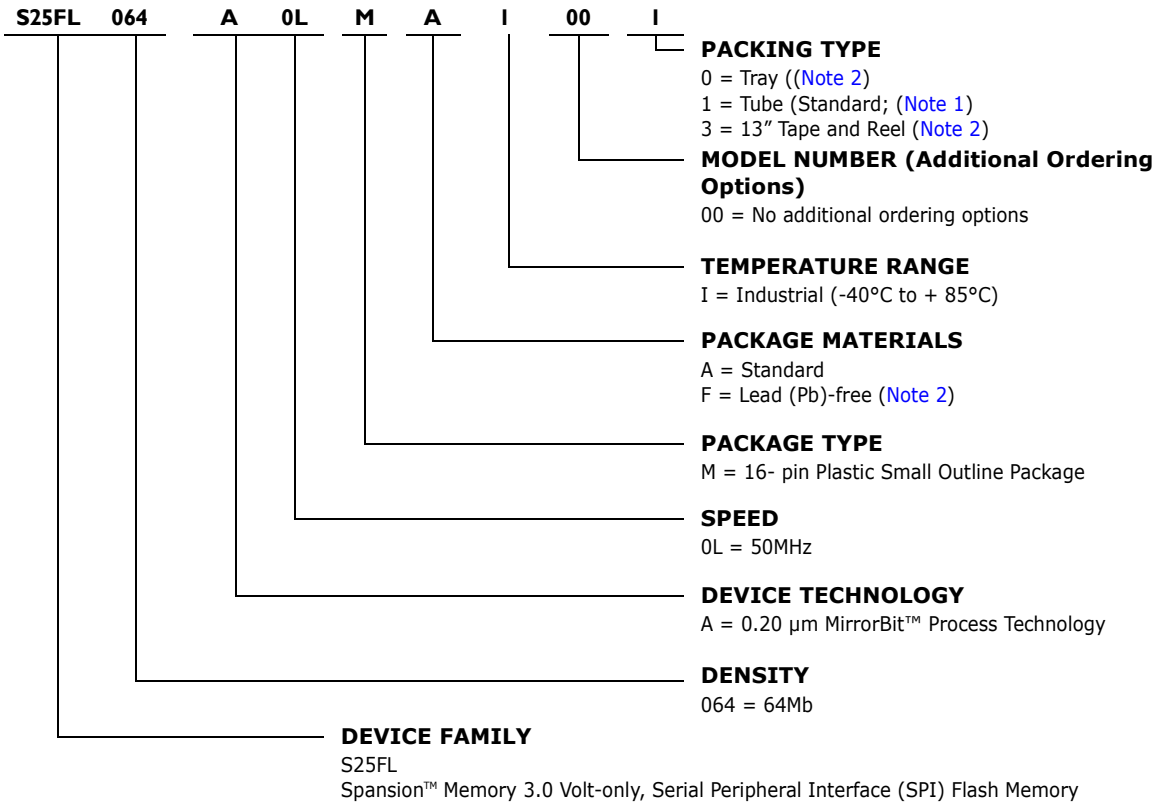


Table I. S25FL Valid Combinations Table

S25FL Valid Combinations					Package Marking (Note 3)
Base Ordering Part Number	Speed Option	Package & Temperature	Model Number	Packing Type	
S25FL064A	0L	MAI, MFI NAI, NFI (Note 2)	00	0, 1, 3 (Note 1)	FL064A + (Temp) (Note 4)

Notes:

1. *Type* 1 *is standard. Specify other options as required.*
2. *Contact your local sales office for availability.*
3. *Package marking omits leading* S25 *and speed, package, and leading digit of model number from ordering part number.*
4. A *for standard package (non-Pb free).*
   F *for Pb-free package.*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device.

Signal Description

Signal Data Output (SO): This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (SCK).

Serial Data Input (SI): This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Values are latched on the rising edge of Serial Clock (SCK).

Serial Clock (SCK): This input signal provides the timing of the serial interface. Instructions, addresses, and data present at the Serial Data input (SI) are latched on the rising edge of Serial Clock (SCK). Data on Serial Data Output (SO) changes after the falling edge of Serial Clock (SCK).

Chip Select (CS#): When this input signal is High, the device is deselected and Serial Data Output (SO) is at high impedance. Unless an internal Program, Erase or Write Status Register cycle is in progress, the device is in Standby mode. Driving Chip Select (CS#) Low enables the device, placing it in the active power mode.

After Power-up, a falling edge on Chip Select (CS#) is required prior to the start of any instruction.

Hold (HOLD#): The Hold (HOLD#) signal is used to pause any serial communications with the device without deselecting the device.

During the Hold instruction, the Serial Data Output (SO) is high impedance, and Serial Data Input (SI) and Serial Clock (SCK) are Don't Care.

To start the Hold condition, the device must be selected, with Chip Select (CS#) driven Low.

Write Protect (W#): The main purpose of this input signal is to freeze the size of the area of memory that is protected against program or erase instructions (as specified by the values in the BP1 and BP0 bits of the Status Register).

SPI Modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

- CPOL = 0, CPHA = 0
- CPOL = 1, CPHA = 1

For these two modes, input data is latched in on the rising edge of Serial Clock (SCK), and output data is available from the falling edge of Serial Clock (SCK).

The difference between the two modes, as shown in Figure 2, on page 9 is the clock polarity when the bus master is in Standby and not transferring data:

- SCK remains at 0 for (CPOL = 0, CPHA = 0)
- SCK remains at 1 for (CPOL = 1, CPHA = 1)

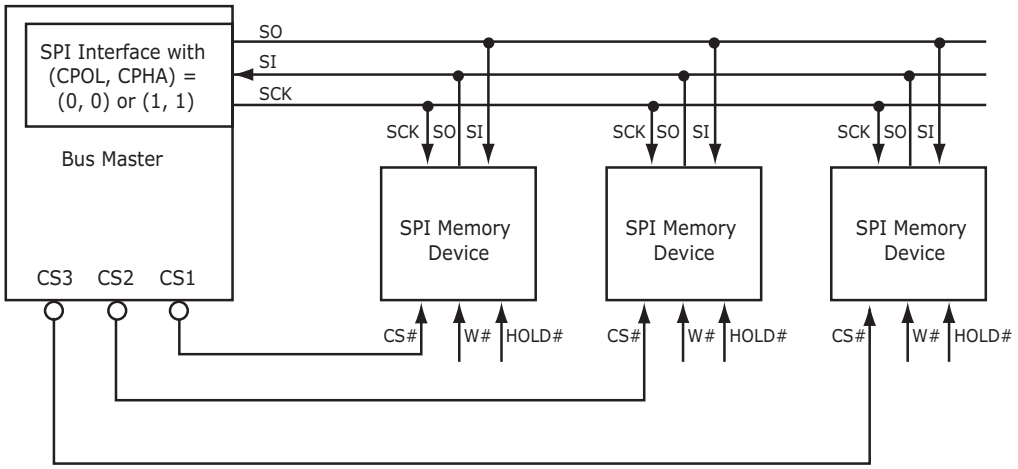


Figure I. Bus Master and Memory Devices on the SPI Bus

Note: *The Write Protect (W#) and Hold (HOLD#) signals should be driven, High or Low as appropriate.*

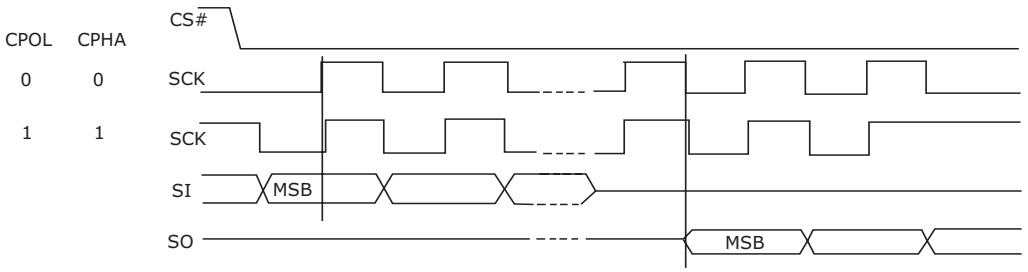


Figure 2. SPI Modes Supported

Operating Features

All data into and out of the device is shifted in 8-bit chunks.

Page Programming

To program one data byte, two instructions are required: Write Enable (WREN), which is one byte, and a Page Program (PP) sequence, which consists of four bytes plus data. This is followed by the internal Program cycle. To spread this overhead, the Page Program (PP) instruction allows up to 256 bytes to be programmed at a time (changing bits from 1 to 0), provided that they lie in consecutive addresses on the same page of memory.

Sector Erase, or Bulk Erase

The Page Program (PP) instruction allows bits to be programmed from 1 to 0. Before this can be applied, the bytes of the memory need to be first erased to all 1's (FFh) before any programming. This can be achieved in two ways: 1) a sector at a time using the Sector Erase (SE) instruction, or 2) throughout the entire memory, using the Bulk Erase (BE) instruction.

Polling During a Write, Program, or Erase Cycle

A further improvement in the time to Write Status Register (WRSR), Program (PP) or Erase (SE or BE) can be achieved by not waiting for the worst-case delay. The Write in Progress (WIP) bit is provided in the Status Register so that the application program can monitor its value, polling it to establish when the previous Write cycle, Program cycle, or Erase cycle is complete.

Active Power and Standby Power Modes

When Chip Select (CS#) is Low, the device is enabled, and in the Active Power mode. When Chip Select (CS#) is High, the device is disabled, but could remain in the Active Power mode until all internal cycles have completed (Program, Erase, Write Status Register). The device then goes into the Standby Power mode. The device consumption drops to I_{SB}. This can be used as an extra Deep Power Down on mechanism, when the device is not in active use, to protect the device from inadvertent Write, Program, or Erase instructions.

Status Register

The Status Register contains a number of status and control bits, as shown in Figure 7, on page 19 that can be read or set (as appropriate) by specific instructions

- **WIP bit:** The Write In Progress (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle.
- **WEL bit:** The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch.
- **BP2, BP1, BP0 bits:** The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions.
- **SRWD bit:** The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect (W#) signal. The Status Register Write Disable (SRWD) bit and Write Protect (W#) signal allow the device to be put in the Hardware Protected mode. In this mode, the non-volatile bits of the Status Register (SRWD, BP2, BP1, BP0) become read-only bits.

Protection Modes

The SPI memory device boasts the following data protection mechanisms:

- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit. This bit is returned to its reset state by the following events:
  - Power-up
  - Write Disable (WRDI) instruction completion
  - Write Status Register (WRSR) instruction completion
  - Page Program (PP) instruction completion
  - Sector Erase (SE) instruction completion
  - Bulk Erase (BE) instruction completion
- The Block Protect (BP2, BP1, BP0) bits allow part of the memory to be configured as read-only. This is the Software Protected Mode (SPM).
- The Write Protect (W#) signal works in cooperation with the Status Register Write Disable (SRWD) bit to enable write-protection. This is the Hardware Protected Mode (HPM).
- Program, Erase and Write Status Register instructions are checked to verify that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.

Table 2. Protected Area Sizes (S25FL064A).

Protected Area	Status Register Contents			Memory Content	
	BP2	BP1	BP0	Protected Area	Unprotected Area
None	0	0	0	None	000000h-7FFFFFh
Upper 64th (2 sectors)	0	0	1	7E0000h-7FFFFFh	000000h-7DFFFFh
Upper 32nd (4 sectors)	0	1	0	7C0000h-7FFFFFh	000000h-7BFFFFh
Upper sixteenth (8 sectors)	0	1	1	780000h-7FFFFFh	000000h-77FFFFh
Upper eighth (16 sectors)	1	0	0	700000h-7FFFFFh	000000h-6FFFFFh
Upper quarter (32 sectors)	1	0	1	600000h-7FFFFFh	000000h-5FFFFFh
Upper half (64 sectors)	1	1	0	400000h-7FFFFFh	000000h-3FFFFFh
All (128 sectors)	1	1	1	000000h-7FFFFFh	None

Hold Condition Modes

The Hold (HOLD#) signal is used to pause any serial communications with the device without resetting the clocking sequence. Hold (HOLD#) signal gates the clock input to the device. However, taking this signal Low does not terminate any Write Status Register, Program or Erase Cycle that is currently in progress.

To enter the Hold condition, the device must be selected, with Chip Select (CS#) Low. The Hold condition starts on the falling edge of the Hold (HOLD#) signal, provided that this coincides with Serial Clock (SCK) being Low (as shown in Figure 3, on page 12).

The Hold condition ends on the rising edge of the Hold (HOLD#) signal, provided that this coincides with Serial Clock (SCK) being Low.

If the falling edge does not coincide with Serial Clock (SCK) being Low, the Hold condition starts after Serial Clock (SCK) next goes Low. Similarly, if the rising edge does not coincide with Serial Clock (SCK) being Low, the Hold condition ends after Serial Clock (SCK) next goes Low (Figure 3). During the Hold condition, the Serial Data Output (SO) is high impedance, and Serial Data Input (SI) and Serial Clock (SCK) are Don't Care.

Normally, the device remains selected, with Chip Select (CS#) driven Low, for the entire duration of the Hold condition. This ensures that the state of the internal logic remains unchanged from the moment of entering the Hold condition.

If Chip Select (CS#) goes High while the device is in the Hold condition, this has the effect of resetting the internal logic of the device. To restart communication with the device, it is necessary to drive Hold (HOLD#) High, and then to drive Chip Select (CS#) Low. This prevents the device from going back to the Hold condition.

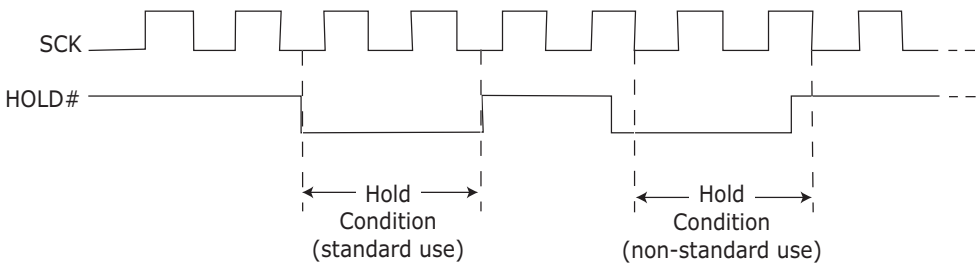


Figure 3. Hold Condition Activation

Memory Organization

The memory is organized as:

- S25FL064A: 128 sectors of 512 Kbit each
- Each page can be individually programmed (bits are programmed from 1 to 0).
- The device is Sector or Bulk erasable (bits are erased from 0 to 1).

Table 3. Sector Address Table - S25FL064A (Sheet I of 3)

Sector	Address Range	
SA127	7F0000h	7FFFFFh
SA126	7E0000h	7EFFFFh
SA125	7D0000h	7DFFFFh
SA124	7C0000h	7CFFFFh
SA123	7B0000h	7BFFFFh
SA122	7A0000h	7AFFFFh
SA121	790000h	79FFFFh
SA120	780000h	78FFFFh
SA119	770000h	77FFFFh
SA118	760000h	76FFFFh
SA117	750000h	75FFFFh
SA116	740000h	74FFFFh
SA115	730000h	73FFFFh
SA114	720000h	72FFFFh
SA113	710000h	71FFFFh
SA112	700000h	70FFFFh
SA111	6F0000h	6FFFFFh
SA110	6E0000h	6EFFFFh
SA109	6D0000h	6DFFFFh
SA108	6C0000h	6CFFFFh
SA107	6B0000h	6BFFFFh
SA106	6A0000h	6AFFFFh
SA105	690000h	69FFFFh
SA104	680000h	68FFFFh
SA103	670000h	67FFFFh
SA102	660000h	66FFFFh
SA101	650000h	65FFFFh
SA100	640000h	64FFFFh
SA99	630000h	63FFFFh
SA98	620000h	62FFFFh
SA97	610000h	61FFFFh
SA96	600000h	60FFFFh
SA95	5F0000h	5FFFFFh
SA94	5E0000h	5EFFFFh
SA93	5D0000h	5DFFFFh
SA92	5C0000h	5CFFFFh
SA91	5B0000h	5BFFFFh

Table 3. Sector Address Table - S25FL064A (Sheet 2 of 3)

SA90	5A0000h	5AFFFFh
SA89	590000h	59FFFFh
SA88	580000h	58FFFFh
SA87	570000h	57FFFFh
SA86	560000h	56FFFFh
SA85	550000h	55FFFFh
SA84	540000h	54FFFFh
SA83	530000h	53FFFFh
SA82	520000h	52FFFFh
SA81	510000h	51FFFFh
SA80	500000h	50FFFFh
SA79	4F0000h	4FFFFFh
SA78	4E0000h	4EFFFFh
SA77	4D0000h	4DFFFFh
SA76	4C0000h	4CFFFFh
SA75	4B0000h	4BFFFFh
SA74	4A0000h	4AFFFFh
SA73	490000h	49FFFFh
SA72	480000h	48FFFFh
SA71	470000h	47FFFFh
SA70	460000h	46FFFFh
SA69	450000h	45FFFFh
SA68	440000h	44FFFFh
SA67	430000h	43FFFFh
SA66	420000h	42FFFFh
SA65	410000h	41FFFFh
SA64	400000h	40FFFFh
SA63	3F0000h	3FFFFFh
SA62	3E0000h	3EFFFFh
SA61	3D0000h	3DFFFFh
SA60	3C0000h	3CFFFFh
SA59	3B0000h	3BFFFFh
SA58	3A0000h	3AFFFFh
SA57	390000h	39FFFFh
SA56	380000h	38FFFFh
SA55	370000h	37FFFFh
SA54	360000h	36FFFFh
SA53	350000h	35FFFFh
SA52	340000h	34FFFFh
SA51	330000h	33FFFFh
SA50	320000h	32FFFFh
SA49	310000h	31FFFFh
SA48	300000h	30FFFFh
SA47	2F0000h	2FFFFFh
SA46	2E0000h	2EFFFFh
SA45	2D0000h	2DFFFFh

Table 3. Sector Address Table - S25FL064A (Sheet 3 of 3)

SA44	2C0000h	2CFFFFh
SA43	2B0000h	2BFFFFh
SA42	2A0000h	2AFFFFh
SA41	290000h	29FFFFh
SA40	280000h	28FFFFh
SA39	270000h	27FFFFh
SA38	260000h	26FFFFh
SA37	250000h	25FFFFh
SA36	240000h	24FFFFh
SA35	230000h	23FFFFh
SA34	220000h	22FFFFh
SA33	210000h	21FFFFh
SA32	200000h	20FFFFh
SA31	1F0000h	1FFFFFh
SA30	1E0000h	1EFFFFh
SA29	1D0000h	1DFFFFh
SA28	1C0000h	1CFFFFh
SA27	1B0000h	1BFFFFh
SA26	1A0000h	1AFFFFh
SA25	190000h	19FFFFh
SA24	180000h	18FFFFh
SA23	170000h	17FFFFh
SA22	160000h	16FFFFh
SA21	150000h	15FFFFh
SA20	140000h	14FFFFh
SA19	130000h	13FFFFh
SA18	120000h	12FFFFh
SA17	110000h	11FFFFh
SA16	100000h	10FFFFh
SA15	0F0000h	0FFFFFh
SA14	0E0000h	0EFFFFh
SA13	0D0000h	0DFFFFh
SA12	0C0000h	0CFFFFh
SA11	0B0000h	0BFFFFh
SA10	0A0000h	0AFFFFh
SA9	090000h	09FFFFh
SA8	080000h	08FFFFh
SA7	070000h	07FFFFh
SA6	060000h	06FFFFh
SA5	050000h	05FFFFh
SA4	040000h	04FFFFh
SA3	030000h	03FFFFh
SA2	020000h	02FFFFh
SA1	010000h	01FFFFh
SA0	000000h	00FFFFh

Instructions

All instructions, addresses, and data are shifted in and out of the device, starting with the most significant bit. Serial Data Input (SI) is sampled on the first rising edge of Serial Clock (SCK) after Chip Select (CS#) is driven Low. Then, the one-byte instruction code must be shifted in to the device, most significant bit first, on Serial Data Input (SI), each bit being latched on the rising edges of Serial Clock (SCK). The instruction set is listed in Table 4 on page 17.

Every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none. Chip Select (CS#) must be driven High after the last bit of the instruction sequence is shifted in.

In the case of a Read Data Bytes (READ), Read Status Register (RDSR), Read Data Bytes at higher speed (FAST_READ) and Read Identification (RDID) instructions, the shifted-in instruction sequence is followed by a data-out sequence. Chip Select (CS#) can be driven High after any bit of the data-out sequence is being shifted out to terminate the transaction.

In the case of a Page Program (PP), Sector Erase (SE), Bulk Erase (BE), Write Status Register (WRSR), Write Enable (WREN), or Write Disable (WRDI) instruction, Chip Select (CS#) must be driven High exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is, Chip Select (CS#) must driven High when the number of clock pulses after Chip Select (CS#) being driven Low is an exact multiple of eight.

All attempts to access the memory array during a Write Status Register cycle, Program cycle or Erase cycle are ignored, and the internal Write Status Register cycle, Program cycle or Erase cycle continues unaffected

Table 4. Instruction Set

Instruction	Description	One-Byte Instruction Code	Address Bytes	Dummy Byte	Data Bytes
Status Register Operations					
WREN	Write Enable	06H (0000 0110)	0	0	0
WRDI	Write Disable	04H (0000 0100)	0	0	0
RDSR	Read from Status Register	05H (0000 0101)	0	0	1 to Infinity
WRSR	Write to Status Register	01H (0000 0001)	0	0	1
Read Operations					
READ	Read Data Bytes	03H (0000 0011)	3	0	1 to Infinity
FAST_READ	Read Data Bytes at Higher Speed	0BH (0000 1011)	3	1	1 to Infinity
RDID	Read Identification	9FH (1001 1111)	0	0	1 to 3
Erase Operations					
SE	Sector Erase	D8H (1101 1000)	3	0	0
BE	Bulk (Chip) Erase	C7H (1100 0111)	0	0	0
Program Operations					
PP	Page Program	02H (0000 0010)	3	0	1 to 256
Deep Power Down Savings Mode Operations					
DP	Deep Power Down	B9H (1011 1001)	0	0	0
RES	Release from Deep Power Down	ABH (1010 1011)	0	0	0
	Release from Deep Power Down and Read Electronic Signature	ABH (1010 1011)	0	3	1 to Infinity

Write Enable (WREN)

The Write Enable (WREN) instruction (Figure 4) sets the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Erase (SE or BE) and Write Status Register (WRSR) instruction. The Write Enable (WREN) instruction is entered by driving Chip Select (CS#) Low, sending the instruction code, and then driving Chip Select (CS#) High.

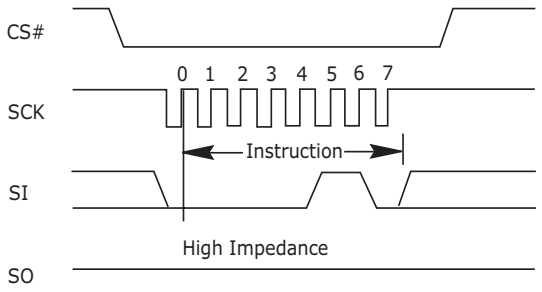


Figure 4. Write Enable (WREN) Instruction Sequence

Write Disable (WRDI)

The Write Disable (WRDI) instruction (Figure 5) resets the Write Enable Latch (WEL) bit. The Write Disable (WRDI) instruction is entered by driving Chip Select (CS#) Low, sending the instruction code, and then driving Chip Select (CS#) High.

The Write Enable Latch (WEL) bit is reset under the following conditions:

- Power-up
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR) instruction completion
- Page Program (PP) instruction completion
- Sector Erase (SE) instruction completion
- Bulk Erase (BE) instruction completion

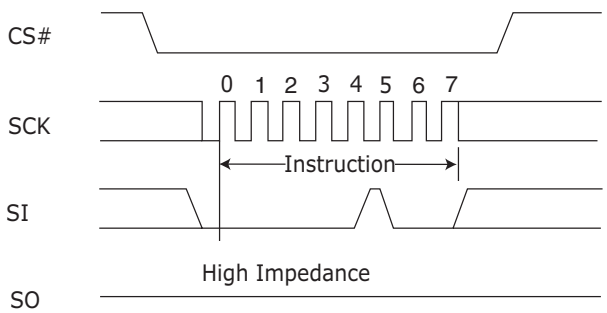


Figure 5. Write Disable (WRDI) Instruction Sequence

Read Status Register (RDSR)

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Program, Erase, or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in Figure 6.

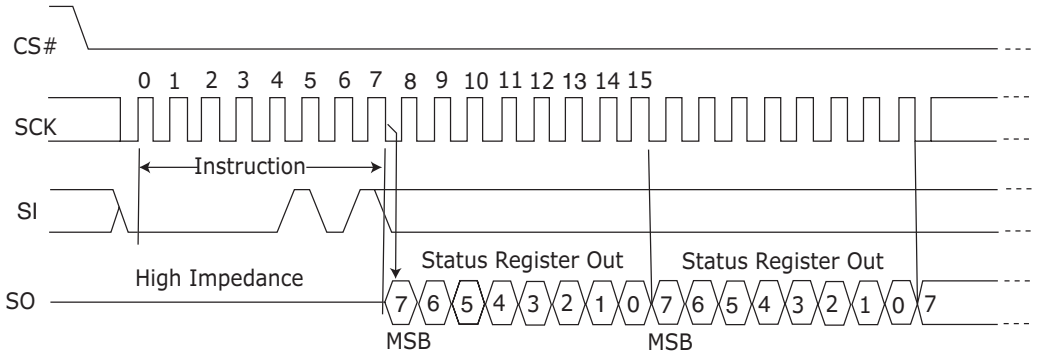


Figure 6. Read Status Register (RDSR) Instruction Sequence

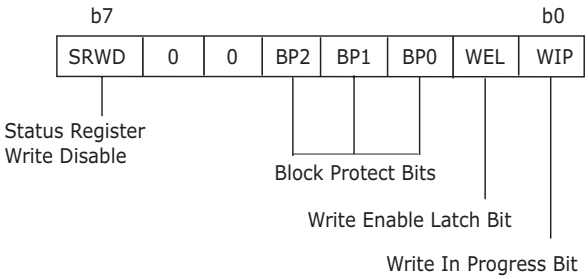


Figure 7. Status Register Format

The status and control bits of the Status Register are as follows:

SRWD bit: The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect (W#) signal. The Status Register Write Disable (SRWD) bit and Write Protect (W#) signal allow the device to be put in the Hardware Protected mode (when the Status Register Write Disable (SRWD) bit is set to 1, and Write Protect (W#) is driven Low). In this mode, the non-volatile bits of the Status Register (SRWD, BP2, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

BP2, BP1, BP0 bits: The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or more of the Block Protect (BP2, BP1, BP0) bits is set to 1, the relevant memory area (Table 2 on page 11) becomes protected against Page Program (PP), and Sector Erase (SE) instructions. The Block Protect (BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode is not set. The Bulk Erase (BE) instruction is executed if, and only if, all Block Protect (BP2, BP1, BP0) bits are 0.

WEL bit: The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1, the internal Write Enable Latch is set; when set to 0, the internal Write Enable Latch is reset and no Write Status Register, Program or Erase instruction is accepted.

WIP bit: The Write In Progress (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle. This bit is a read only bit and is read by executing a RDSR instruction. If this bit is 1, such a cycle is in progress, if it is 0, no such cycle is in progress.

Write Status Register (WRSR)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it is accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction is decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code (Figure 8) and the data byte on Serial Data Input (SI).

The Write Status Register (WRSR) instruction has no effect on bits b6, b1 and b0 of the Status Register. Bit b6 is always read as 0.

Chip Select (CS#) must be driven High after the eighth bit of the data byte is latched in. If not, the Write Status Register (WRSR) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) is reset.

The WRSR instruction enables the user to select one of nine levels of protection. The S25FL064A is divided into eight array segments. The top one twenty-eighth, sixty-fourth, thirty-second, sixteenth, eighth, quarter, half or all of the memory segments can be protected (as defined in Table 1 on page 7). The data within a selected segment is therefore read-only. The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Write Disable (SRWD) bit in accordance with the Write Protect (W#) signal. The Status Register Write Disable (SRWD) bit and Write Protect (W#) signal allow the device to be put in the Hardware Protected Mode (HPM). The Write Status Register (WRSR) instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

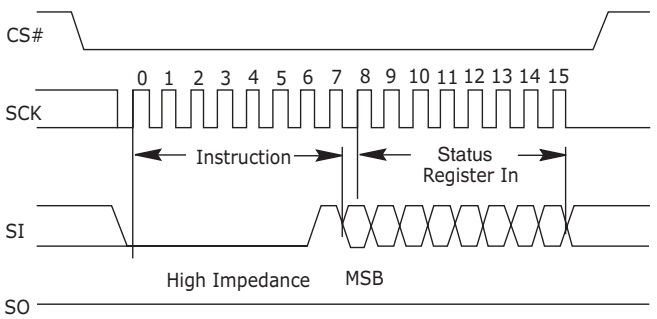


Figure 8. Write Status Register (WRSR) Instruction Sequence

Table 5. Protection Modes

W# Signal	SRWD Bit	Mode	Write Protection of the Status Register	Protected Area (See Note)	Unprotected Area (See Note)
1	1	Software Protected (SPM)	Status Register is Writable (if the WREN instruction set the WEL bit) The values in the SRWD, BP2, BP1 and BP0 bits can be changed	Protected against Page Program and Erase (SE, BE)	Ready to accept Page Program and Sector Erase Instructions
1	0				
0	0				
0	1	Hardware Protected (HPM)	Status Register is Hardware write protected The values in the SRWD, BP2, BP1 and BP0 bits cannot be changed	Protected against Page Program and Erase (SE, BE)	Ready to accept Page Program and Sector Erase Instructions

Note: *As defined by the values in the Block Protect (BP2, BP1, BP0) bits of the Status Register, as shown in Table 2 on page 11.*

The protection features of the device are summarized in Table 5.

When the Status Register Write Disable (SRWD) bit is 0 (its initial delivery state), it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit was previously set by a Write Enable (WREN) instruction, regardless of whether Write Protect (W#) is driven High or Low.

When the Status Register Write Disable (SRWD) bit is set to 1, two cases need to be considered, depending on the state of Write Protect (W#):

- If Write Protect (W#) is driven High, it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit was previously set by a Write Enable (WREN) instruction.
- If Write Protect (W#) is driven Low, it is not possible to write to the Status Register even if the Write Enable Latch (WEL) bit was previously set by a Write Enable (WREN) instruction. (Attempts to write to the Status Register are rejected, and are not accepted for execution.) As a consequence, all the data bytes in the memory area that are software protected (SPM) by the Block Protect (BP2, BP1, BP0) bits of the Status Register, are also hardware protected against data modification.

Regardless of the order of the two events, the Hardware Protected Mode (HPM) can be entered:

- By setting the Status Register Write Disable (SRWD) bit after driving Write Protect (W#) Low.
- By driving Write Protect (W#) Low after setting the Status Register Write Disable (SRWD) bit.

The only way to exit the Hardware Protected Mode (HPM) once entered, is to pull Write Protect (W#) High.

If Write Protect (W#) is permanently tied High, the Hardware Protected Mode (HPM) can never be activated and only the Software Protected Mode (SPM), using the Block Protect (BP2, BP1, BP0) bits of the Status Register, can be used.

Read Data Bytes (READ)

The READ instruction reads the memory at the specified SCK frequency (f_{SCK}) with a maximum speed of 25 MHz.

The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Read Data Bytes (READ) instruction is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of Serial Clock (SCK). Then the memory contents, at that address, are shifted out on Serial Data Output (SO), each bit being shifted out, at a frequency f_{SCK}, during the falling edge of Serial Clock (SCK).

The instruction sequence is shown in Figure 9. The first byte addressed can be at any location. The address automatically increments to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) instruction. When the highest address is reached, the address counter rolls over to 00000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes (READ) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Read Data Bytes (READ) instruction, while a Program, Erase, or Write cycle is in progress, is rejected without having any effect on the cycle that is in progress.

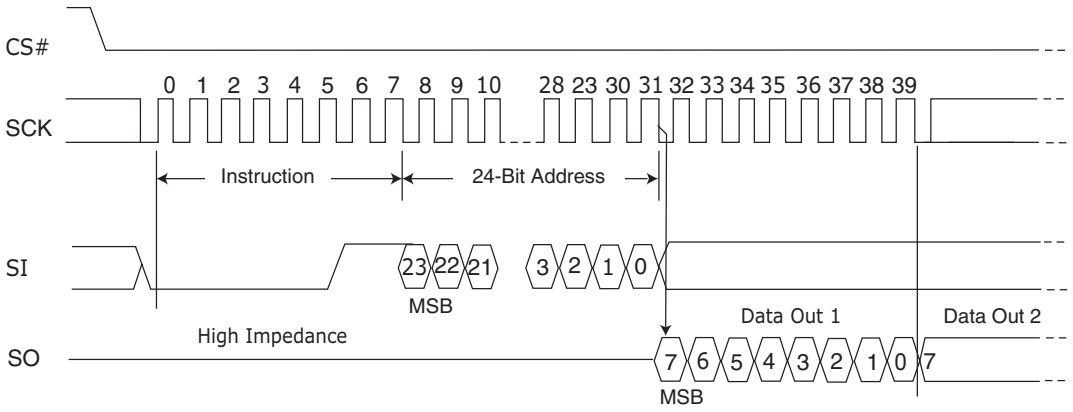


Figure 9. Read Data Bytes (READ) Instruction Sequence

Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ instruction reads the memory at the specified SCK frequency (f_{SCK}) with a maximum speed of 50 MHz. The device is first selected by driving Chip Select (CS#) Low. The instruction code for (FAST_READ) instruction is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (SCK). Then the memory contents, at that address, are shifted out on Serial Data Output (SO), each bit being shifted out, at a maximum frequency F_{SCK}, during the falling edge of Serial Clock (SCK).

The instruction sequence is shown in Figure 10, on page 23. The first byte addressed can be at any location. The address automatically increments to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single (FAST_READ) instruction. When the highest address is reached, the address counter rolls over to 00000h, allowing the read sequence to be continued indefinitely.

The (FAST_READ) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any (FAST_READ) instruction, while an Erase, Program, or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

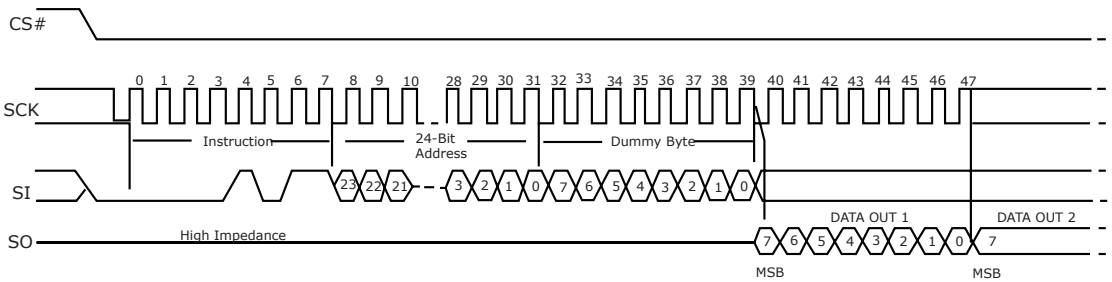


Figure I0. Read Data Bytes at Higher Speed (FAST_READ) Instruction Sequence

Read Identification (RDID)

The Read Identification (RDID) instruction allows the 8-bit manufacturer identification to be read, followed by two bytes of the device identification.

The manufacturer identification byte is assigned by JEDEC, and has a value of 01h for Spansion™ products. The device identification is assigned by the device manufacturer, and indicates the memory type in the first byte (02h), and the memory capacity of the device in the second byte (16h).

Any Read Identification (RDID) instruction executed while an Erase, Program, or Write Status Register cycle is in progress is not decoded, and has no effect on the cycle that is in progress.

The device is first selected by driving Chip Select (CS#) Low. Then, the 8-bit instruction code for the instruction is shifted in, with each bit being latched in on SI during the rising edge of SCK. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output (SO), with each bit being shifted out during the falling edge of Serial Clock (SCK).

The instruction sequence is shown in Figure 11.

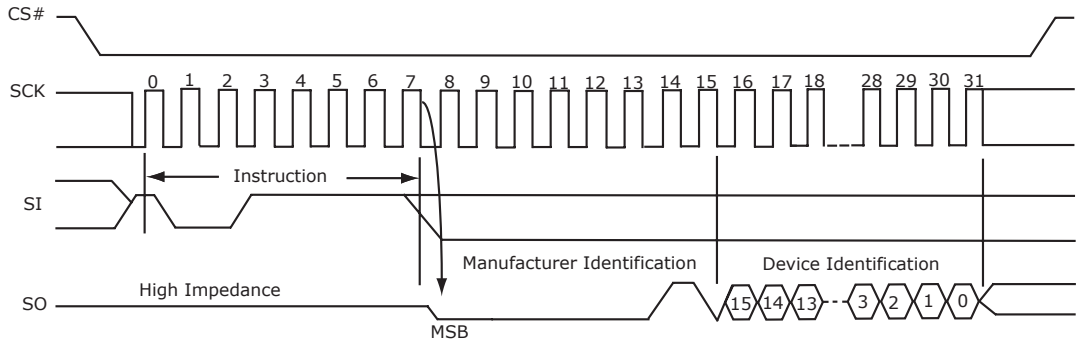


Figure II. Read Identification (RDID) Instruction Sequence and Data-Out Sequence

Driving CS# high after the Device Identification is read at least once terminates the READ_ID instruction. The Read Identification (RDID) instruction can also be terminated by driving CS# High at any time during data output.

When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Table 6. Read Identification (RDID) Data-Out Sequence

Manufacturer Identification	Device Identification	
	Memory Type	Memory Capacity
01h	02h	16h

Page Program (PP)

The Page Program (PP) instruction allows bytes to be programmed in the memory (changing bits from 1 to 0). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction is decoded, the device sets the Write Enable Latch (WEL).

The Page Program (PP) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, three address bytes and at least one data byte on Serial Data Input (SI). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 12, on page 25.

If more than 256 bytes are sent to the device, the addressing wraps to the beginning of the same page, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If fewer than 256 Data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

Chip Select (CS#) must be driven High after the eighth bit of the last data byte is latched in, otherwise the Page Program (PP) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) instruction applied to a page that is protected by the Block Protect (BP2, BP1, BP0) bits (Table 2 on page 11) is not executed.

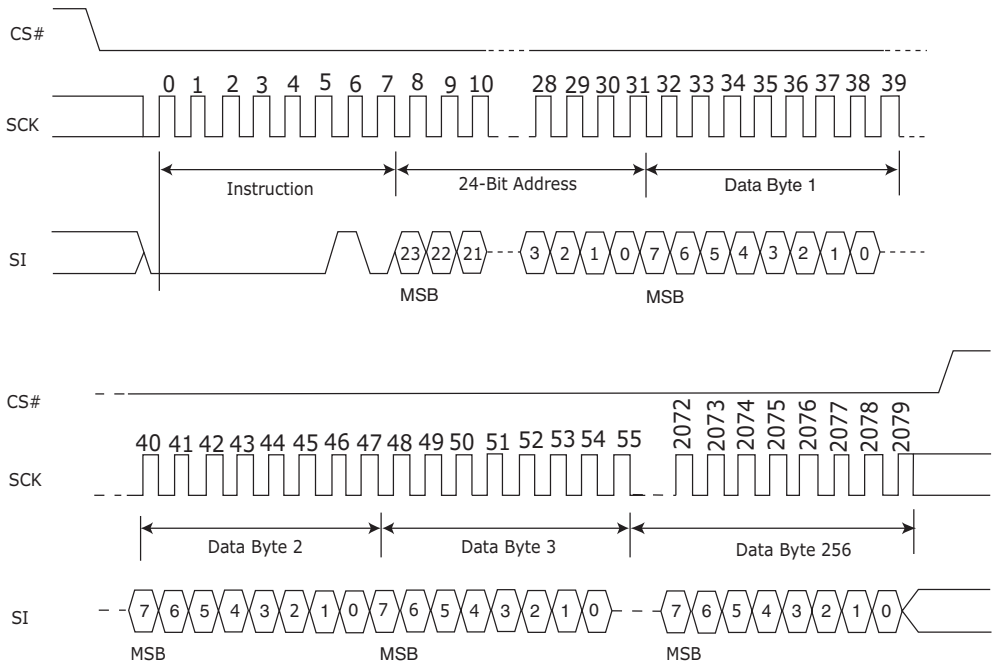


Figure I2. Page Program (PP) Instruction Sequence

Sector Erase (SE)

The Sector Erase (SE) instruction sets to 1 (FFh) all bits inside the chosen sector. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction is decoded, the device sets the Write Enable Latch (WEL).

The Sector Erase (SE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, and three address bytes on Serial Data Input (SI). Any address inside the Sector (Table 2 on page 11) is a valid address for the Sector Erase (SE) instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 13, on page 26.

Chip Select (CS#) must be driven High after the eighth bit of the last address byte is latched in, otherwise the Sector Erase (SE) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Sector Erase cycle (whose duration is tSE) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Sector Erase (SE) instruction applied to any memory area that is protected by the Block Protect (BP2, BP1, BP0) bits (Table 2 on page 11) is not executed.

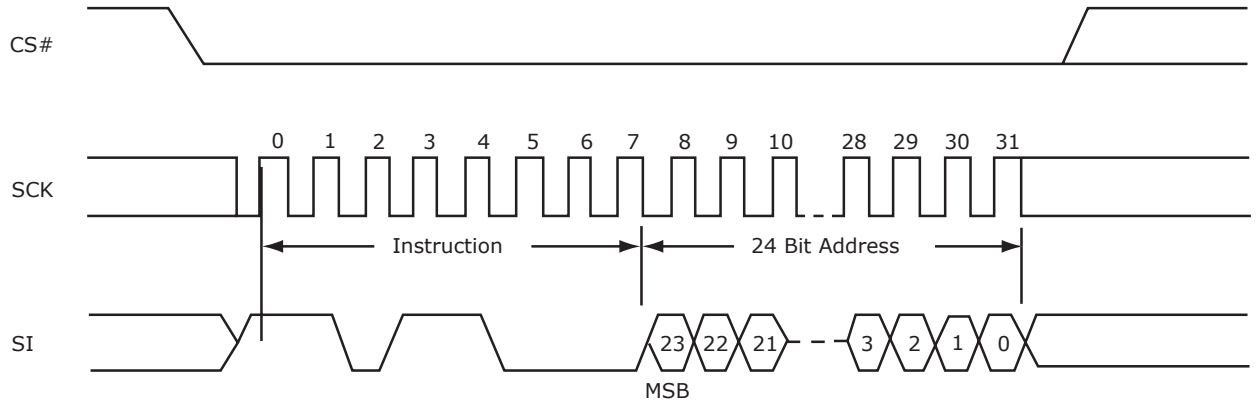


Figure 13. Sector Erase (SE) Instruction Sequence

Bulk Erase (BE)

The Bulk Erase (BE) instruction sets to 1 (FFh) all bits inside the entire memory. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction is decoded, the device sets the Write Enable Latch (WEL).

The Bulk Erase (BE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, on Serial Data Input (SI). No address is required for the Bulk Erase (BE) instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 14, on page 27.

Chip Select (CS#) must be driven High after the eighth bit of the last address byte is latched in, otherwise the Bulk Erase (BE) instruction is not executed.

As soon as Chip Select (CS#) is driven High, the self-timed Bulk Erase cycle (whose duration is t_{BE}) is initiated. While the Bulk Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Bulk Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Bulk Erase (BE) instruction is executed only if all the Block Protect (BP2, BP1, BP0) bits (see Table 2 on page 11) are set to 0. The Bulk Erase (BE) instruction is ignored if one or more sectors are protected.

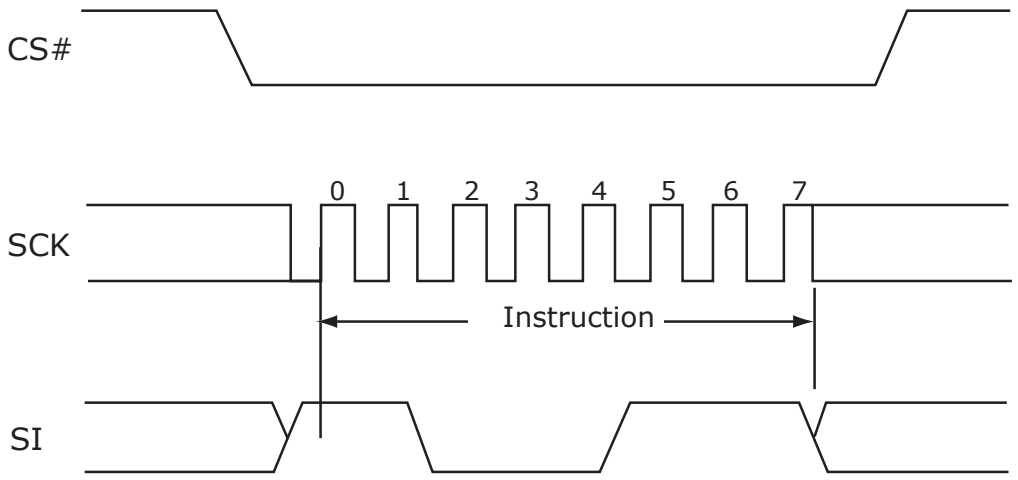


Figure 14. Bulk Erase (BE) Instruction Sequence

Deep Power Down (DP)

The Deep Power Down (DP) instruction puts the device in the lowest current mode of 1 µA typical.

It is recommended that the standard Standby mode be used for the lowest power current draw, as well as the Deep Power Down (DP) as an extra software protection mechanism when this device is not in active use. In this mode, the device ignores all Write, Program and Erase instructions. Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The Deep Power Down (DP) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code on Serial Data Input (SI). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 15, on page 28.

Driving Chip Select (CS#) High after the eighth bit of the instruction code is latched, places the device in Deep Power Down mode. The Deep Power Down mode can only be entered by executing the Deep Power Down (DP) instruction to reduce the standby current (from I_{SB} to I_{DP} as specified in Table 8 on page 33). As soon as Chip Select (CS#) is driven high, it requires a delay of t_{DP} currently in progress before Deep Power Down mode is entered.

Once the device enters the Deep Power Down mode, all instructions are ignored except the Release from Deep Power Down (RES) and Read Electronic Signature. This releases the device from the Deep Power Down mode. The Release from Deep Power Down and Read Electronic Signature (RES) instruction also allows the Electronic Signature of the device to be output on Serial Data Output (SO).

The Deep Power Down mode automatically stops at Power-down, and the device always powers up in the Standby mode.

Any Deep Power Down (DP) instruction, while an Erase, Program, or WRSR cycle is in progress, is rejected without having any effect on the cycle in progress.

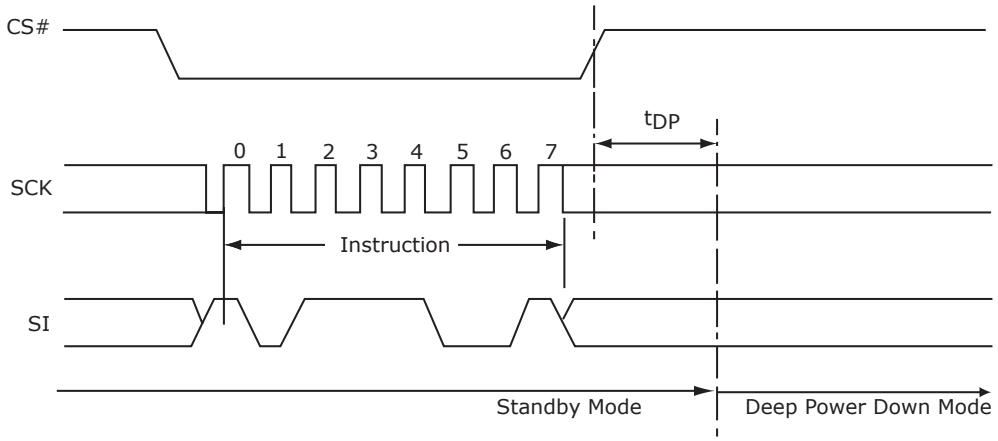


Figure 15. Deep Power Down (DP) Instruction Sequence

Release from Deep Power Down (RES)

The Release from Deep Power Down (RES) instruction provides the only way to exit the Deep Power Down mode. Once the device enters the Deep Power Down mode, all instructions are ignored except the Release from Deep Power Down (RES) instruction. Executing this instruction takes the device out of Deep Power Down mode.

The Release from Deep Power Down (RES) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code on Serial Data Input (SI). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 16, on page 29.

Driving Chip Select (CS#) High after the 8-bit instruction byte is received by the device, but before the whole of the 8-bit Electronic Signature is transmitted for the first time, still insures that the device is placed into Standby mode. If the device was previously in the Deep Power Down mode, though, the transition to the Stand-by Power mode is delayed by t_{RES}, and Chip Select (CS#) must remain High for at least $t_{RES(max)}$, as specified in Table 10 on page 35. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode, and execute instructions.

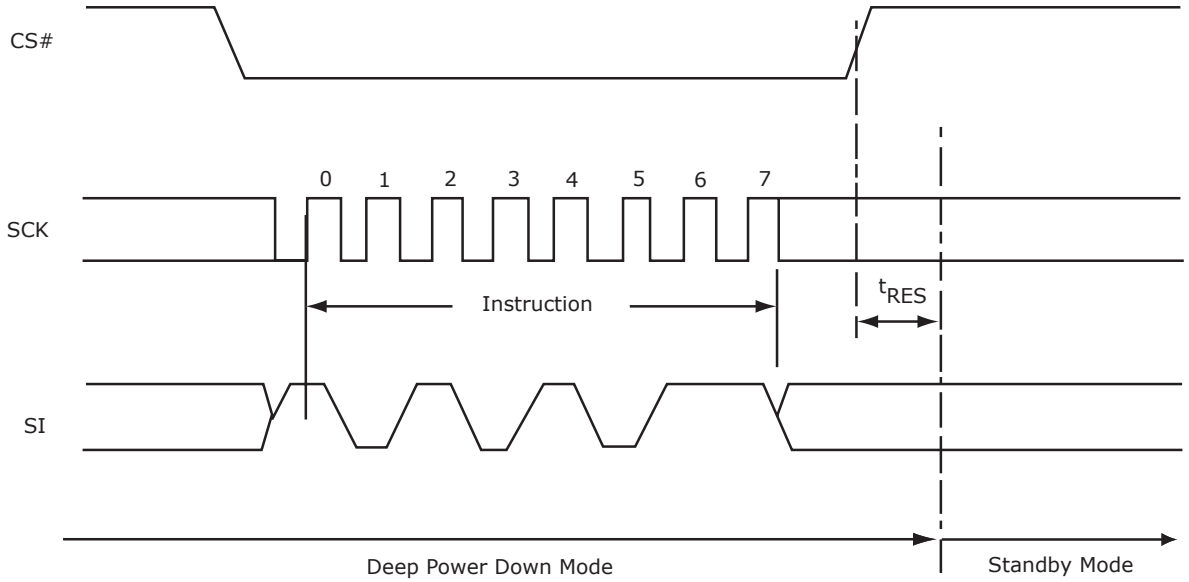


Figure 16. Release from Deep Power Down Instruction Sequence

Release from Deep Power Down and Read Electronic Signature (RES)

Once the device enters Deep Power Down mode, all instructions are ignored except the RES instruction. The RES instruction can also be used to read the old-style 8-bit Electronic Signature of the device on the SO pin. The RES instruction always provides access to the device's Electronic Signature (except while an Erase, Program, or WRSR cycle is in progress), and can be applied even if DP mode was not entered. Any RES instruction executed while an Erase, Program, or WRSR cycle is in progress, is not decoded and has no effect on the cycle in progress.

The device features an 8-bit Electronic Signature, whose value for the S25FL064A is 16h. This is read using the RES instruction.

The device is first selected by driving Chip Select (CS#) Low. The instruction code is followed by three dummy bytes, each bit being latched-in on Serial Data Input (SI) during the rising edge of Serial Clock (SCK). Then, the 8-bit Electronic Signature, stored in the memory, is shifted out on Serial Data Output (SO), each bit being shifted out during the falling edge of Serial Clock (SCK).

The instruction sequence is shown in Figure 17, on page 30.

The Release from Deep Power Down and Read Electronic Signature (RES) is terminated by driving Chip Select (CS#) High after the Electronic Signature is read at least once. Sending additional clock cycles on Serial Clock (SCK), while Chip Select (CS#) is driven Low, causes the Electronic Signature to be output repeatedly.

When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power Down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power Down mode, though, the transition to the Standby mode is delayed by t_{RES}, and Chip Select (CS#) must remain High for at lease $t_{RES(max)}$, as specified in Table 10 on page 35. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode, and execute instructions.

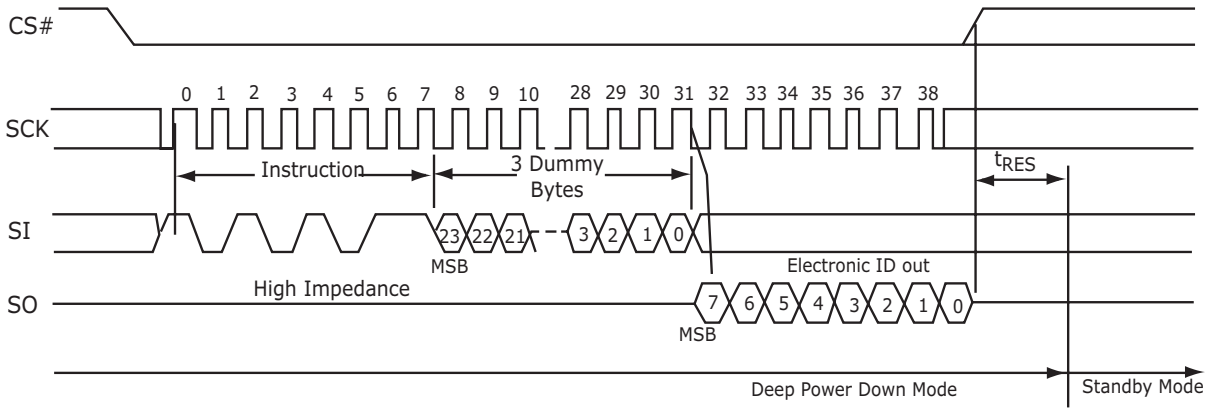


Figure 17. Release from Deep Power Down and Read Electronic Signature (RES) Instruction Sequence

Power-up and Power-down

The device must not be selected at power-up or power-down (that is, CS# must follow the voltage applied on V_{CC}) until V_{CC} reaches the correct value as follows:

- V_{CC} (min) at power-up, and then for a further delay of t_{PU} (Table 7 on page 31)
- V_{SS} at power-down

A simple pull-up resistor on Chip Select (CS#) can usually be used to insure safe and proper power-up and power-down.

The device ignores all instructions until a time delay of t_{PU} (Table 7 on page 31) has elapsed after the moment that V_{CC} rises above the minimum V_{CC} threshold. However, correct operation of the device is not guaranteed if by this time V_{CC} is still below V_{CC} (min). No Write Status Register, Program or Erase instructions should be sent until t_{PU} after V_{CC} reaches the minimum V_{CC} threshold.

At power-up, the device is in Standby mode (not Deep Power Down mode) and the WEL bit is reset.

Normal precautions must be taken for supply rail decoupling to stabilize the V_{CC} feed. Each device in a system should have the V_{CC} rail decoupled by a suitable capacitor close to the package pins (this capacitor is generally of the order of 0.1 µF).

At power-down, when V_{CC} drops from the operating voltage to below the minimum V_{CC} threshold, all operations are disabled and the device does not respond to any instructions. (The designer needs to be aware that if a power-down occurs while a Write, Program or Erase cycle is in progress, data corruption can result.)

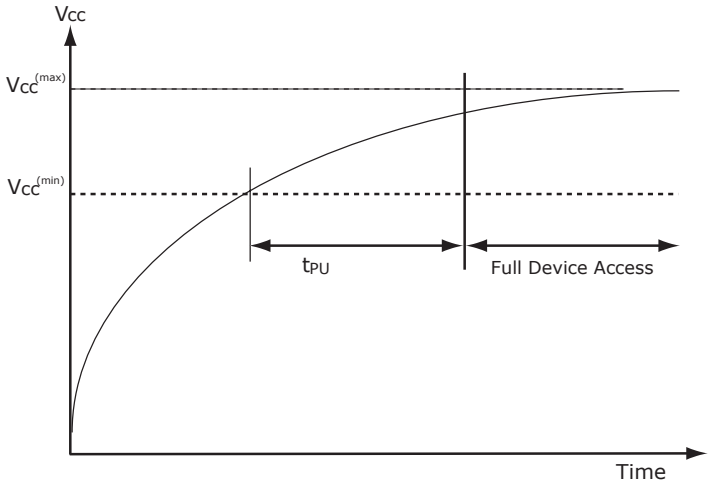


Figure 18. Power-Up Timing

Table 7. Power-Up Timing

Symbol	Parameter	Min	Max	Unit
$V_{CC(min)}$	V_{CC} (minimum)	2.7		V
t_{PU}	V_{CC} (min) to device operation	10		ms

Initial Delivery State

The device is delivered with all bits set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

Maximum Rating

Stressing the device above the rating listed in the **Absolute Maximum Ratings** section below may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Absolute Maximum Ratings

Ambient Storage Temperature . . . . . –65°C to +150°C

Voltage with Respect to Ground:

All Inputs and I/Os. . . . . –0.3 V to 4.5 V

Operating Ranges

Ambient Operating Temperature (T_A)

Commercial . . . . . 0°C to +70°C

Industrial . . . . . –40°C to +85°C

Positive Power Supply

Voltage Range . . . . . 2.7 V to 3.6 V

Note: *Operating ranges define those limits between which functionality of the device is guaranteed.*

DC Characteristics

This section summarizes the DC and AC Characteristics of the device. Designers should check that the operating conditions in their circuit match the measurement conditions specified in the Test Specifications in Table 9 on page 34, when relying on the quoted parameters.

CMOS Compatible

Table 8. DC Characteristics

Parameter	Description	Test Conditions (See Note)		Min	Typ.	Max	Unit
V_{CC}	Supply Voltage			2.7	3	3.6	V
I_{CC1}	Active Read Current	SCK = 0.1 V_{CC}/0.9V_{CC}	25 MHz		8	10	mA
		SCK = 0.1 V_{CC}/0.9V_{CC}	V_{CC} = 3.0V 50 MHz		10	13	mA
I_{CC2}	Active Page Program Current	CS# = V_{CC}				26	mA
I_{CC3}	Active WRSR Current	CS# = V_{CC}				28	mA
I_{CC4}	Active Sector Erase Current	CS# = V_{CC}				26	mA
I_{CC5}	Active Bulk Erase Current	CS# = V_{CC}				26	mA
I_{SB}	Standby Current	V_{CC} = 3.0 V CS# = V_{CC}				50	µA
I_{DP}	Deep Power Down Current	V_{CC} = 3.0 V CS# = V_{CC}			1	10	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}				1	µA
I_{LO}	Output Leakage Current	V_{IN} = GND to V_{CC}				1	µA
V_{IL}	Input Low Voltage			−0.3		0.3 V_{CC}	V
V_{IH}	Input High Voltage			0.7 V_{CC}		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA, V_{CC} = $V_{CC\ min}$				0.4	V
V_{OH}	Output High Voltage	I_{OH} = −0.1 mA		V_{CC} − 0.2			V

Note: *Typical values are at T_A = 25°C and 3.0 V.*

Test Conditions

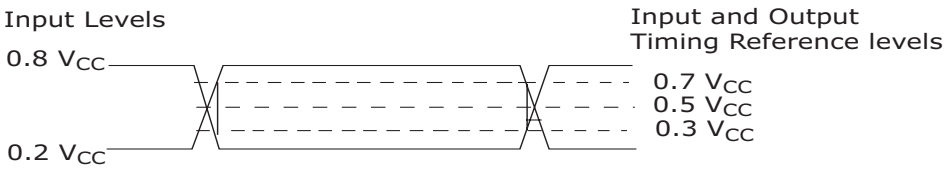


Figure 19. AC Measurements I/O Waveform

Table 9. Test Specifications

Symbol	Parameter	Min	Max	Unit
C_L	Load Capacitance	30		pF
	Input Rise and Fall Times		5	ns
	Input Pulse Voltage	0.2 V_{CC} to 0.8 V_{CC}		V
	Input Timing Reference Voltage	0.3 V_{CC} to 0.7 V_{CC}		V
	Output Timing Reference Voltage	0.5 V_{CC}		V

AC Characteristics

Table 10. AC Characteristics

Symbol (Notes)	Parameter	Min	Typ (Notes)	Max (Notes)	Unit
F_{SCK}	SCK Clock Frequency READ instruction	D.C.		25	MHz
F_{SCK}	SCK Clock Frequency for: FAST_READ, PP, SE, BE, DP, RES, WREN, WRDI, RDSR, WRSR	D.C.		50	MHz
t_{CRT}	Clock Rise Time (Slew Rate)	0.1			V/ns
t_{CFT}	Clock Fall Time (Slew Rate)	0.1			V/ns
t_{WH}	SCK High Time	9			ns
t_{WL}	SCK Low Time	9			ns
t_{CS}	CS# High Time	100			ns
t_{CSS} (3)	CS# Setup Time	5			ns
t_{CSH} (3)	CS# HOLD Time	5			ns
t_{HD} (3)	HOLD# Setup Time (relative to SCK)	5			ns
t_{CD} (3)	HOLD# Hold Time (relative to SCK)	5			ns
t_{HC}	HOLD# Setup Time (relative to SCK)	5			ns
t_{CH}	HOLD# Hold Time (relative to SCK)	5			ns
t_{V}	Output Valid	0		9	ns
t_{HO}	Output Hold Time	0			ns
$t_{HD:DAT}$	Data in Hold Time	5			ns
$t_{SU:DAT}$	Data in Setup Time	5			ns
t_{R}	Input Rise Time			5	ns
t_{F}	Input Fall Time			5	ns
t_{LZ} (3)	HOLD# to Output Low Z			10	ns
t_{HZ} (3)	HOLD# to Output High Z			10	ns
t_{DIS} (3)	Output Disable Time			10	ns
t_{WPS} (3)	Write Protect Setup Time	15			ns
t_{WPH} (3)	Write Protect Hold Time	15			ns
t_{W}	Write Status Register Time			60	ms
t_{DP}	CS# High to Deep Power Down Mode			3	µs
t_{RES}	Release DP Mode			30	µs
t_{PP}	Page Programming Time		1.5 (1)	3 (2)	ms
t_{SE}	Sector Erase Time		1.5 (1)	3 (2)	sec
t_{BE}	Bulk Erase Time		192 (1)	384 (2)	sec

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, VCC = 3.0V; 10, 000 cycles; checkerboard data pattern*
2. *Under worst-case conditions of 90°C; VCC = 2.7V; 100,000 cycles*
3. *Not 100% tested*

AC Characteristics

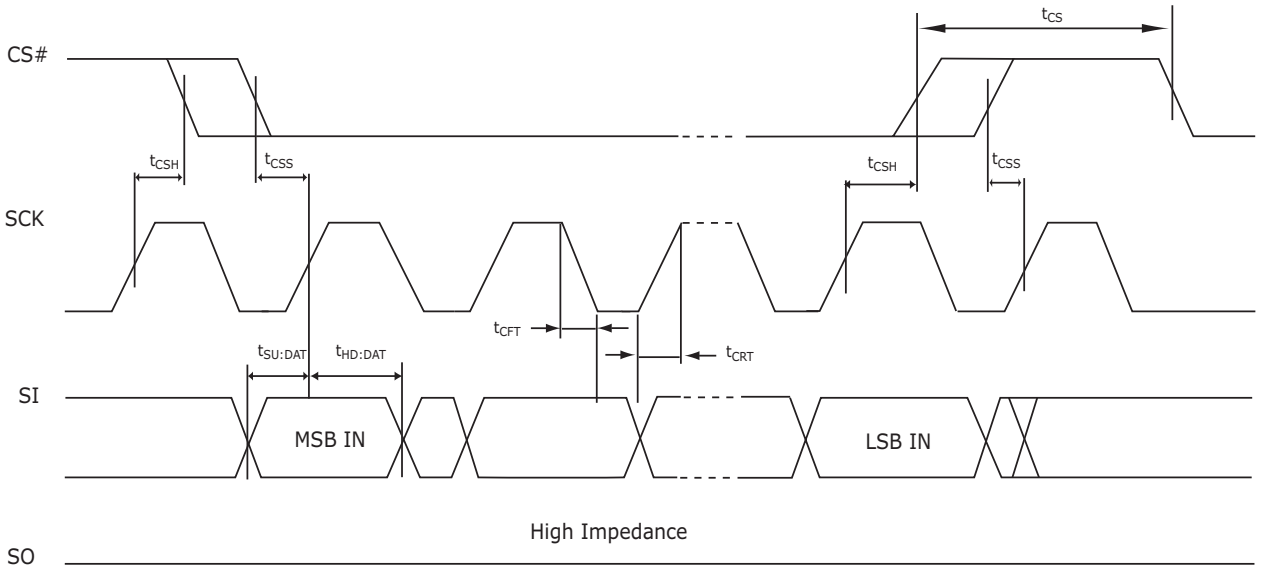


Figure 20. SPI Mode 0 (0,0) Input Timing

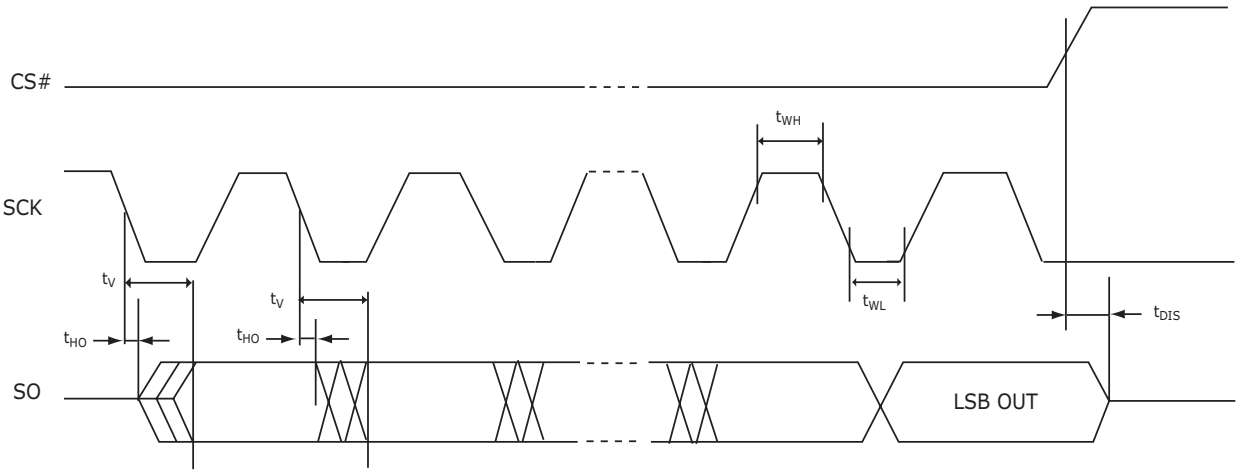


Figure 21. SPI Mode 0 (0,0) Output Timing

AC Characteristics

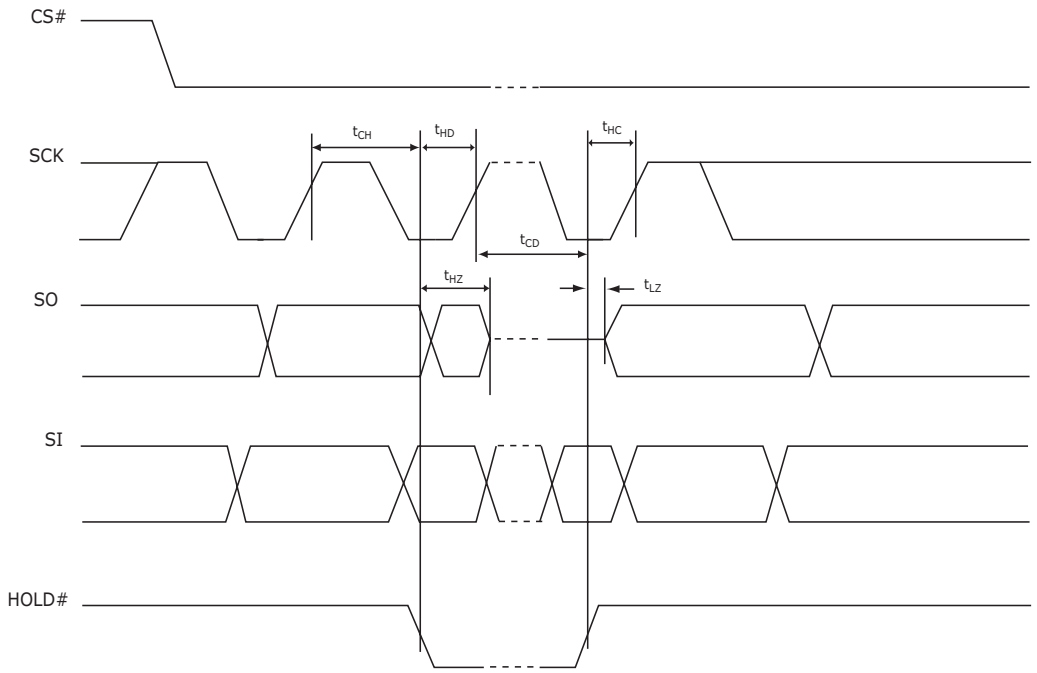


Figure 22. HOLD# Timing

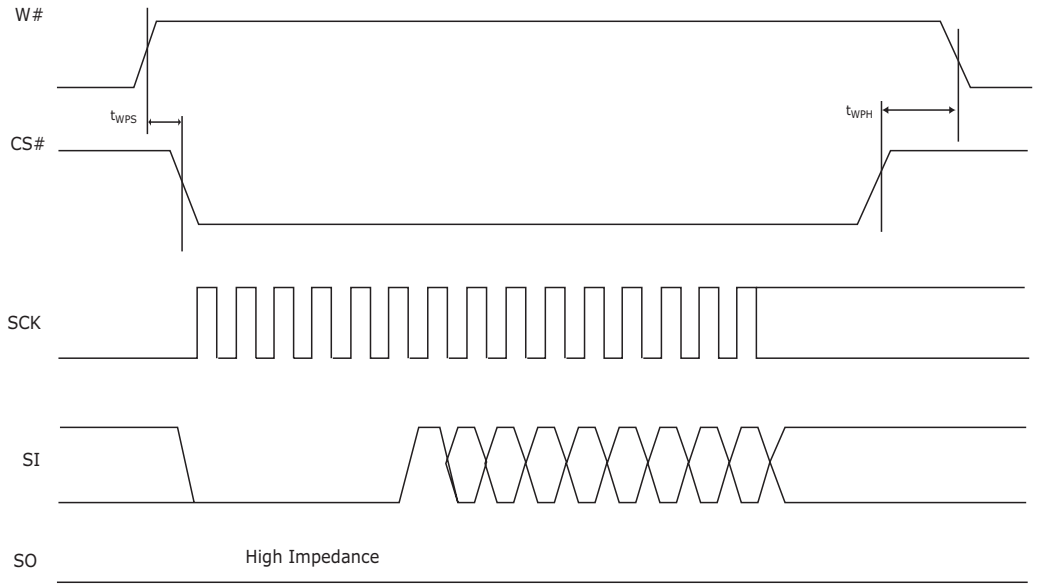
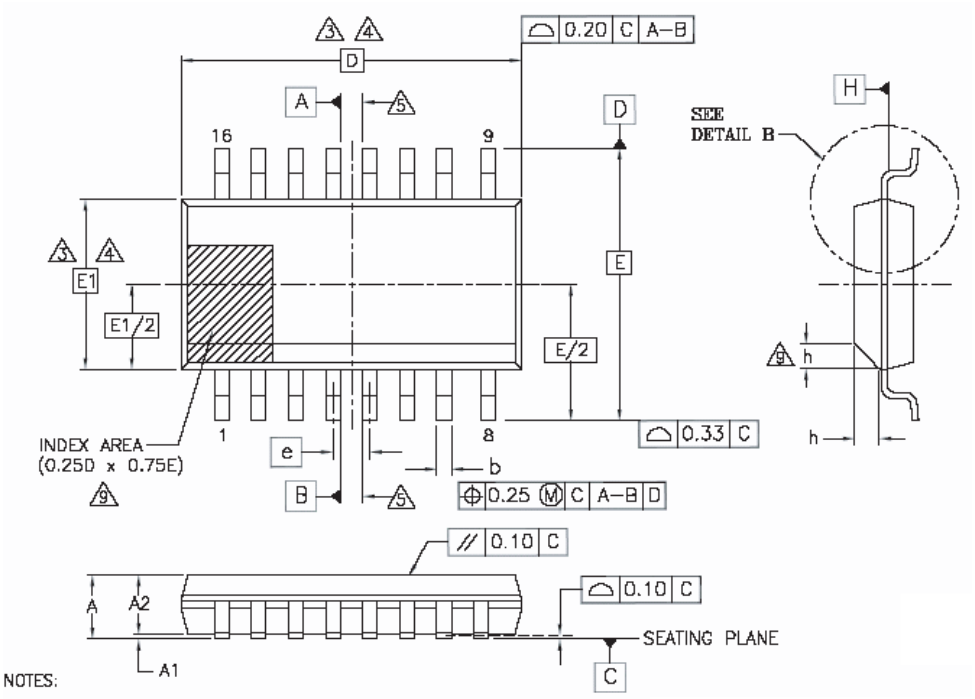


Figure 23. Write Protect Setup and Hold Timing during WRSR when SRWD=I

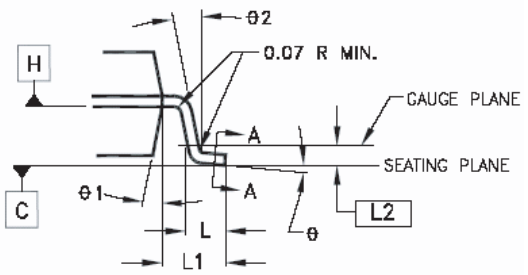
Physical Dimensions

S016 Wide—16-pin Plastic Small Outline 300 mils Body Width Package



NOTES:

PACKAGE	xSO3 016(INCHES)		xSO3 016(MM)	
JEDEC	MS-013(D)AA		MS-013(D)AA	
SYMBOL	MIN	MAX	MIN	MAX
A	.093	.104	2.35	2.65
A1	.004	.012	0.10	0.30
A2	.081	.104	2.05	2.55
b	.012	.020	0.31	0.51
b1	.011	.019	0.27	0.48
c	.008	.013	0.20	0.33
c1	.008	.012	0.20	0.30
D	.406 BSC		10.30 BSC	
E	.406 BSC		10.30 BSC	
E1	.295 BSC		7.50 BSC	
e	.050 BSC		1.27 BSC	
L	.016	.050	0.40	1.27
L1	.055 REF		1.40 REF	
L2	.010 BSC		0.25 BSC	
N	16		16	
h	0.10	0.30	0.25	0.75
θ	0°	8°	0°	8°
θ1	5°	15°	5°	15°
θ2	0°		0°	



Revision Summary

Revision A0 (April 26, 2005)

Initial Release.

Colophon

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