EG&G RETICON

D Series Tapped High Speed Charge-Coupled Photodiode Array

T-41-55

EG&G Reticon's RL1282D, RL1284D and RL1288D are ultra-high-speed, self-scanned charge-coupled linear arrays with video output taps every 128 diodes. The RL1282D has two sections and a resolution of 256, the RL1284D has four sections and a resolution of 512, and the RL1288D has eight sections with 1024 resolution.

Applications for these arrays include optical character recognition, high-speed document scanning, pattern recognition, noncontact measurement, or any process requiring a high-speed linear array.

Key Features:

- 256, 512 or 1024 elements
- 18 µm x 18 µm picture elements
- Low power requirements
- +15 and -5V supplies
- On-chip preamplifier
- Wide dynamic range
- Low noise equivalent exposure
- Video sampling rates up to 15 MHz per output channel
- Effective data rates to 240 MHz
- 4.2 µs line scan time
- Wide spectral response, near UV to near IR
- Antiblooming circuitry
- Line reset feature

Functional Description

The RL1282D, RL1284D, and RL1288D have 256, 512 and 1024 contiguous diodes respectively, divided into sections of 128 pixels. Each block of 128 pixels has two shift registers for readout, one for odd-numbered pixels within a section (odd video channel), the other for even-numbered pixels within a section (even video channel). The RL1282D, RL1284D, and RL1288D have, respectively, 4, 8, and 16 CCD analog shift registers and the same number of video output lines. Each video output has a preamplifier and can obtain pixel rates up to 15 MHz. Pin configurations are shown in Figure 1. Figure 2 is a simplified schematic diagram.

The sensing elements consist of a row of diffused p-n junction photodiodes spaced on 18 µm centers and interdigitated into a sensing aperture 18 µm wide. Figure 3 gives the aperture response function and sensor geometry where a = photodiode width, b = center-to-center spacing, and c = aperture width. Light incident on the sensing aperture generates photocurrent which is integrated and stored as a charge on the capacitance of each of the photodiodes. If the charge accumulated on any diode exceeds a saturation value, the excess is shunted to the reset drain V_{RD} (Figure 2), through the antiblooming gates ϕ_{AB}, thus avoiding blooming effects.

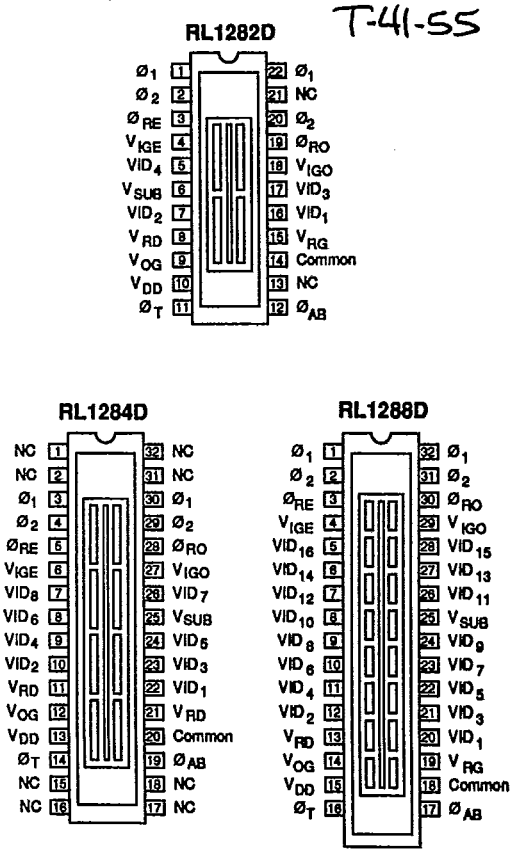

Figure 1. Pinout configurations

At the end of each integration period, the charges on all the diodes are simultaneously switched through transfer gates, ϕ_T, into CCD analog shift registers for readout. The photodiodes of each section are divided, with the 64 odd diodes switched into one register and the 64 even diodes into the other. Immediately after this parallel transfer, a new integration period begins.

Readout for each block is accomplished by clocking the CCD shift registers so that the charge packets are delivered sequentially into two on-chip charge-detection circuits (refer to Figure 5 for timing). The registers deliver the charge packets alternately, allowing the inactive charge detector to be reset to a fixed level of ϕ_{RE} or ϕ_{RO} while the opposite detector is active. The outputs of the two detectors may then be multiplexed off-chip to obtain a stepwise-continuous video signal.

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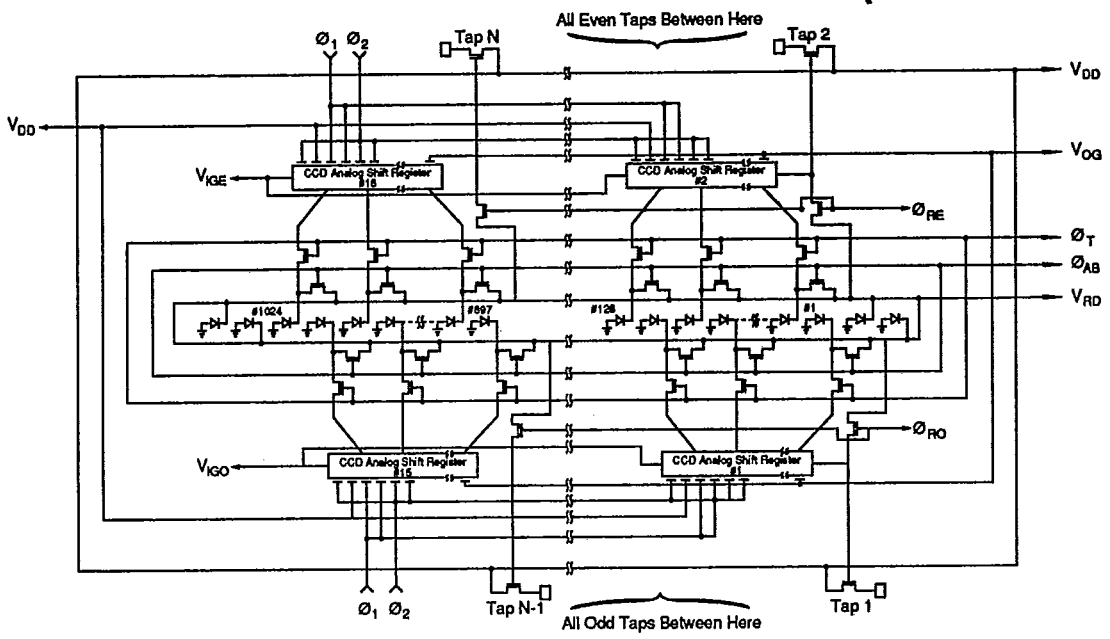

Figure 2. Schematic diagram of D Series Tapped

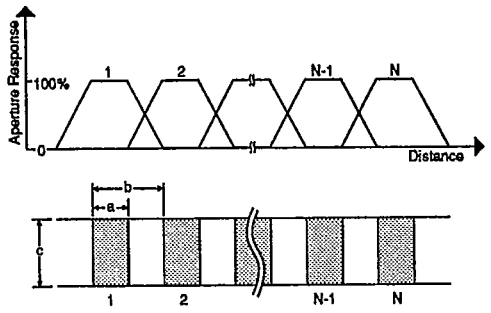

Figure 3. Sensor geometry and idealized aperture response

Operation

The D Series Tapped arrays require two clock pulses, $\varnothing_1$ and $\varnothing_2$, a transfer gate pulse, $\varnothing_T$, and several bias inputs (all voltage references are to common or ground level). The $\varnothing_1$ and $\varnothing_2$ clock waveforms should swing between 0 and +15V. The two-phase clock waveforms are depicted in Figure 4 with waveforms crossing at the 60% amplitude level. The minimum clock crossings is 60% (see Figure 4). For high-speed operation, the rise and fall should be less than 30 nanoseconds, with no over- or under-shooting on the clock edges.

The transfer pulse, $\varnothing_T$, should swing between -3 and +5V and have a width greater than 0.5 µsec. In order to transfer the charge from the photodiodes into the CCD register, the $\varnothing_1$ clock should remain high during the blanking and transfer interval, as shown in Figure 5. This same figure also shows $\varnothing_{RE}$, the even reset clock, and its relationship to $\varnothing_1$ and $\varnothing_2$ clocks, as well as the odd and even video outputs. The odd and even output reset clocks, $\varnothing_{RO}$ and $\varnothing_{RE}$, are derived from the same sources as $\varnothing_1$ and $\varnothing_2$ and are nominally synchronous with them.

A bias charge level is not required in the CCD registers to obtain operation. This charge is supplied by biasing the V_{IGE} and V_{IGO} inputs to the registers with a positive voltage which is nominally set at 8.5V. Also, in order to balance the dc output levels of the two registers, one input level can be adjusted relative to the other. Resistive dividers (potentiometers) may be used since very little current is required.

The output gate, V_{OG}, draws negligible current. It may also be biased, through a resistive divider, to any voltage from 2 to 5.5V.

The substrate, V_{SUB}, is held at -5V, the common reference and the antiblooming gate, $\varnothing_{AB}$, are at ground, and the output amplifier drain, V_{DD}, is at +15V. The V_{RG} gate is used for test purposes at the factory and is normally set at +10V during operation.

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The reset drain, V_{RD}, normally is connected to 10.5V, but may be at an intermediate level if desired. In some applications, it may be desirable to define an integration period shorter than the readout time. This may be accomplished by resetting the diodes with the antiblooming gate. At the desired reset time, ϕ_{AB} is pulsed to +15V for at least one µsec and then back to ground. The integration period is then the time between the trailing edge of the ϕ_{AB} pulse and the trailing edge of the next ϕ_T pulse. At low voltages (typically 2-3V), ϕ_{AB} drains off saturation charges. This can be used to eliminate blooming effects. With the output at saturation, ϕ_{AB} is increased from ground until the output voltage begins to decrease. At this point, charge in excess of saturation is shunted to V_{RD}.

A suitable high-speed video output circuit is shown in Figure 6. This circuit is preferable to a 3K load resistor because it reduces the current demand while maintaining speed capabilities.

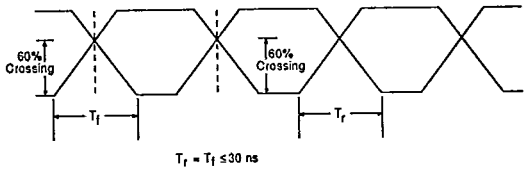

Figure 4. Two-phase clocks

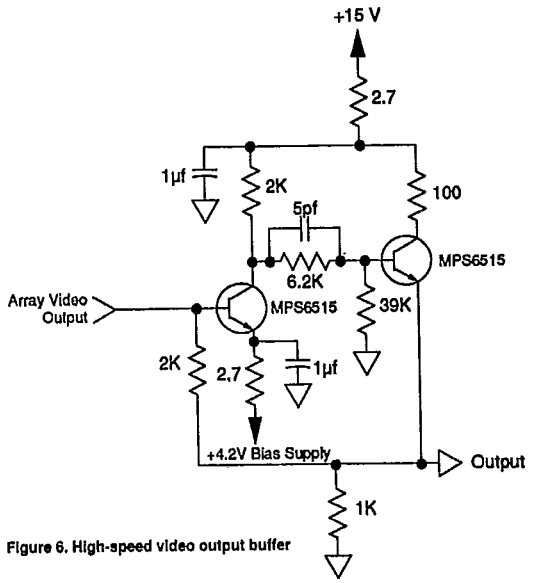

Figure 6. High-speed video output buffer

Performance

Spectral response of the D Series Tapped arrays is similar to that of other high-quality silicon photodetectors, covering the range from near UV to near IR. A quartz window is standard. Relative spectral response is shown as a function of wavelength in Figure 7.

As most applications for these devices (OCR, machine vision, etc.) use visible light, the responsivity and uniformity of response are specified using a source with the spectral distribution shown by the dotted line in Figure 7. This spectral distribution is produced by filtering a 2870°K tungsten source with a Fish-Schurman HA-11 heat-absorbing 1 mm thick filter.

Transfer characteristics showing the saturation output voltage can be seen in Figure 8. Since Reticon line scanners operate in the charge-storage mode, the charge output of each diode (below saturation) is proportional to exposure, i.e., the irradiance or light intensity multiplied by the integration time or the time interval between successive transfer pulses.

There is a trade-off between scanning speed and the required light intensity. Light intensity (watts), needed to saturate a pixel at a particular integration time, can be obtained by dividing saturation exposure by integration time. Longer integration times may be used to detect lower light levels. However, this approach is ultimately limited by dark leakage current which is integrated along with the photocurrent.

Video Output waveforms shown in Figure 5 typify video output performance as measured across a 3K load resistor. The rise and fall times are relative since they are affected by capacitive loading, including oscilloscope probe capacitance. For data rates greater than 3 MHz, an output circuit such as Figure 6 is recommended and video rise and fall times of 50 ns or less are typical.

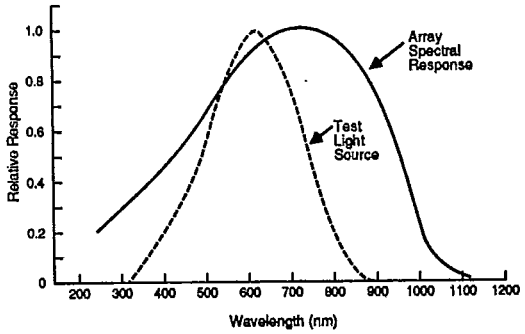

Figure 7. Relative spectral response as a function of wavelength

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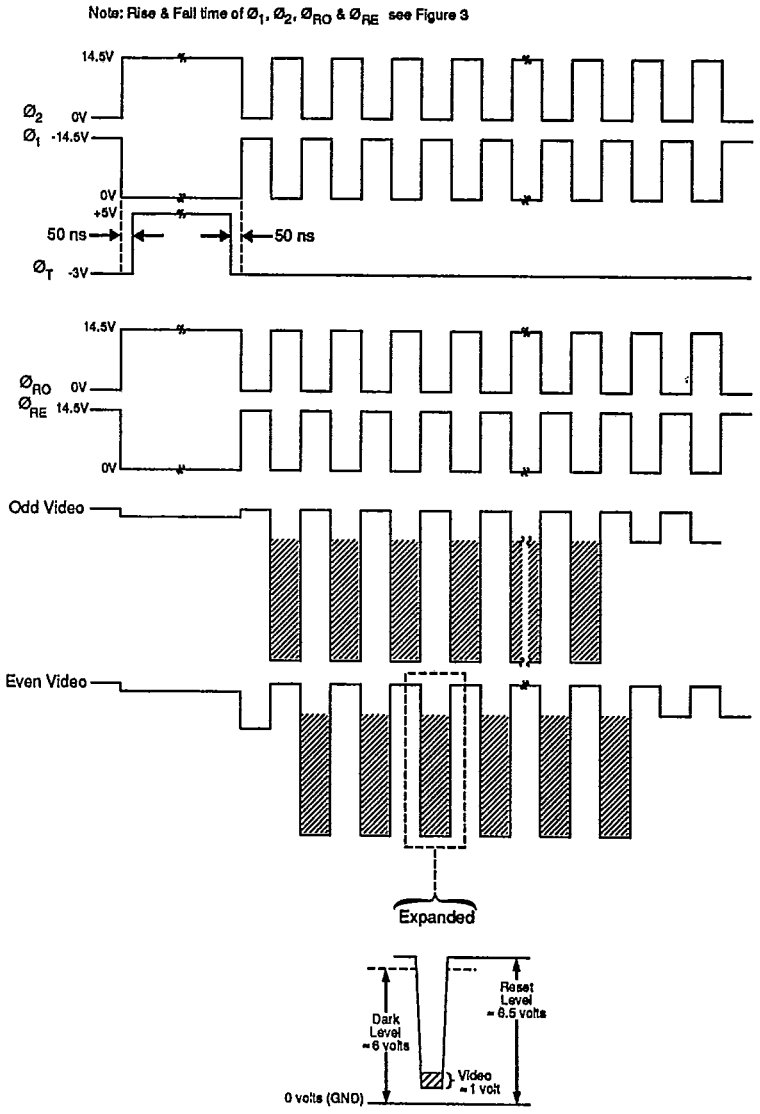

Figure 5. Timing relationship of the array's clocks and output

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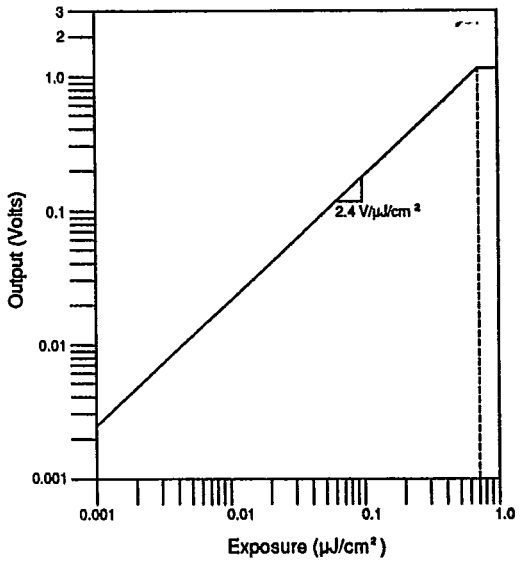

Figure 8. Typical transfer characteristic

Circuits

A complete evaluation circuit board is available for the D Series Tapped arrays and is recommended for first-time evaluation. The RC0716 Board contains all required drive circuitry and has buffered outputs capable of speeds to 10 MHz/tap.

Table I. Absolute Maximum Ratings
(Above Which Useful Life May be Impaired)

Storage temperature	-25°C to 100°C
Operating temperature	-25°C to 55°C
Voltage on any pin with respect to substrate	-0.3V to 22V

Table II. Typical Clock Capacitance *

Clock	Capacitance (pF)		
	RL1282	RL1284	RL1288
$Ø_1$	65	137	186
$Ø_2$	64	143	183
$Ø_2$	65	155	187
$Ø_1$	65	120	194
$Ø_T$	19	42	56
$Ø_{RO}$	7	11	18
$Ø_{AB}$	19	19	19
$Ø_{RE}$	9	13	19

* Measured with 10V applied to the terminal

Table III. Drive and Voltage Requirements [1]

Symbol	Parameter		Min	Typ	Max	Units
V_{RD}	Reset drain bias		10	10.5	13	V
V_{DD}	Output drain bias			14.5	15	V
V_{OG}	Output gate bias		2	3.5	5.5	V
V_{IG}	Input gate bias [2]		6	8.5	14	V
$Ø_{AB}$	Antiblooming gate [3]		-	0	-	V
V_{SUB}	Substrate bias		-5.25	-5	-4.75	V
$Ø_1, Ø_2$	CCD transport clocks	High	14	14.5	15	V
		Low	-0.3	0	+0.5	V
$Ø_T$	Transfer clock	High	3	5	7	V
		Low	-5	-3	-2	V
$Ø_{RE}$	Reset - High		14	14.5	15	V
$Ø_{RO}$	Clocks - Low		-0.3	0	+0.5	V
V_{RG}				10	10.5	V
f_{clock}	Video sampling rate [4]			-	15	MHz

Notes:

1. All voltage referenced to COMMON. Use typical values for best performance
2. The odd and even input gate biases may be adjusted differentially to achieve an odd/even balance in the video output
3. Maximum effective array data rate is as follows (15 MHz per video output); RL1282D = 60 MHz; RL1284D = 120 MHz; RL1288D = 240 MHz
4. See text

Table IV. Array Performance Characteristics (@ 200 Hz, 25°C)
(Use Typical Voltages shown in Table III)

Symbol	Parameter	Min	Typ	Max	Units
DRFPN	Dynamic range FPN [1,6]	250	600		-
DRTN	Dynamic range thermal noise [2]	1200	7500		
E_{NE}	Peak-to-peak noise Equivalent exposure [3]	-	.0004		µj/cm²
E_{SAT}	Saturation exposure [3]		0.45	0.7	µj/cm²
	Spectral response range Limits	-	0.2-1.1	-	µm
R	Responsivity [3,4]	2.0	2.4	-	V per µj/cm²
	Photoresponse nonuniformity:				
	Individual output [3,5,8]		5	10	±%
	Match across array [3,5,7,8]		7	15	%
V_{DARK}	Average dark signal [6]	-		4	mV
	Dark signal nonuniformity FPN (Fixed Pattern Noise) [6]	-	1	5	mV
V_{SAT}	Saturation output voltage	1.2	1.5	-	V
P	Power dissipation D.C. [4]	-	600	-	mW
R_O	Output impedance	-	1500	-	Ω
N_{PP}	Peak-to-peak noise [2]		1	5	mV
	Dark level DC mismatch (output to output)		150	400	mV
	Dark level [7]		6.0		V
CTE	Charge transfer efficiency		.99995		

Notes:
1. Dynamic range defined as V_{SAT}/p-p fixed pattern noise
2. Dynamic range defines as V_{SAT}/single pixel rms thermal noise; rms noise is defined as 1/5 of p-p noise
3. Measured using light source of Figure 6. Filtered with Fish-Schurman HA-11 heat absorbing filter
4. 3KΩ load resistors and V_{DD} = 14.5V
5. Measured with uniform illumination at approximately 50% of saturation
6. At 20°C with 1 msec integration time. Dark signal and dark signal nonuniformity are proportional to integration time, and approximately double for every 7°C increase in temperature
7. See Figure 5 for output schematic
8. Calculated as: + % NU = Max Diode - Avg./Avg. x 100

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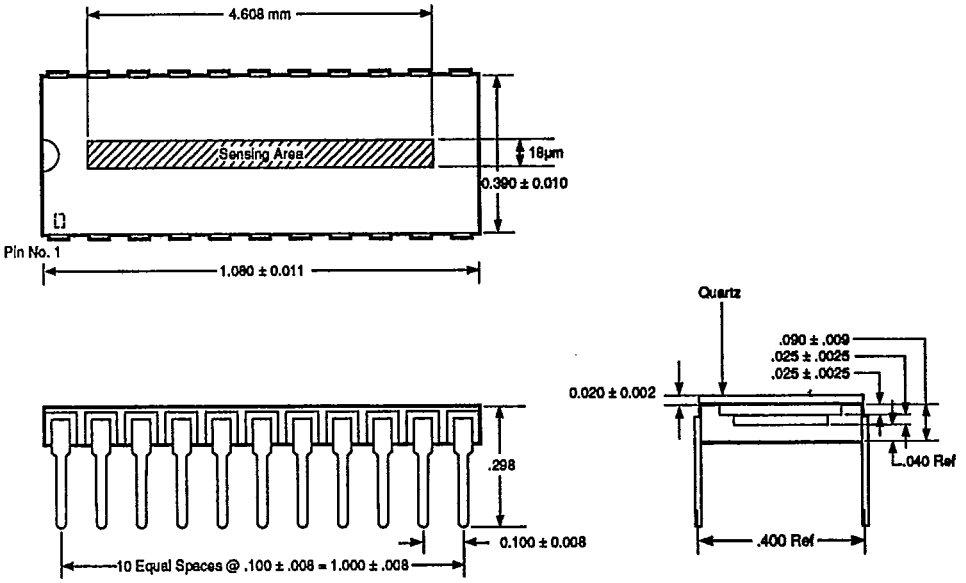
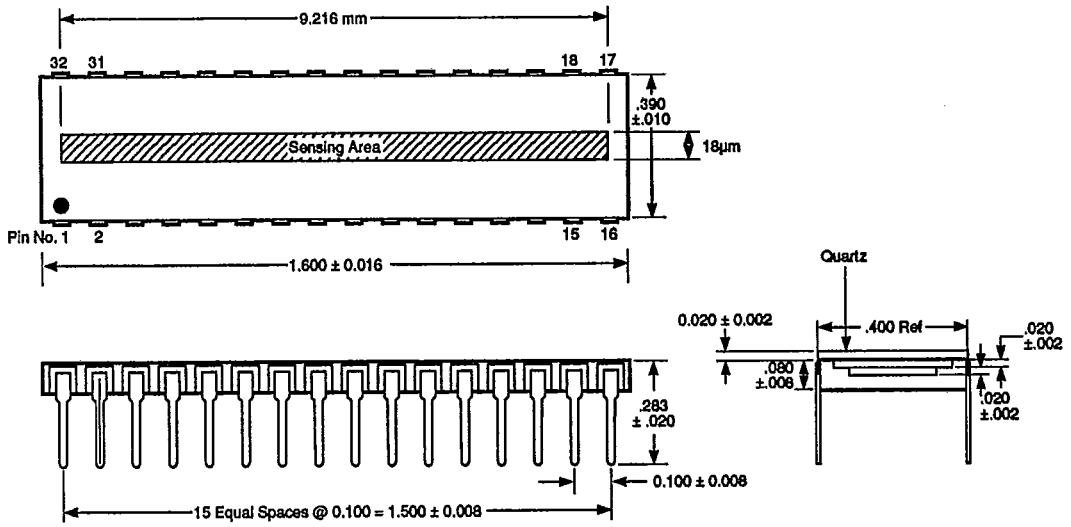
Package Dimensions RL1282D



Package Dimensions RL1284D



D Series Tapped

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Package Dimensions RL1288D

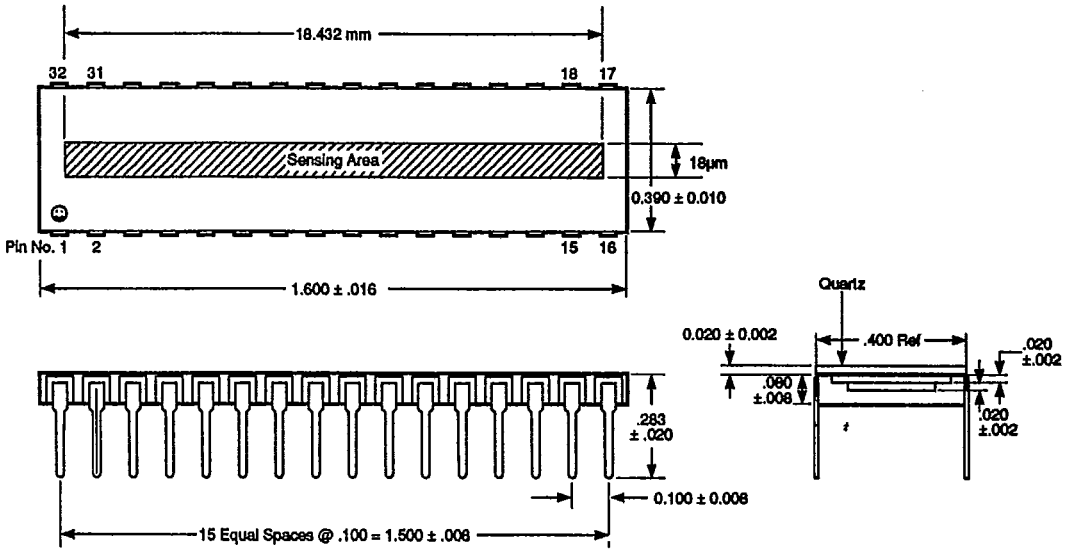

Figure 9. Package dimensions

Ordering Information *

Part Number	Evaluation Board
RL1282DAQ-011	No Board Available
RL1284DAQ-011	RC0716LNN-020
RL1288DAQ-011	RC0716LNN-011

* Includes standard devices. For options, consult EG&G Reticon sales offices.

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