PCKEL14

2.5 V/3.3 V PECL/ECL 1:5 clock distribution chip

Rev. 01 — 14 October 2002 **Product data**

1. Description

The PCKEL14 is a low skew 1:5 clock distribution chip designed explicitly for low skew clock distribution applications. The device can be driven by either a differential or single-ended ECL, or if positive power supplies are used, PECL input signal. The PCKEL14 is designed to operate in ECL or PECL mode for a voltage supply range of –2.375 V to –3.8 V (or 2.375 V to 3.8 V).

The PCKEL14 features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open and pulled LOW by the input pull-down resistor), the SEL pin will select the differential clock input.

The common enable ($\overline{EN}$) is synchronous, so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled, as can happen with an asynchronous control. The internal flip-flop is clocked on the falling edge of the input clock, therefore all associated specification limits are referenced to the negative edge of the clock input.

The V_{BB} pin (an internally generated voltage supply) is available to this device only. For single-ended conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC-coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.1 mA. When not used, V_{BB} should be left open.

2. Features

- 50 ps output-to-output skew at 3.3 V
- Synchronous enable/disable
- Multiplexed clock input
- ESD protection: > 2.5 kV HBM
- The PCK series contains temperature compensation
- PECL mode operating range: V_{CC} = 2.375 V to 3.8 V, with V_{EE} = 0 V
- NECL mode operating range: V_{CC} = 0 V, with V_{EE} = –2.375 V to –3.8 V
- Internal 75 kΩ pull-down resistors on all inputs, plus a 37.5 kΩ pull-up on $\overline{CLK}$
- Q output will default LOW with inputs open or at V_{EE}
- Meets or exceeds JEDEC spec EIA/JESD78 IC latch-up test
- Moisture sensitivity level 1
- Flammability rating: UL-94 code V-0 @ 1/8”

3. Pinning information

3.1 Pinning

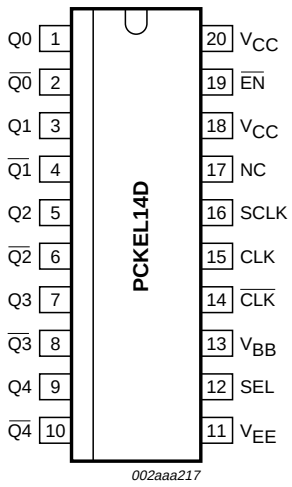


Fig 1. SO20 pin configuration.

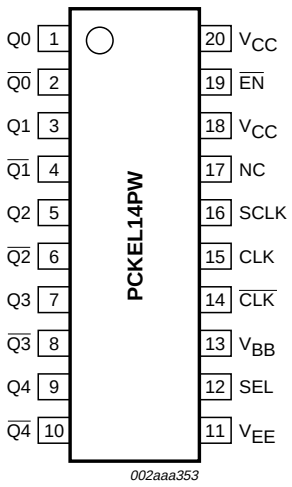


Fig 2. TSSOP pin configuration.

3.2 Pin description

Table 1: Pin description

Symbol	Pin	Description
Q0-Q4	1, 3, 5, 7, 9	ECL differential clock outputs, non-inverted
$\overline{Q0}$-$\overline{Q4}$	2, 4, 6, 8, 10	ECL differential clock outputs, inverted
V_{EE}	11	negative supply voltage
SEL	12	ECL clock select input
V_{BB}	13	reference voltage output
$\overline{CLK}$	14	ECL differential clock input, inverted
CLK	15	ECL differential clock input, non-inverted
SCLK	16	ECL scan clock input
NC	17	no connect
$\overline{EN}$	19	ECL synchronous enable, Active-LOW
V_{CC}	18, 20	positive supply voltage

3.2.1 Power supply connection

CAUTION

All V_{CC} and V_{EE} pins must be connected to an appropriate power supply to guarantee proper operation.

4. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
PCKEL14D	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
PCKEL14PW	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

5. Logic diagram

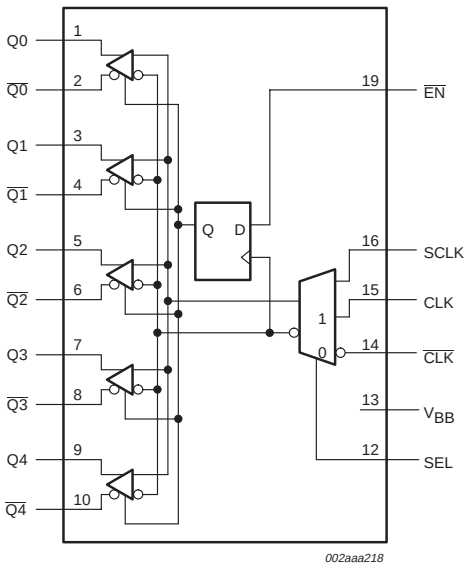


Fig 3. Logic diagram.

CAUTION

All V_{CC} and V_{EE} pins must be connected to an appropriate power supply to guarantee proper operation.

6. Function table

Table 3: Function table

X = Don't care.

CLK	SCLK	SEL	$\overline{EN}$	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L[1]

[1] On next negative transition of CLK or SCLK.

7. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	power supply	PECL mode; V_{EE} = 0 V	0	4.1	V
V_{EE}	power supply	NECL mode; V_{CC} = 0 V	0	–4.1	V
V_I	input voltage	PECL mode; V_{EE} = 0 V; $V_I \leq V_{CC}$	0	4.1	V
		NECL mode; V_{CC} = 0 V; $V_I \geq V_{EE}$	0	–4.1	V
I_o	output current	continuous	-	50	mA
		surge	-	100	mA
I_{BB}	V_{BB} sink/source		–0.1	+0.1	mA
T_{amb}	ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–65	+150	°C
$R_{th(j-a)}$	thermal resistance from junction to ambient	0 LFPM	-	90	°C/W
		500 LFPM	-	60	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case	std bd	30	35	°C/W
T_{sld}	soldering temperature	< 2 to 3 sec @ 248 °C	-	265	°C
ESDHBM	electrostatic discharge	Human Body Model; 1.5 kΩ; 100 pF	-	>2.50	kV
ESDMM	electrostatic discharge	Machine Model; 0 kΩ; 200 pF	-	>100	V
ESCCDM	electrostatic discharge	Charge Device Model	-	>1000	V

[1] Maximum ratings are those values beyond which device damage may occur.

8. Static characteristics

Table 5: PECL DC characteristics[1]

V_{CC} = 2.5 V; V_{EE} = 0 V [2]

Symbol	Parameter	Conditions	T_{amb} = −40 °C			T_{amb} = +25 °C			T_{amb} = +85 °C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	power supply current		-	28	40	-	30	40	-	31	42	mA
V_{OH}	HIGH-level output voltage	[3]	1325	1460	1620	1435	1545	1620	1475	1545	1620	mV
V_{OL}	LOW-level output voltage	[3]	670	805	945	690	795	880	690	795	880	mV
V_{IH}	HIGH-level input voltage	single-ended [4]	1310	-	1620	1335	-	1620	1335	-	1620	mV
V_{IL}	LOW-level input voltage	single-ended [4]	690	-	1025	690	-	1025	690	-	1025	mV
V_{BB}	output voltage reference		1.07	-	1.25	1.15	-	1.25	1.15	-	1.31	V
V_{IHCMR}	HIGH-level input voltage, common mode range (differential)	[5]	1.2	-	2.1	1.2	-	2.1	1.2	-	2.1	V
I_{IH}	HIGH-level input current		-	-	150	-	-	150	-	-	150	µA
I_{IL}	LOW-level input current	CLK	0.5	-	-	0.5	-	-	0.5	-	-	µA
		$\overline{CLK}$	−300	-	-	−300	-	-	−300	-	-	µA

[1] Devices are designed to meet the DC specifications shown in this table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 LFPM is maintained.

[2] Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.125 V to −1.3 V.

[3] All loading with 50 Ω to V_{CC} − 2 V.

[4] Do not use V_{BB} at V_{CC} < 3.0 V.

[5] $V_{IHCMR(min)}$ varies 1:1 with V_{EE}, $V_{IHCMR(max)}$ varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 6: Positive DC characteristics[1]

V_{CC} = 3.3 V; V_{EE} = 0 V [2]

Symbol	Parameter	Conditions	T_{amb} = −40 °C			T_{amb} = +25 °C			T_{amb} = +85 °C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	power supply current		-	32	40	-	32	40	-	34	42	mA
V_{OH}	HIGH-level output voltage	[3]	2125	2260	2420	2235	2345	2420	2275	2345	2420	mV
V_{OL}	LOW-level output voltage	[3]	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	HIGH-level input voltage	single-ended	2110	-	2420	2135	-	2420	2135	-	2420	mV
V_{IL}	LOW-level input voltage	single-ended	1490	-	1825	1490	-	1825	1490	-	1825	mV
V_{BB}	output voltage reference		1.87	-	2.05	1.95	-	2.05	1.95	-	2.11	V
V_{IHCMR}	HIGH-level input voltage, common mode range (differential)	V_{p-p} < 500 mV [4]	1.3	-	2.9	1.2	-	2.9	1.2	-	2.9	V
		$V_{p-p} \geq$ 500 mV	1.5	-	2.9	1.4	-	2.9	1.4	-	2.9	V
I_{IH}	HIGH-level input current		-	-	150	-	-	150	-	-	150	µA
I_{IL}	LOW-level input current	$\overline{CLK}$	−300	-	-	−300	-	-	−300	-	-	µA
		others	0.5	-	-	0.5	-	-	0.5	-	-	µA

[1] Devices are designed to meet the DC specifications shown in this table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 LFPM is maintained.

[2] Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.

[3] Outputs are terminated through a 50 Ω resistor to V_{CC} − 2V.

[4] $V_{IHCMR(min)}$ varies 1:1 with V_{EE}, $V_{IHCMR(max)}$ varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between $V_{p-p(min)}$ and 1 V.

Table 7: Negative DC characteristics[1]

V_{CC} = 0.0 V; V_{EE} = – 3.8 V to –2.375 V[2]

Symbol	Parameter	Conditions	T_{amb} = –40 °C			T_{amb} = +25 °C			T_{amb} = +85 °C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	power supply current		-	32	40	-	32	40	-	34	42	mA
V_{OH}	HIGH-level output voltage	[3]	–1175	–1040	–880	–1065	–955	–880	–1025	–955	–880	mV
V_{OL}	LOW-level output voltage	[3]	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	HIGH-level input voltage	single-ended	–1190	-	–880	–1165	-	–880	–1165	-	–880	mV
V_{IL}	LOW-level input voltage	single-ended	–1810	-	–1475	–1810	-	–1475	–1810	-	–1475	mV
V_{BB}	output voltage reference		–1.43	-	–1.25	–1.35	-	–1.25	–1.35	-	–1.19	V
V_{IHCMR}	HIGH-level input voltage, common mode range (differential)	V_{p-p} < 500 mV [4]	–2.0	-	–0.4	–2.1	-	–0.4	–2.1	-	–0.4	V
		$V_{p-p} \geq$ 500 mV	–1.8	-	–0.4	–1.9	-	–0.4	–1.9	-	–0.4	V
I_{IH}	HIGH-level input current		-	-	150	-	-	150	-	-	150	µA
I_{IL}	LOW-level input current	$\overline{CLK}$	–300	-	-	–300	-	-	–300	-	-	µA
		others	0.5	-	-	0.5	-	-	0.5	-	-	µA

[1] Devices are designed to meet the DC specifications shown in this table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 LFPM is maintained.

[2] Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.

[3] Outputs are terminated through a 50 Ω resistor to V_{CC} – 2 V.

[4] $V_{IHCMR(min)}$ varies 1:1 with V_{EE}, $V_{IHCMR(max)}$ varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between $V_{p-p(min)}$ and 1 V.

9. Dynamic characteristics

Table 8: AC characteristics

(V_{CC} = 2.375 V to 3.8 V; V_{EE} = 0 V) or (V_{CC} = 0 V; V_{EE} = −2.375 V to −3.8 V) [1]

Symbol	Parameter	Conditions	T_{amb} = −40 °C			T_{amb} = +25 °C			T_{amb} = +85 °C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	maximum toggle frequency	see Figure 4	-	> 1	-	-	> 1	-	-	> 1	-	GHz
t_{PLH}	LOW-to-HIGH propagation delay	CLK to Q (diff); 3.3 V	400	-	720	450	-	780	475	-	830	ps
		CLK to Q (diff); 2.5 V	400	-	800	450	-	940	500	-	970	ps
t_{PHL}	HIGH-to-LOW propagation delay	CLK to Q (SE)	330	-	770	350	680	830	370	-	880	ps
		SCLK to Q	330	-	770	350	680	830	370	-	880	ps
t_{SKEW}	skew time	part-to-part	-	-	200	-	-	200	-	-	200	ps
		within-device; 3.3 V [2]	-	-	50	-	-	50	-	-	50	ps
		within-device; 2.5 V [2]	-	-	70	-	-	70	-	-	70	ps
t_{JITTER}	cycle-to cycle jitter		-	0.2	< 1	-	0.2	< 1	-	0.2	< 1	ps
t_{su}	$\overline{EN}$ set-up time		0	-	-	0	-	-	0	-	-	ps
t_h	$\overline{EN}$ hold time		0	-	-	0	-	-	0	-	-	ps
$V_{i(p-p)}$	input swing CLK	[3]	150	-	1000	150	-	1000	150	-	1000	mV
t_r/t_f	output rise/fall times	Q pins (20% - 80%); 3.3 V	230	-	500	230	-	500	230	-	500	ps
		Q pins (20% - 80%); 2.5 V	230	-	600	230	-	600	230	-	625	ps

[1] V_{EE} can vary ±0.3 V.

[2] Skews are specified for identical LOW-to-HIGH or HIGH-to-LOW transitions.

[3] $V_{i(p-p)(min)}$ is minimum input swing for which AC parameters are guaranteed.

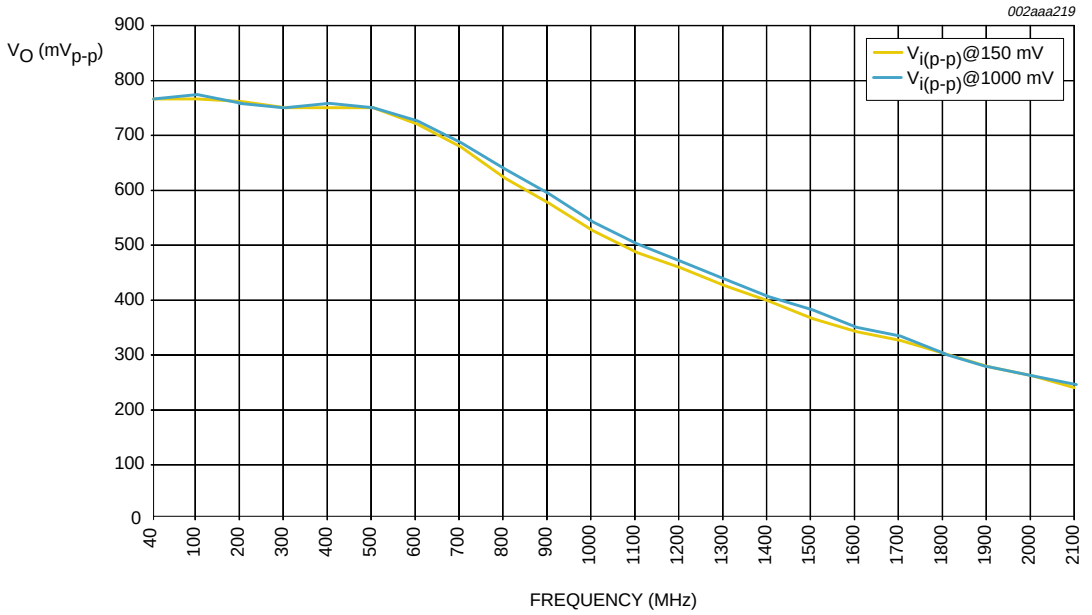
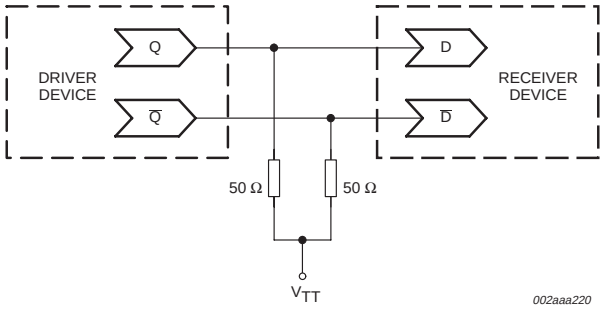


Fig 4. f_{max} @ 150 mV and 1000 mV input.

10. Application information

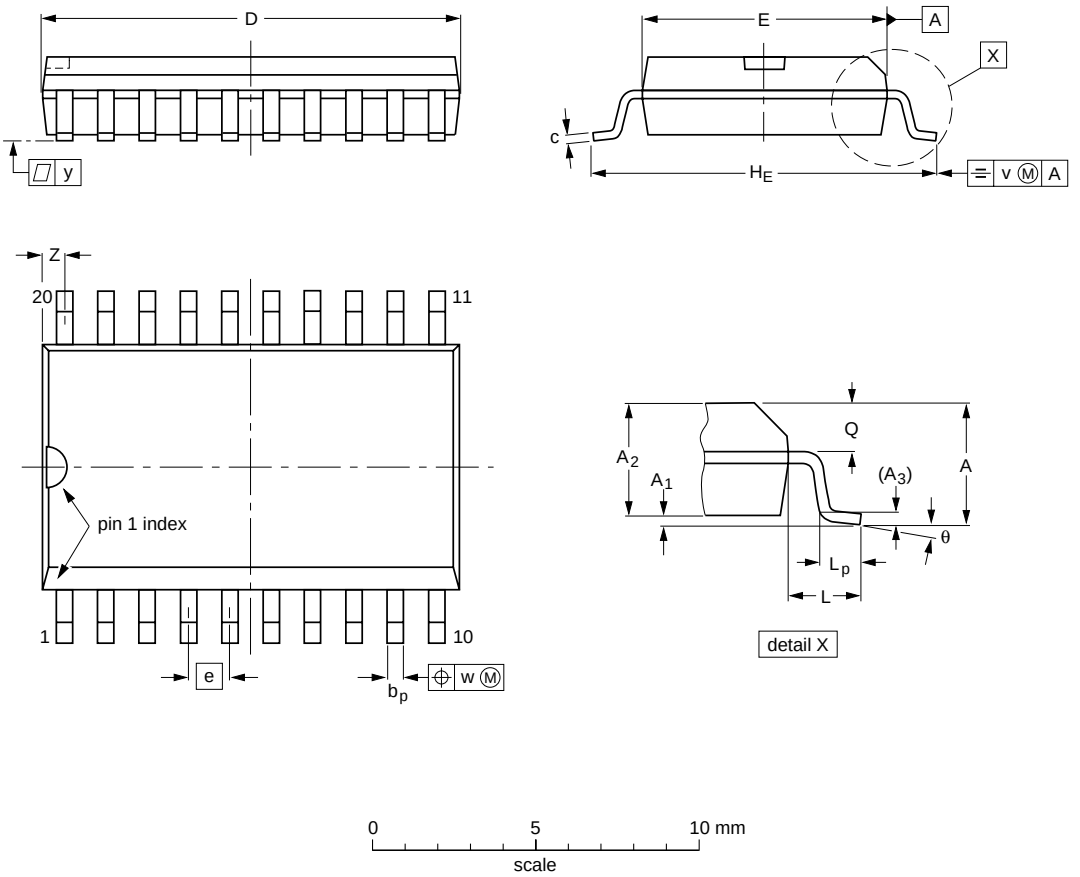


$V_{TT} = V_{CC} - 2.0$ V.

Fig 5. Typical termination for output driver and device evaluation.

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

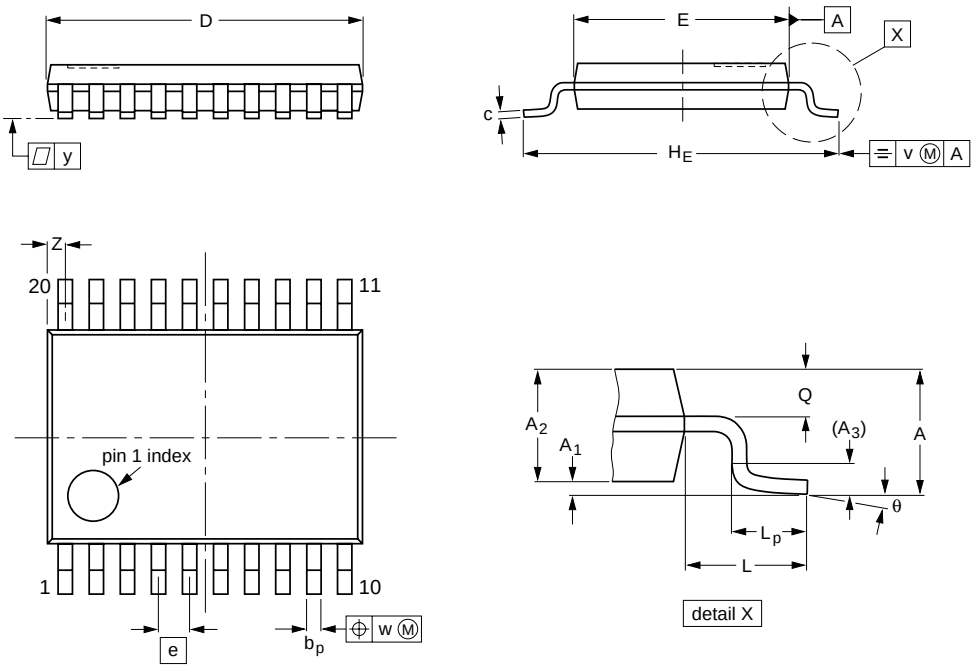
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013				~~97-05-22~~ 99-12-27

Fig 6. SO20 package outline (SOT163-1).

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153				~~95-02-04~~ 99-12-27

Fig 7. TSSOP20 package outline (SOT360-1).

12. Soldering

12.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

12.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C small/thin packages.

12.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

12.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

12.5 Package related soldering information

Table 9: Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	Soldering method	
	Wave	Reflow[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO	not recommended[6]	suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[4] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[5] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[6] Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

13. Revision history

Table 10: Revision history

Rev	Date	CPCN	Description
01	20021014	-	**Product data; initial version (9397 750 09564).** Engineering Change Notice 853-2372 2877 (date: 20020909).

14. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

15. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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