Non-Linear High Speed Termination IC

Features

- 16 channel, dual rail clamping action in a single package
- Provides bus termination independent of line impedance or loading conditions
- Uses CAMD's patented EZterm™ technology
- 24-pin QSOP package saves board space and eases layout in space critical areas.
- One IC replaces and outperforms up to 32 discrete components.
- Enable pin included

Applications

- High speed, low voltage buses

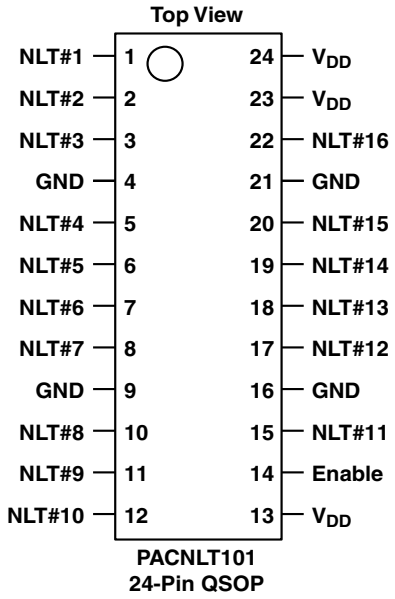
Product Description

CAMD's non-linear termination IC is specifically designed to minimize overshoot/undershoot disturbances caused by impedance mismatch reflections and noise on high-speed transmission lines.

Reflections on high-speed data lines lead to voltage overshoot and understoot disturbances, which may result in data loss or improper system operation. Resistive terminations, when used to terminate these high-speed data lines, increase power consumption and degrade output levels, resulting in reduced noise immunity. Clamping-type termination is the best overall solution for applications in which these may be considerations.

This highly integrated non-linear termination IC provides very effective termination performance for high-speed data lines under variable loading conditions. The device supports up to 16 terminated lines per package – each of which are clamped to both ground and power supply rail. A typical application may use 4 devices to replace (and outperform) 64 conventional Schottky diode pairs; thus providing significant reductions in component and assembly costs, improvements in manufacturing efficiency and reliability, and savings in allocated board area for space-critical designs.

Pin Configuration



PACNLT101
24-Pin QSOP

Standard Part Ordering Information

Package		Ordering Part Number	
Pin	Style	Tape & Reel	Part Marking
24	QSOP	PACNLT101Q	PACNLT101Q

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215 Topaz Street, Milpitas, California 95035 ▲ Tel: (408) 263-3214 ▲ Fax: (408) 263-7846 ▲ www.calmicro.com

Absolute Maximum Ratings		
Parameter	**Rating**	**Unit**
Maximum DC Voltage on any pin	3.6	V
Minimum DC Voltage on any pin	–0.5	V
Continuous current per channel	72	mA
Operating Temperature (Ambient)	0 to 70	°C
Storage Temperature (Ambient)	–65 to 150	°C
Power Dissipation @ T = 25°C	0.9	W

Operating Characterisitcs - 3.3V: Temperature rated at 0°C to 70°C, V_{DD} Enable rated 3.3V ± 0.3V

Operating Characteristics — 3.3V			
Parameter	**Conditions**	**TYP**	**UNIT**
Signal Voltage	above V_{DD} @ I = 50mA	610	mV
	below GND @ I = 50mA	510	mV
V_{DD} current	all Channels floating	69	mA
Enable pin (pin 14) current	all Channels floating	8	mA
Input Capacitance*	Signal voltage = V_{DD}	3.4	pF
	Signal voltage = $V_{DD/2}$	3.0	pF
ESD protection	MIL-STD-883, method 3015*	4	kV

*These parameters are guaranteed by design and characterization.

Operating Characterisitcs - 2.0V: Temperature rated at 0°C to 70°C, V_{DD} Enable rated 2.0V ± 0.2V

Operating Characteristics — 2.0V			
Parameter	**Conditions**	**TYP**	**UNIT**
Signal Voltage	above V_{DD} @ I = 20mA	390	mV
	below GND @ I = 20mA	300	mV
V_{DD} current	all Channels floating	21	mA
Enable pin (pin 14) current	all Channels floating	3.5	mA
Input Capacitance*	Signal voltage = V_{DD}	3.5	pF
	Signal voltage = $V_{DD/2}$	3.2	pF
ESD protection	MIL-STD-883, method 3015*	4	kV

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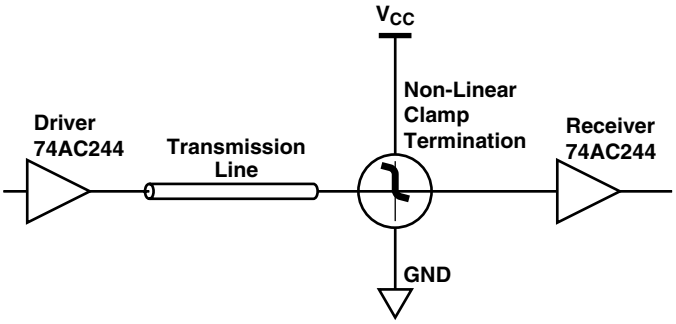

Figure 1. Example Circuit: Single-Driver/Single Receiver

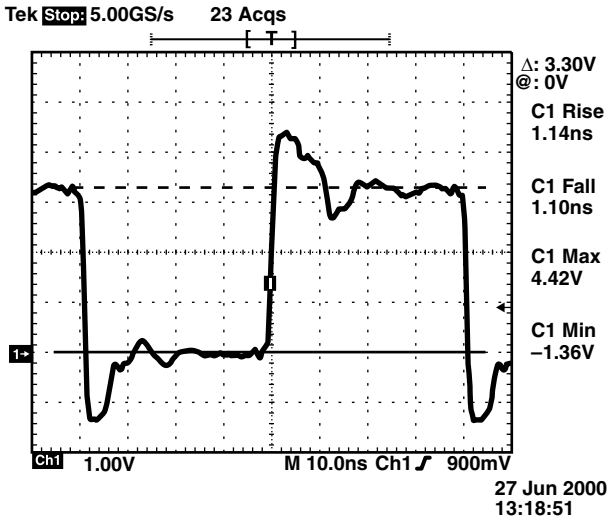

Figure 2. 74AC244 Termination Only

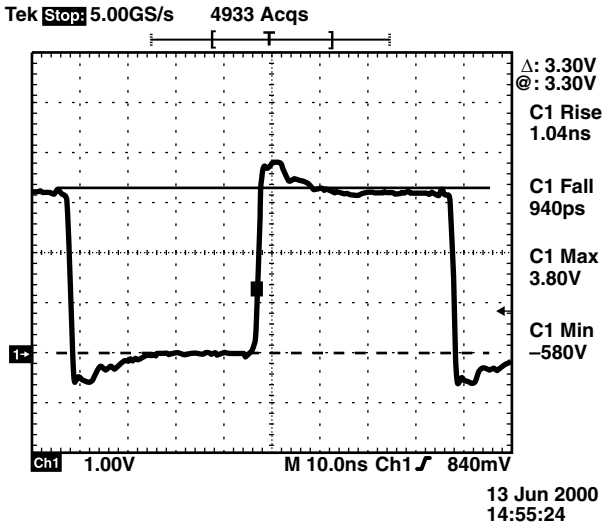

Figure 3. With PACNLT101 Termination

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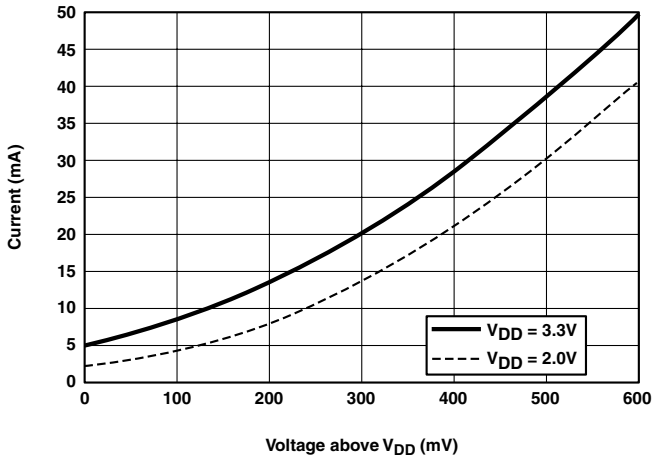

Figure 4. DC I-V Curves for V_{DD} = 2V and V_{DD} = 3.3V

Application Information

Figure 5 shows one method of configuring the printed circuit board such that all 16 terminated signals are easily accessible. The decoupling capacitor should be a high-frequency type, 0.1µF or larger, and placed as close to the IC as possible. This will minimize the positive overshoot voltage and also reduce EMI emissions. It should be noted that for optimum performance the PACNLT101 termination should be located as physically close to the receiving IC input as is possible.

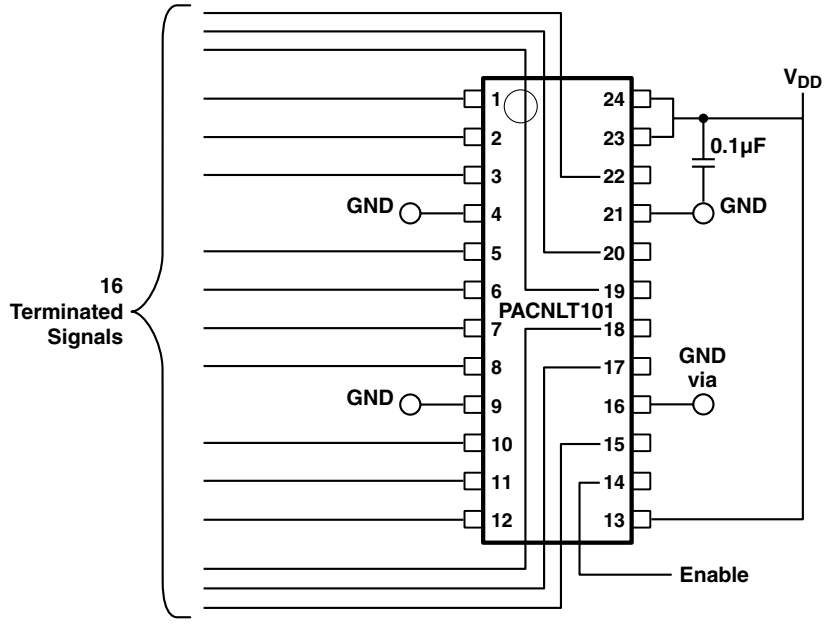

Figure 5. Printed Circuit Board with Accessible Configuration for 16 Terminated Signals

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Enable pin

The Enable pin has a dual function. If forced to ground or set to high impedance it will greatly reduce the supply current of the PACNLT101.

The Enable pin can also be used to vary the supply current and clamping voltage. As the current into the Enable pin is increased the supply current will increase and the clamping voltage will be reduced. The minimum clamping voltage will occur when the Enable pin voltage equals the supply voltage. (The Enable pin voltage cannot exceed the supply voltage.)

Users who cannot tolerate the supply current quoted in the Operating Characteristics can connect a resistor in series with the Enable pin to reduce the supply current, at the cost of increasing the clamping voltage. See Figure 6.

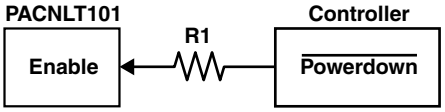

Figure 6. Resistor In Series with the Enable Pin

The controller IC sets the powerdown pin to 0V to depower the PACNLT101, and sets the powerdown pin to V_{DD} to power up the PACNLT101. The system designer can vary the value of R1 to optimize the trade-off between power consumption and clamping voltage. See Figure 7 and Figure 8.

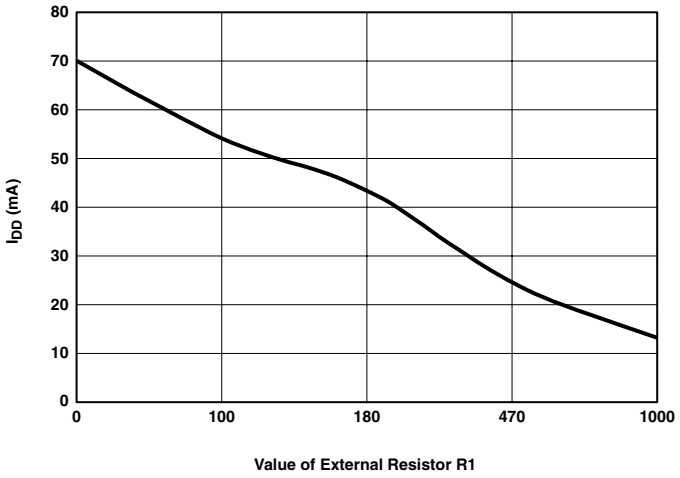

Figure 7. Variation I_{DD} with R1

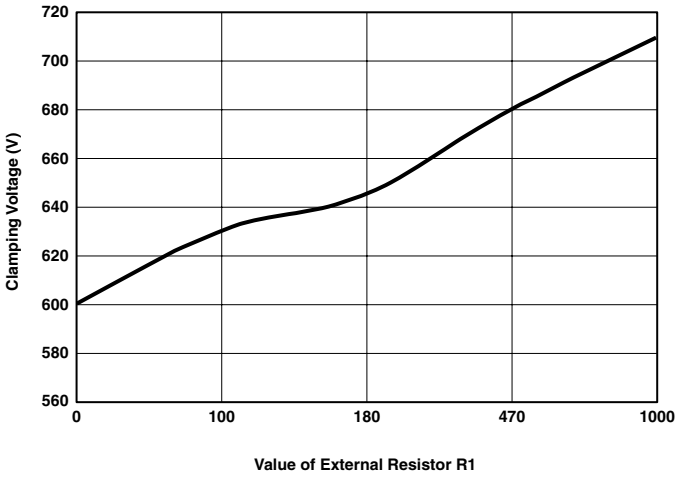

Figure 8. Variation of Clamping Voltage with R1

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