PA10 • PA10A

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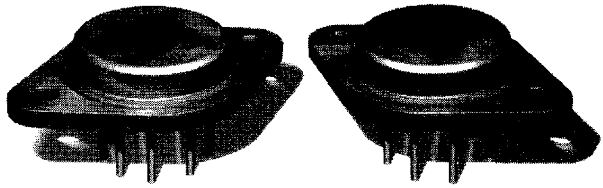
FEATURES

- GAIN BANDWIDTH PRODUCT — 4MHz
- TEMPERATURE RANGE — −55 to +125°C (PA10A)
- EXCELLENT LINEARITY — Class A/B Output
- WIDE SUPPLY RANGE — ±10V to ±50V
- HIGH OUTPUT CURRENT — ±5A Peak



APPLICATIONS

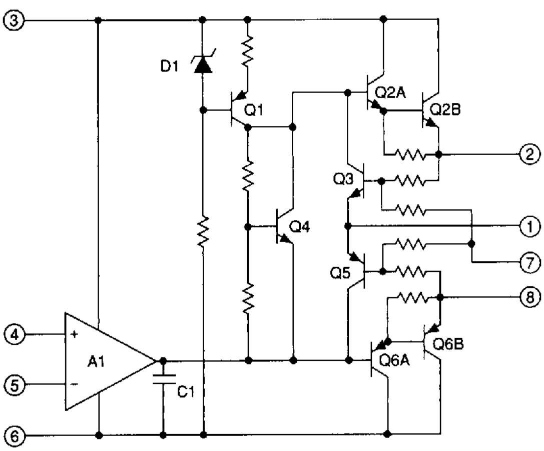
- MOTOR, VALVE AND ACTUATOR CONTROL
- MAGNETIC DEFLECTION CIRCUITS UP TO 4A
- POWER TRANSDUCERS UP TO 100kHz
- TEMPERATURE CONTROL UP TO 180W
- PROGRAMMABLE POWER SUPPLIES UP TO 90V
- AUDIO AMPLIFIERS UP TO 60W RMS

DESCRIPTION

The PA10 and PA10A are high voltage, high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. For optimum linearity, the output stage is biased for class A/B operation. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limiting resistors. Both amplifiers are internally compensated for all gain settings. For continuous operation under load, a heatsink of proper rating is recommended.

This hybrid integrated circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers voids the warranty.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATION

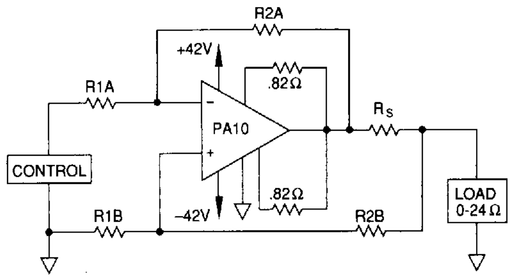
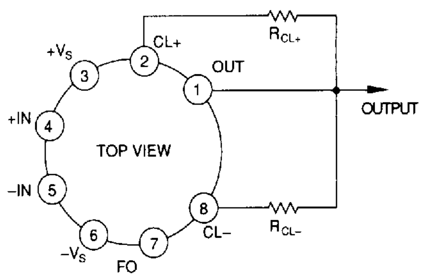


FIGURE 1. VOLTAGE-TO-CURRENT CONVERSION

DC and low distortion AC current waveforms are delivered to a grounded load by using matched resistors (A and B sections) and taking advantage of the high common mode rejection of the PA10.

Foldover current limit is used to modify current limits based on output voltage. When load resistance drops to 0, the current is limited based on output voltage. When load resistance drops to 0, the current limit is 0.79A resulting in an internal dissipation of 33.3 W. When output voltage increases to 36V, the current limit is 1.69A. Refer to Application Note 9 on foldover limiting for details.

EXTERNAL CONNECTIONS



PA10 • PA10A

ABSOLUTE MAXIMUM RATINGS
SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	100V
OUTPUT CURRENT, within SOA	5A
POWER DISSIPATION, internal	67W
INPUT VOLTAGE, differential	$\pm V_S$ –3V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[1]	200°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

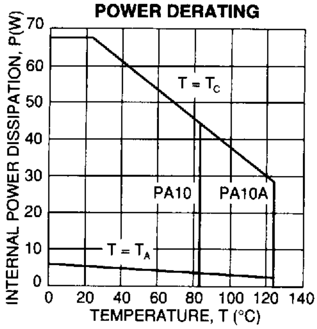
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2, 5]	PA10 MIN	PA10 TYP	PA10 MAX	PA10A MIN	PA10A TYP	PA10A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±2	±6		±1	±3	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		±10	±65		*	±40	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		±30	±200		*	*	µV/V
OFFSET VOLTAGE, vs. power	T_C = 25°C		±20			*		µVW
BIAS CURRENT, initial	T_C = 25°C		12	30		10	20	nA
BIAS CURRENT, vs. temperature	Full temperature range		±50	±500		*	*	pA/°C
BIAS CURRENT, vs. supply	T_C = 25°C		±10			*		pA/V
OFFSET CURRENT, initial	T_C = 25°C		±12	±30		±5	±10	nA
OFFSET CURRENT, vs. temperature	Full temperature range		±50			*		pA/°C
INPUT IMPEDANCE, DC	T_C = 25°C		200			*		MΩ
INPUT CAPACITANCE	T_C = 25°C		3			*		pF
COMMON MODE VOLTAGE RANGE[3]	Full temperature range	$\pm V_S$–5	$\pm V_S$–3		*	*		V
COMMON MODE REJECTION, DC[3]	Full temp. range, $V_{CM} = \pm V_S$ –6V	74	100		*	*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	T_C = 25°C, 1KΩ load		110			*		dB
OPEN LOOP GAIN at 10Hz	Full temp. range, 15Ω load	96	108		*	*		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	T_C = 25°C, 15Ω load		4			*		MHz
POWER BANDWIDTH	T_C = 25°C, 15Ω load	10	15		*	*		kHz
PHASE MARGIN	Full temp. range, 15Ω load		20			*		°
OUTPUT								
VOLTAGE SWING[3]	T_C = 25°C, I_O = 5A	$\pm V_S$–8	$\pm V_S$–5		$\pm V_S$–6	*		V
VOLTAGE SWING[3]	Full temp. range, I_O = 2A	$\pm V_S$–6			*			V
VOLTAGE SWING[3]	Full temp. range, I_O = 80mA	$\pm V_S$–5			*			V
CURRENT, peak	T_C = 25°C	5			*			A
SETTLING TIME to .1%	T_C = 25°C, 2V step		2			*		µs
SLEW RATE	T_C = 25°C	2	3		*	*		V/µs
CAPACITIVE LOAD	Full temperature range, A_V = 1			.68			*	nF
CAPACITIVE LOAD	Full temperature range, A_V = 2.5			10			*	nF
CAPACITIVE LOAD	Full temperature range, A_V > 10			SOA			*	nF
POWER SUPPLY								
VOLTAGE	Full temperature range	±10	±40	±45	*	*	±50	V
CURRENT, quiescent	T_C = 25°C	8	15	30	*	*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[4]	T_C = –55 to +125°C, F > 60Hz		1.9	2.1		*	*	°C/W
RESISTANCE, DC, junction to case	T_C = –55 to +125°C		2.4	2.6		*	*	°C/W
RESISTANCE, junction to air	T_C = –55 to +125°C		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	–55		+125	°C

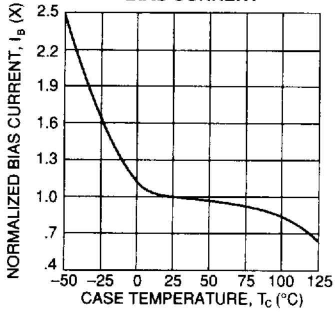
NOTES:
* The specification of PA10A is identical to the specification for PA10 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all tests is ±40, unless otherwise noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Full temperature range specifications are guaranteed but not tested.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

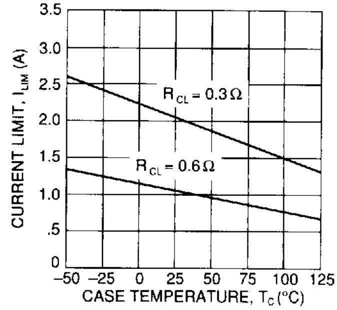
POWER DERATING



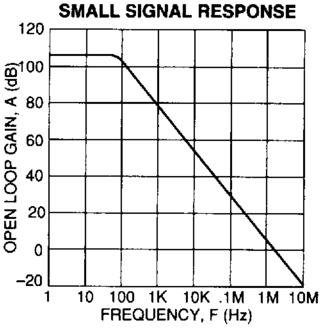
BIAS CURRENT



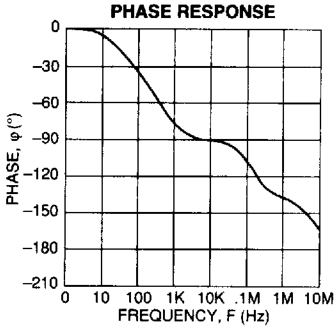
CURRENT LIMIT



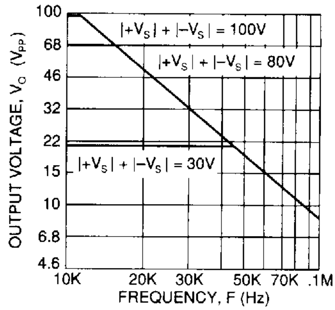
SMALL SIGNAL RESPONSE



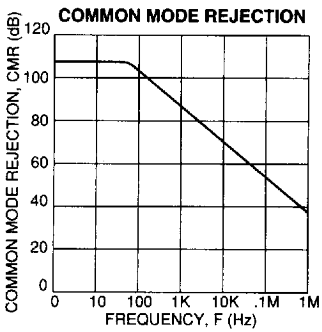
PHASE RESPONSE



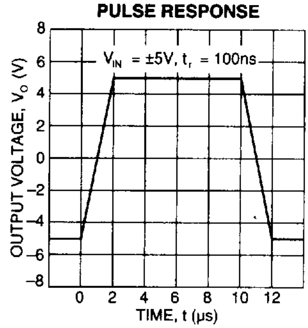
POWER RESPONSE



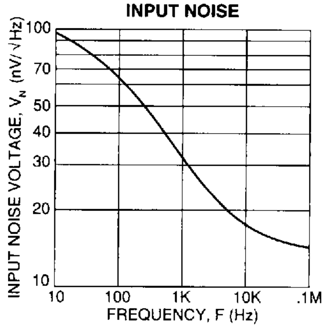
COMMON MODE REJECTION



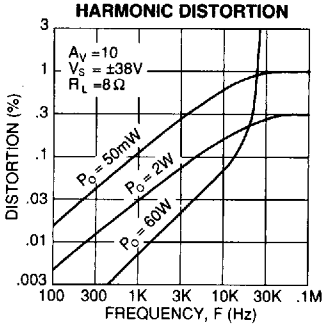
PULSE RESPONSE



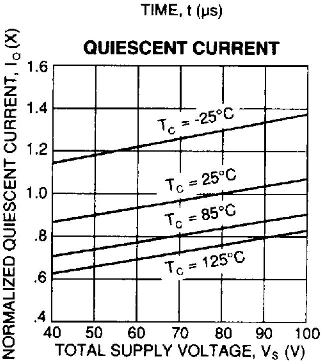
INPUT NOISE



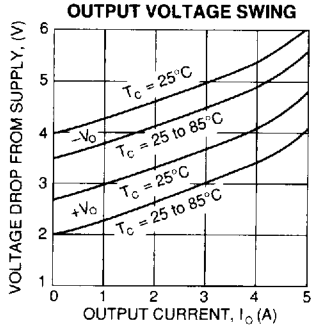
HARMONIC DISTORTION



QUIESCENT CURRENT



OUTPUT VOLTAGE SWING



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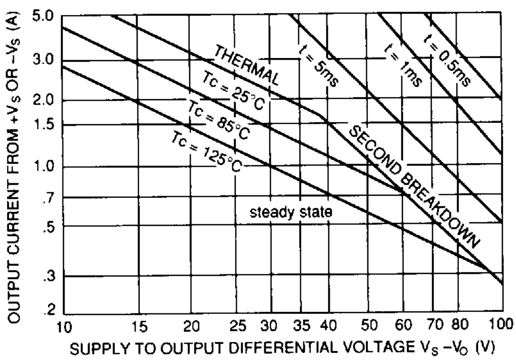
GENERAL

Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the data book.

SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has three distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.



The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts.

1. Capacitive and dynamic* inductive loads up to the following maximum are safe with the current limits set as specified.

	CAPACITIVE LOAD		INDUCTIVE LOAD	
$\pm V_S$	$I_{LIM} = 2A$	$I_{LIM} = 5A$	$I_{LIM} = 2A$	$I_{LIM} = 5A$
50V	80µF	75µF	55mH	7.5mH
40V	250µF	150µF	150mH	11mH
35V	500µF	250µF	200mH	15mH
30V	1,200µF	500µF	250mH	24mH
25V	4,000µF	1,600µF	400mH	38mH
20V	20,000µF	5,000µF	1,500mH	75mH
15V	**	25,000µF	**	100mH

*If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 8V below the supply rail with I_{LIM} = 5A or 20V below the supply rail with I_{LIM} = 2A while the amplifier is current limiting, the inductor must be capacitively coupled or the current limit must be lowered to meet SOA criteria.

**Second breakdown effect imposes no limitation but thermal limitations must still be observed.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rail or shorts to common if the current limits are set as follows at T_C = 85°C:

$\pm V_S$	SHORT TO $\pm V_S$ C, L, OR EMF LOAD	SHORT TO COMMON
50V	.26A	.84A
40V	.38A	1.1A
35V	.49A	1.2A
30V	.65A	1.4A
25V	.84A	1.7A
20V	1.1A	2.2A
15V	1.4A	2.9A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

CURRENT LIMITING

Refer to Application Note 9, "Current Limiting", for details of both fixed and foldover current limit operation. Visit the Apex web site at www.apexmicrotech.com for a copy of llimit.xls which plots current limits vs. steady state SOA. Beware that current limit should be thought of as a +/–20% function initially and varies about 2:1 over the range of –55°C to 125°C.

For fixed current limit, leave pin 7 open and use equations 1 and 2.

$$R_{CL} = 0.65/L_{CL} \quad (1)$$

$$I_{CL} = 0.65/R_{CL} \quad (2)$$

Where:
I_{CL} is the current limit in amperes.
R_{CL} is the current limit resistor in ohms.

For certain applications, foldover current limit adds a slope to the current limit which allows more power to be delivered to the load without violating the SOA. For maximum foldover slope, ground pin 7 and use equations 3 and 4.

$$I_{CL} = \frac{0.65 + (Vo * 0.014)}{R_{CL}} \quad (3)$$

$$R_{CL} = \frac{0.65 + (Vo * 0.014)}{I_{CL}} \quad (4)$$

Where:
Vo is the output voltage in volts.

Most designers start with either equation 1 to set R_{CL} for the desired current at 0v out, or with equation 4 to set R_{CL} at the maximum output voltage. Equation 3 should then be used to plot the resulting foldover limits on the SOA graph. If equation 3 results in a negative current limit, foldover slope must be reduced. This can happen when the output voltage is the opposite polarity of the supply conducting the current.

In applications where a reduced foldover slope is desired, this can be achieved by adding a resistor (R_{FO}) between pin 7 and ground. Use equations 4 and 5 with this new resistor in the circuit.

$$I_{CL} = \frac{0.65 + \dfrac{Vo * 0.14}{10.14 + R_{FO}}}{R_{CL}} \quad (5)$$

$$R_{CL} = \frac{0.65 + \dfrac{Vo * 0.14}{10.14 + R_{FO}}}{I_{CL}} \quad (6)$$

Where:
R_{FO} is in K ohms.

TABLE 4 GROUP A INSPECTION

PA10M

APEX MICROTECHNOLOGY

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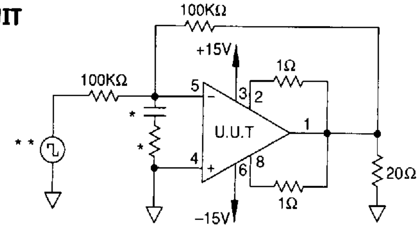
SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent current	I_Q	25°C	±40V	$V_{IN} = 0$, $A_V = 100$, $R_{CL} = .1\Omega$		30	mA
1	Input offset voltage	V_{OS}	25°C	±40V	$V_{IN} = 0$, $A_V = 100$		±6	mV
1	Input offset voltage	V_{OS}	25°C	±10V	$V_{IN} = 0$, $A_V = 100$		±12	mV
1	Input offset voltage	V_{OS}	25°C	±45V	$V_{IN} = 0$, $A_V = 100$		±7	mV
1	Input bias current, +IN	$+I_B$	25°C	±40V	$V_{IN} = 0$		±30	nA
1	Input bias current, –IN	$-I_B$	25°C	±40V	$V_{IN} = 0$		±30	nA
1	Input offset current	I_{OS}	25°C	±40V	$V_{IN} = 0$		±30	nA
3	Quiescent current	I_Q	–55°C	±40V	$V_{IN} = 0$, $A_V = 100$, $R_{CL} = .1\Omega$		75	mA
3	Input offset voltage	V_{OS}	–55°C	±40V	$V_{IN} = 0$, $A_V = 100$		±11.2	mV
3	Input offset voltage	V_{OS}	–55°C	±10V	$V_{IN} = 0$, $A_V = 100$		±17.2	mV
3	Input offset voltage	V_{OS}	–55°C	±45V	$V_{IN} = 0$, $A_V = 100$		±12.2	mV
3	Input bias current, +IN	$+I_B$	–55°C	±40V	$V_{IN} = 0$		±115	nA
3	Input bias current, –IN	$-I_B$	–55°C	±40V	$V_{IN} = 0$		±115	nA
3	Input offset current	I_{OS}	–55°C	±40V	$V_{IN} = 0$		±115	nA
2	Quiescent current	I_Q	125°C	±40V	$V_{IN} = 0$, $A_V = 100$, $R_{CL} = .1\Omega$		30	mA
2	Input offset voltage	V_{OS}	125°C	±40V	$V_{IN} = 0$, $A_V = 100$		±12.5	mV
2	Input offset voltage	V_{OS}	125°C	±10V	$V_{IN} = 0$, $A_V = 100$		±18.5	mV
2	Input offset voltage	V_{OS}	125°C	±45V	$V_{IN} = 0$, $A_V = 100$		±13.5	mV
2	Input bias current, +IN	$+I_B$	125°C	±40V	$V_{IN} = 0$		±70	nA
2	Input bias current, –IN	$-I_B$	125°C	±40V	$V_{IN} = 0$		±70	nA
2	Input offset current	I_{OS}	125°C	±40V	$V_{IN} = 0$		±70	nA
4	Output voltage, $I_O = 5A$	V_O	25°C	±18V	$R_L = 2.07\Omega$	10		V
4	Output voltage, $I_O = 80mA$	V_O	25°C	±45V	$R_L = 500\Omega$	40		V
4	Output voltage, $I_O = 2A$	V_O	25°C	±30V	$R_L = 12\Omega$	24		V
4	Current limits	I_{CL}	25°C	±17V	$R_L = 12\Omega$, $R_{CL} = 1\Omega$	.6	.89	A
4	Stability/noise	E_N	25°C	±40V	$R_L = 500\Omega$, $A_V = 1$, $C_L = .68nF$		1	mV
4	Slew rate	SR	25°C	±40V	$R_L = 500\Omega$	2	10	V/µs
4	Open loop gain	A_{OL}	25°C	±40V	$R_L = 500\Omega$, F = 10Hz	96		dB
4	Common mode rejection	CMR	25°C	±15V	$R_L = 500\Omega$, F = DC, $V_{CM} = \pm 9V$	74		dB
6	Output voltage, $I_O = 5A$	V_O	–55°C	±18V	$R_L = 2.07\Omega$	10		V
6	Output voltage, $I_O = 80mA$	V_O	–55°C	±45V	$R_L = 500\Omega$	40		V
6	Output voltage, $I_O = 2A$	V_O	–55°C	±30V	$R_L = 12\Omega$	24		V
6	Stability/noise	E_N	–55°C	±40V	$R_L = 500\Omega$, $A_V = 1$, $C_L = .68nF$		1	mV
6	Slew rate	SR	–55°C	±40V	$R_L = 500\Omega$	2	10	V/µs
6	Open loop gain	A_{OL}	–55°C	±40V	$R_L = 500\Omega$, F = 10Hz	96		db
6	Common mode rejection	CMR	–55°C	±15V	$R_L = 500\Omega$, F = DC, $V_{CM} = \pm 9V$	74		dB
5	Output voltage, $I_O = 3A$	V_O	125°C	±14.3V	$R_L = 2.07\Omega$	6.3		V
5	Output voltage, $I_O = 80mA$	V_O	125°C	±45V	$R_L = 500\Omega$	40		V
5	Output voltage, $I_O = 2A$	V_O	125°C	±30V	$R_L = 12\Omega$	24		V
5	Stability/noise	E_N	125°C	±40V	$R_L = 500\Omega$, $A_V = 1$, $C_L = .68nF$		1	mV
5	Slew rate	SR	125°C	±40V	$R_L = 500\Omega$	2	10	V/µs
5	Open loop gain	A_{OL}	125°C	±40V	$R_L = 500\Omega$, F = 10Hz	96		dB
5	Common mode rejection	CMR	125°C	±15V	$R_L = 500\Omega$, F = DC, $V_{CM} = \pm 9V$	74		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

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