Product Preview

Medium Power Surface Mount Products

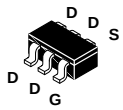
TMOS™ Field Effect Transistor

P–Channel Enhancement–Mode MOSFET

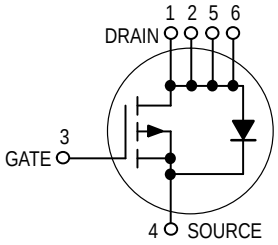
MGSF2P02HD

POWER MOSFET
P–CHANNEL
1.3 AMPERES
20 VOLTS
$R_{DS(on)}$ = 175 mOHMS

This device represents a series of power MOSFETs which utilizes Motorola's High Cell Density HDTMOS process to achieve the lowest on–resistance per silicon area. The series of products are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. These devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.



CASE 318G–01, Style 1
TSOP 6 PLASTIC



- Miniature TSOP6 Surface Mount Package — Saves Board Space
- Low Profile for Thin Applications such as PCMCIA Cards
- Very Low $R_{DS(on)}$ Provides Higher Efficiency and Expands Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Diode is Characterized for Use in Bridge Circuits
- Diode Exhibits High Speed, with Soft Recovery
- I_{DSS} Specified at Elevated Temperatures
- Avalanche Energy Specified
- Package Mounting Information Provided

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	20	V
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	20	V
Gate–to–Source Voltage	V_{GS}	±9	V
Drain Current — Continuous	I_D	1.3	A
— Single Pulse ($t_p \le 10$ μs)	I_{DM}	10	
Total Power Dissipation @ T_C = 25°C	P_D	400	mW
Total Power Dissipation @ T_C = 85°C	P_D	210	mW
Thermal Resistance — Junction to Ambient (1)	$R_{\theta JA}$	312	°C/W
Drain Current — Continuous	I_D	2.9	A
— Single Pulse ($t_p \le 10$ μs)	I_{DM}	15	
Total Power Dissipation @ T_C = 25°C	P_D	2.0	W
Total Power Dissipation @ T_C = 85°C	P_D	1.0	W
Thermal Resistance — Junction to Ambient (2)	$R_{\theta JA}$	62.5	°C/W
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C

Single Pulse Drain Source Avalanche Energy V_{DD} = 20 V, V_{GS} = 4.5 Vpk, I_L = 3.6 Apk, L = 25 mH, R_G = 25 Ω	E_{AS}	160	mJ

THERMAL CHARACTERISTICS

Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 5 seconds	T_L	260	°C

(1) Minimum FR–4 or G–10 PCB, Operating to Steady State.
(2) Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz. Cu 0.06″ thick single sided), Operating time ≤5 seconds.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

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Thermal Clad is a trademark of the Bergquist Company.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)		$V_{(BR)DSS}$	20	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	1.0 10	μA
Gate–to–Source Leakage Current (V_{GS} = ±9.0 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	±100	nAdc
ON CHARACTERISTICS						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	0.7 —	0.95 2.2	1.4 —	Vdc mV/°C
Drain–to–Source On–Voltage (V_{GS} = 4.5 Vdc, I_D = 1.3 Adc) (VGS = 2.7 Vdc, I_D = 0.8 Adc)		$R_{DS(on)}$	— —	145 220	175 280	mΩ
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 0.6 Adc)		g_{FS}	1.3	2.0	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 15 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	225	—	pF
Output Capacitance		C_{oss}	—	150	—	
Transfer Capacitance		C_{rss}	—	60	—	
SWITCHING CHARACTERISTICS						
Turn–On Delay Time	(V_{DS} = 10 Vdc, I_D = 1.2 Adc, V_{GS} = 4.5 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	—	15	—	nsec
Rise Time		t_r	—	27	—	
Turn–Off Delay Time		$t_{d(off)}$	—	60	—	
Fall Time		t_f	—	72	—	
Turn–On Delay Time	(V_{DD} = 10 Vdc, I_D = 0.6 Adc, V_{GS} = 2.7 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	—	20	—	
Rise Time		t_r	—	94	—	
Turn–Off Delay Time		$t_{d(off)}$	—	49	—	
Fall Time		t_f	—	76	—	
Gate Charge	(V_{DS} = 16 Vdc, I_D = 1.2 Adc, V_{GS} = 4.5 Vdc)	Q_T	—	5.3	7.5	nC
		Q_1	—	0.7	—	
		Q_2	—	2.6	—	
		Q_3	—	1.9	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 1.2 Adc, V_{GS} = 0 Vdc)	V_{SD}	— —	0.89 0.72	1.1 —	Vdc
Reverse Recovery Time	(I_S = 1.2 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	86	—	nsec
		t_a	—	27	—	
		t_b	—	59	—	
		Q_{RR}	—	0.115	—	μC

NOTE: Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

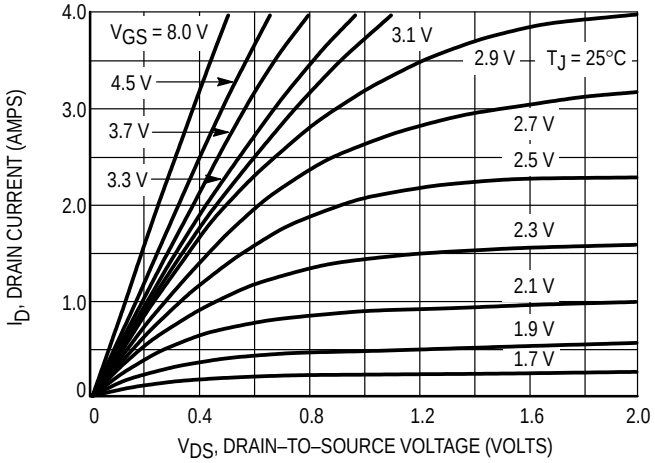


Figure 1. On–Region Characteristics

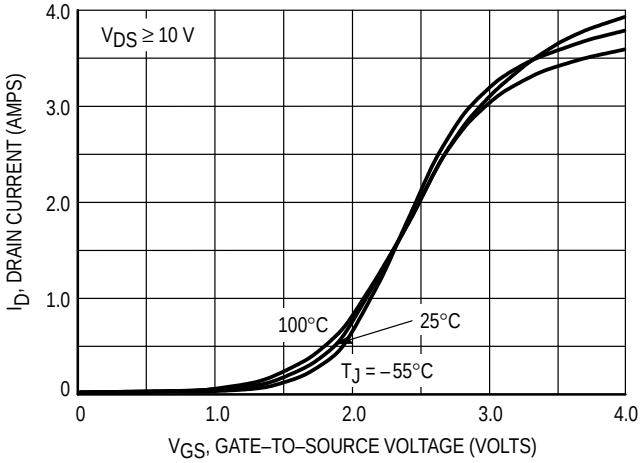


Figure 2. Transfer Characteristics

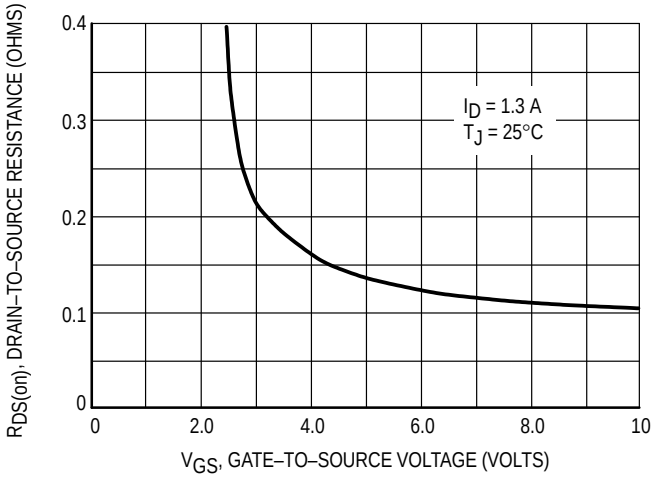


Figure 3. On–Resistance versus Drain Current

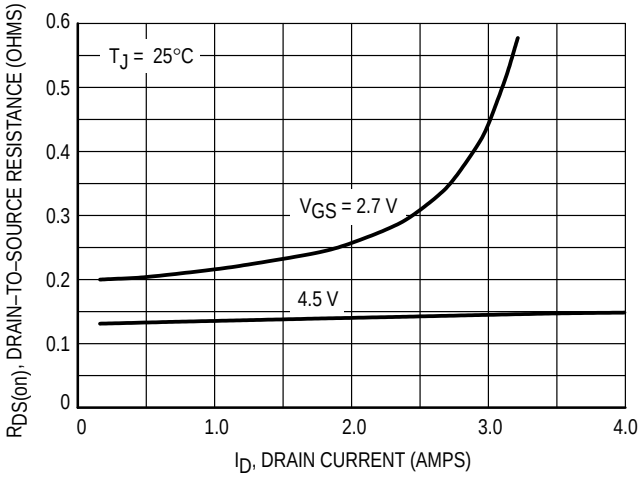


Figure 4. On–Resistance versus Drain Current and Gate Voltage

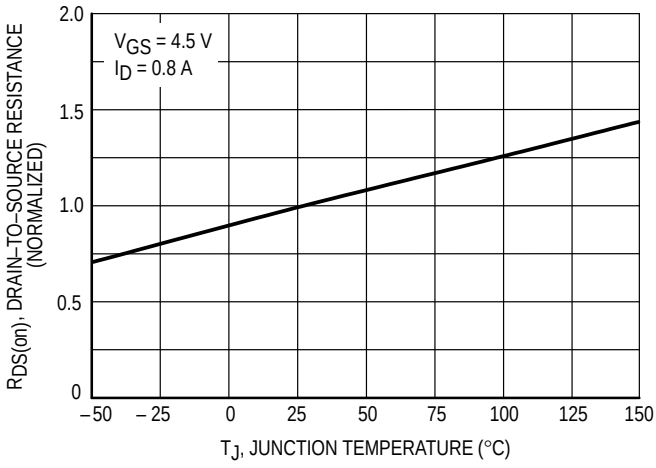


Figure 5. On–Resistance versus Temperature

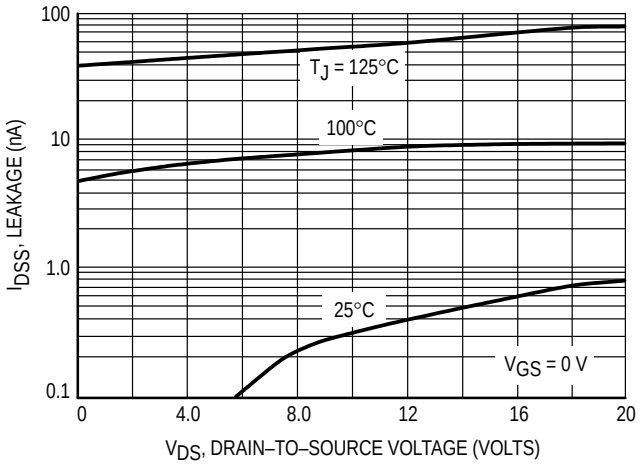


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

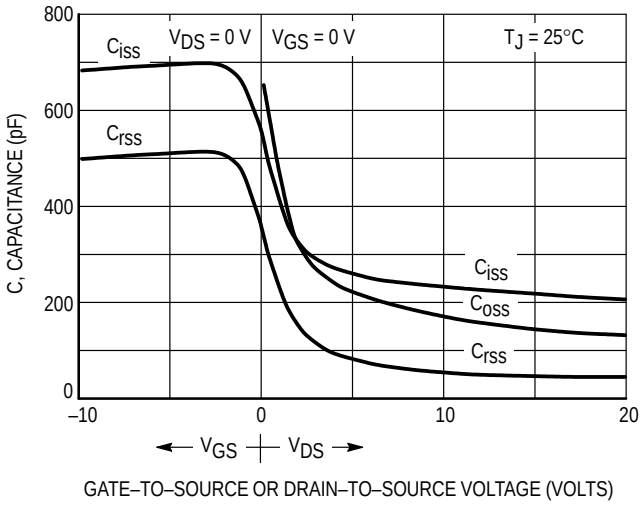


Figure 7. Capacitance Variation

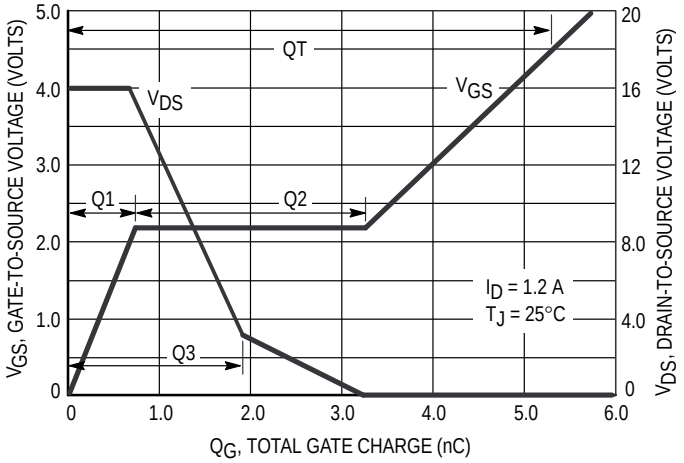


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

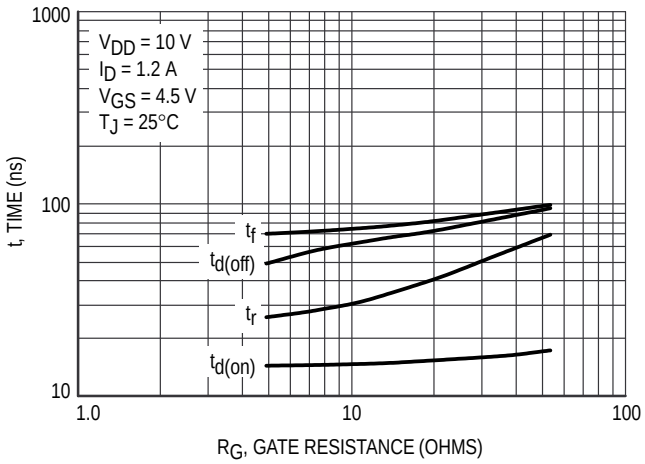


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 11. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

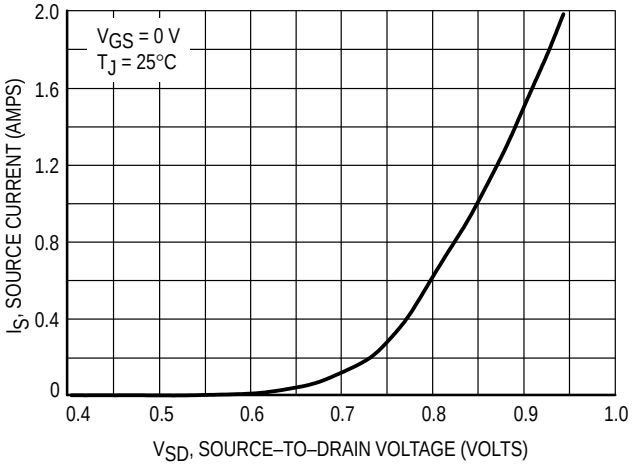


Figure 10. Diode Forward Voltage versus Current

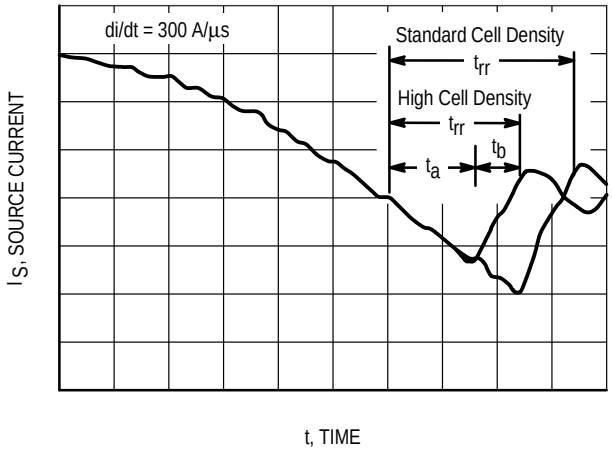


Figure 11. Reverse Recovery Time (t_{rr})

TYPICAL ELECTRICAL CHARACTERISTICS

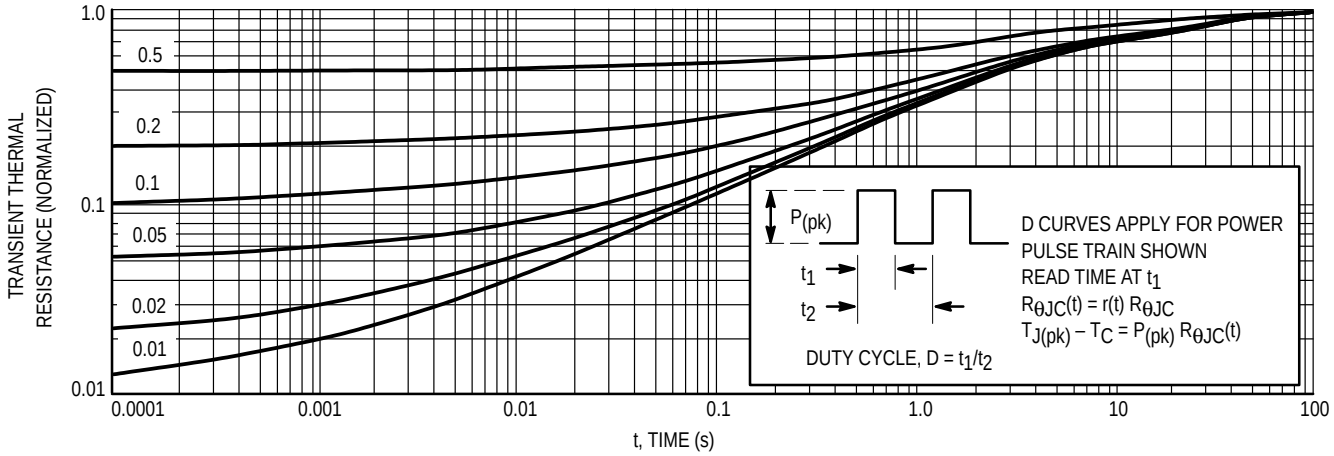


Figure 12. Thermal Response

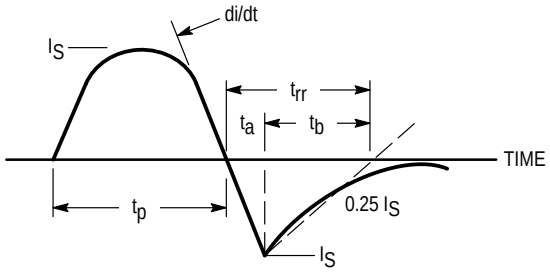
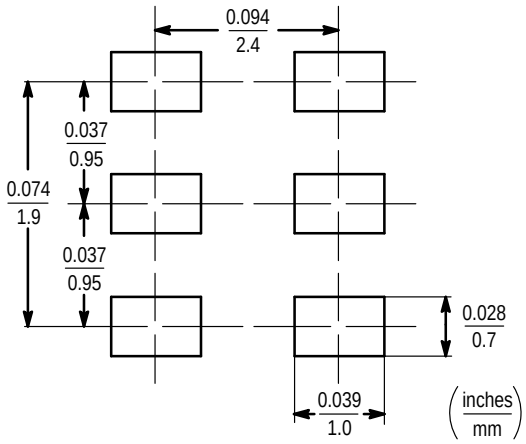


Figure 13. Diode Reverse Recovery Waveform

INFORMATION FOR USING THE TSOP–6 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



TSOP–6

TSOP–6 POWER DISSIPATION

The power dissipation of the TSOP–6 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the TSOP–6 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 400 milliwatts.

$$P_D = \frac{150°C - 25°C}{312°C/W} = 400 \text{ milliwatts}$$

The 312°C/W for the TSOP–6 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 400 milliwatts. There are other alternatives to achieving higher power dissipation from the TSOP–6 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

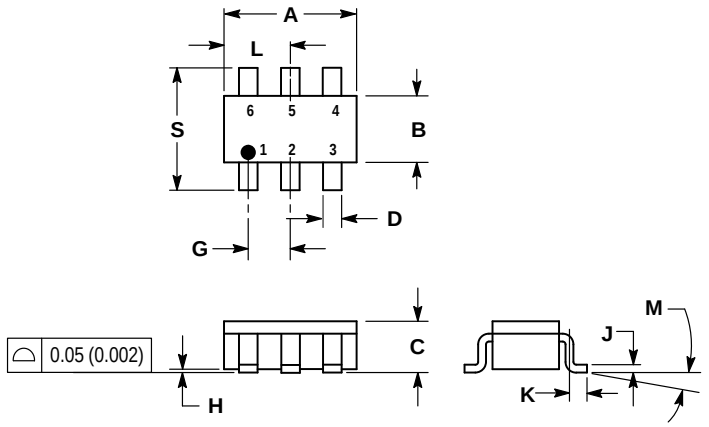
SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0 °	10 °	0 °	10 °
S	2.50	3.00	0.0985	0.1181

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

CASE 318G–02
ISSUE B

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