MC10EP56

Dual Differential 2:1 Multiplexer

The MC10EP56 is a dual, fully differential 2:1 multiplexer. The differential data path makes the device ideal for multiplexing low skew clock or other skew sensitive signals. Multiple V_{BB} pins are provided to ease AC coupling of input signals. If used, the V_{BB} output should be bypassed to ground with a 0.01μF capacitor.

The device features both individual and common select inputs to address both data path and random logic applications.

- 350ps Typical Propagation Delays
- Typical Frequency 3.0GHz
- 20–Lead TSSOP Package
- PECL mode: 3.0V to 5.5V V_{CC} with V_{EE} = 0V
- ECL mode: 0V V_{CC} with V_{EE} = –3.0V to –5.5V
- Separate and Common Select
- Internal Input Resistors: Pulldown on D, $\overline{D}$
- Q Output will default LOW with inputs open or at V_{EE}
- ESD Protection: >4KV HBM, >200V MM
- V_{BB} Outputs
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack. For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 140 devices

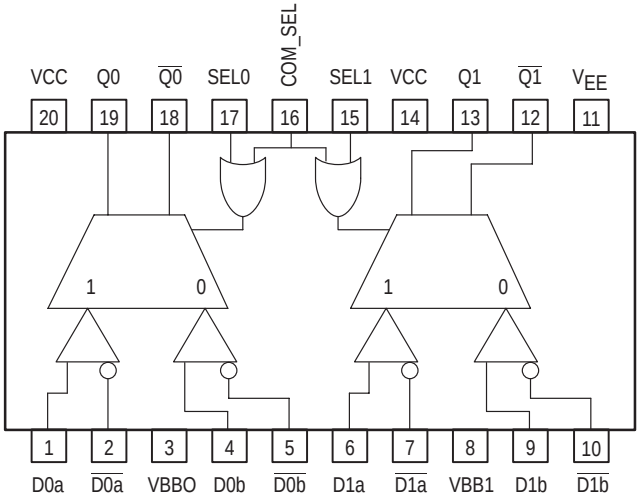

Figure 1. 20–Lead TSSOP (Top View) **and Logic Diagram**

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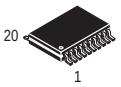
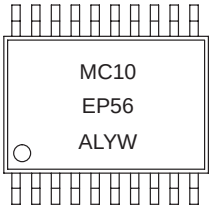


TSSOP–20
DT SUFFIX
CASE 948E

MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	**FUNCTION**
D0a–D1a	ECL Input Data a
$\overline{D0a}$–$\overline{D1a}$	ECL Input Data a Invert
D0b–D1b	ECL Input Data b
$\overline{D0b}$–$\overline{D1b}$	ECL Input Data b Invert
SEL0–SEL1	ECL Indiv. Select Input
COM_SEL	ECL Common Select Input
V_{BB0}, V_{BB1}	Output Reference Voltage
Q0–Q1	ECL True Outputs
$\overline{Q0}$–$\overline{Q1}$	ECL Inverted Outputs
V_{CC}	Positive Supply
V_{EE}	Negative, 0 Supply

TRUTH TABLE

SEL0	SEL1	COM_SEL	Q0, $\overline{Q0}$	Q1, $\overline{Q1}$
X	X	H	a	a
L	L	L	b	b
L	H	L	b	a
H	H	L	a	a
H	L	L	a	b

ORDERING INFORMATION

Device	Package	Shipping
MC10EP56DT	TSSOP	75 Units/Rail
MC10EP56DTR2	TSSOP	2500 Tape & Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current Continuous Surge	50 100	mA
I_{BB}	V_{BB} Sink/Source Current†	± 0.5	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) Still Air 500lfpm	140 100	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	23 to 41 ± 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V; V_{EE} = –5.5V to –3.0V) (Note 4.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
IEE	Power Supply Current (Note 1.)	50	65	88	50	65	88	50	65	88	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1135	–1060	–885	–1070	–1015	–820	–1010	–975	–760	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1995	–1810	–1685	–1995	–1745	–1620	–1995	–1685	–1560	mV
V_{IH}	Input HIGH Voltage Single Ended	–1210		–885	–1145		–820	–1085		–760	mV
V_{IL}	Input LOW Voltage Single Ended	–1935		–1610	–1870		–1545	–1810		–1485	mV
V_{BB}	Output Voltage Reference	–1550	–1450	–1350	–1500	–1400	–1300	–1450	–1350	–1250	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current SEL, COM_SEL, D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			µA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC}–2.0 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
4. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V) (Note 8.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 5.)	50	65	88	50	65	88	50	65	88	mA
V_{OH}	Output HIGH Voltage (Note 6.)	2165	2240	2415	2230	2285	2480	2290	2325	2540	mV
V_{OL}	Output LOW Voltage (Note 6.)	1305	1490	1615	1305	1555	1680	1305	1615	1740	mV
V_{IH}	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
V_{BB}	Output Voltage Reference	1750	1850	1950	1800	1900	2000	1850	1950	2050	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 7.)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current SEL, COM_SEL, D $\overline{D}$	 0.5 –150			 0.5 –150			 0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

5. V_{CC} = 3.3V, V_{EE} = 0V, all other pins floating.
6. All loading with 50 ohms to V_{CC}–2.0 volts.
7. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
8. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, PECL (V_{CC} = 5.0V ± 0.5V, V_{EE} = 0V) (Note 12.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 9.)	50	65	88	50	65	88	50	65	88	mA
V_{OH}	Output HIGH Voltage (Note 10.)	3865	3940	4115	3930	3985	4180	3990	4025	4240	mV
V_{OL}	Output LOW Voltage (Note 10.)	3005	3190	3315	3005	3255	3380	3005	3315	3440	mV
V_{IH}	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
V_{BB}	Output Voltage Reference	3450	3550	3650	3500	3600	3700	3550	3650	3750	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 11.)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current SEL, COM_SEL, D $\overline{D}$	 0.5 –150			 0.5 –150			 0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

9. V_{CC} = 5.0V, V_{EE} = 0V, all other pins floating.
10. All loading with 50 ohms to V_{CC}–2.0 volts.
11. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
12. Input and output parameters vary 1:1 with V_{CC}.

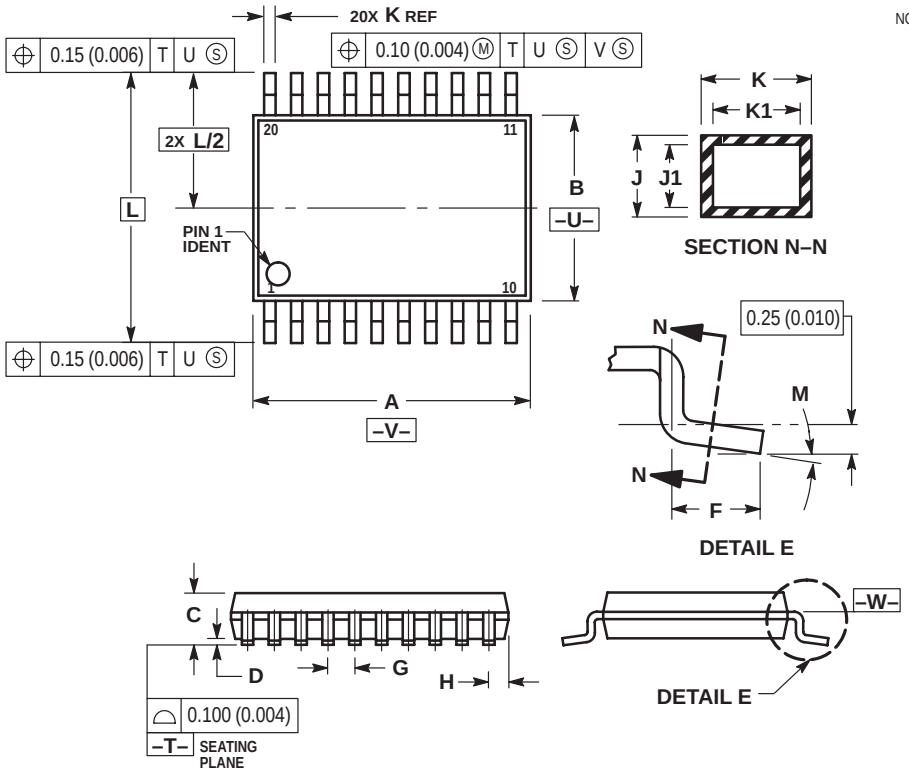
AC CHARACTERISTICS (V_{CC} = 0V; V_{EE} = –3.0V to –5.5V) or (V_{CC} = 3.0V to 5.5V; V_{EE} = 0V)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle Frequency (Note 13.)					3.0					GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential										ps
	D–>Q, $\overline{Q}$ (Diff)	250	340	480	250	360	480	300	400	520	
	D–>Q, $\overline{Q}$ (SE)	250	340	480	250	360	480	300	400	520	
	SEL–>Q, $\overline{Q}$	200	340	550	200	340	550	200	390	650	
	COM_SEL–>Q, $\overline{Q}$	200	350	580	200	360	580	200	400	675	
t_{SKEW}	Within–Device Skew (Note 14.)		TBD			TBD			TBD		ps
	Duty Cycle Skew (Note 15.)		TBD			TBD			TBD		
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times Q, $\overline{Q}$ (20% – 80%)	100	150	200	100	150	200	100	160	220	ps

13. F_{max} guaranteed for functionality only.
14. Within–Device Skew is defined as identical transitions on similar paths through a device.
15. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

PACKAGE DIMENSIONS

TSSOP–20
DT SUFFIX
20 PIN PLASTIC TSSOP PACKAGE
CASE 948E–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

Notes

Notes

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