National Semiconductor

MICROCIRCUIT DATA SHEET

MNLM149-X REV 0B1

Original Creation Date: 08/08/95
Last Update Date: 10/23/98
Last Major Revision Date: 08/08/95

QUAD OP AMP

General Description

The LM149 is a quad op amp. It consists of four independent, high gain, internally compensated, low power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar LM741 operational amplifier. In addition the total supply current for all four amplifiers is comparable to the supply current of a single LM741 type op amp. Other features include input offset currents and input bias current which are much less than those of standard LM741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling. The LM149 has the same features as the LM148 plus a gain bandwidth product of a 4 MHz at a gain of 5 or greater.

The LM149 can be used anywhere multiple LM741 or LM1558 type amplifiers are being used and in applications where amplifier matching, high packing density, or high speed is required.

Industry Part Number

LM149

NS Part Numbers

LM149J/883

Prime Die

LM149

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 741 op amp operating characteristics
- Low supply current drain 0.6mA/Amplifier
- Class AB output stage-no crossover distortion
- Pin compatible with the LM124
- Low input offset voltage 1mV
- Low input offset current 4nA
- Low input bias current 30nA
- Gain bandwidth product (Av $\geq$ 5) 4Mhz
- High degree of isolation between amplifiers 120dB
- Overload protection for inputs and outputs

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage	± 22V
Differential Input Voltage	± 44V
Output Short Circuit Duration (Note 2)	Continuous
Power Dissipation (Note 3)	
(Pd at 25 C)	1100mW
Maximum Junction Temperature (TjMAX)	150 C
Operating Temperature Range	-55 C ≤ TA ≤ +125 C
Storage Temperature Range	-65 C to +150 C
Lead Temperature (Soldering, 10 seconds)	300 C
Thermal Resistance	
ThetaJA	
(Still Air)	103 C/W
(500LF/Min Air flow)	52 C/W
ThetaJC	19 C/W
ESD Tolerance (Note 4)	500V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: Any of the amplifier outputs can be shorted to ground indefinitely however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is less.

Note 4: Human body model, 1.5K Ohms in series with 100pF.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vs = ±15V, Rs = 0.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage	Rs = 10K Oohms			-5	5	mV	1
					-6	6	mV	2, 3
Iio	Input Offset Current	Rs = 10K Ohms			-25	25	nA	1
					-75	75	nA	2, 3
+Iib	Input Bias Current	Rs = 10K Ohms			-100		nA	1
					-325		nA	2, 3
-Iib	Input Bias Current	Rs = 10K Ohms				+100	nA	1
						+325	nA	2, 3
Avs+	Open Loop Voltage Gain	Rl = 2K Ohms, Vout = 0V to +10V, Rs = 10K Ohms	2		50		K	1
			2		25		K	2, 3
Avs-	Open Loop Voltage Gain	Rl = 2K Ohms, Vout = 0V to -10V, Rs = 10K Ohms	2		50		K	1
			2		25		K	2, 3
Icc	Power Supply Current	Vs = ± 15V				3.6	mA	1
CMRR	Common Mode Rejection Ratio	Vcm = ±12V			70		dB	1, 2, 3
SVRR	Supply Voltage Rejection Ratio	Rs = 10K Ohms, Vs = ±15 to ±5V			77		dB	1, 2, 3
+Swing	Output Voltage Swing	Rl = 10K Ohms			+12		V	1, 2, 3
		Rl = 2K Ohms			+10		V	1, 2, 3
-Swing	Output Voltage Swing	Rl = 10K Ohms				-12	V	1, 2, 3
		Rl = 2K Ohms				-10	V	1, 2, 3
Ios+	Short Circuit Current				-45	-14	mA	1
Ios-	Short Circuit Current				+14	+45	mA	1
IBVcc	Breakdown Supply Current	Vs = ±22V, Vin = ±19V				9	mA	1, 2, 3
+Il	Input Leakage Current	Vs = ±22V, Vin = ±19V				+10	uA	1, 2, 3
-Il	Input Leakage Current	Vs = ±22V, Vin = ±19V			-10		uA	1, 2, 3

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vs = ±15V, Rs = 0.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Rin	Input Resistance		1		0.8		MOhms	1
Vin	Input Voltage Range	Vs = ±22V	1		±19		V	1
		Vs = ±15V	1		±12		V	1, 2, 3
Vdiff	Differential Input Voltage	Vcc = ±22V	1		±38		V	1

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vs = ±15V, Rs = 0.

Gbw	Gain Bandwidth Product		1		2		MHz	7

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vs = ±15V, Rs = 0. "Deltas not required on B-Level product. Deltas required for S-Level product ONLY as specified on Internal Processing Instructions (IPI)."

Vio	Input Offset Voltage	Rs = 10K Ohms			-1	1	mV	1
Iio	Input Offset Current	Rs = 10K Ohms			-5	5	nA	1

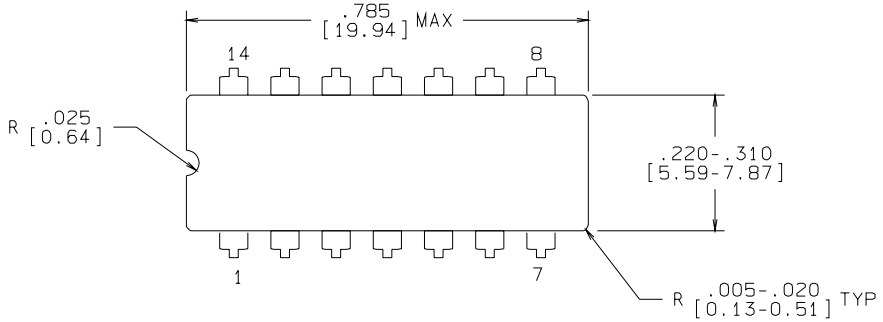
Note 1: Parameter tested go-no-go.
Note 2: K = V/mV.

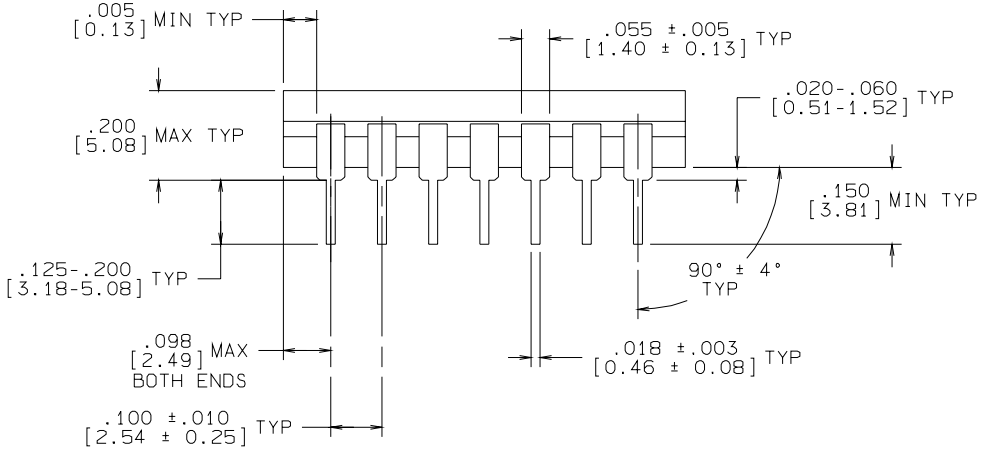
Graphics and Diagrams

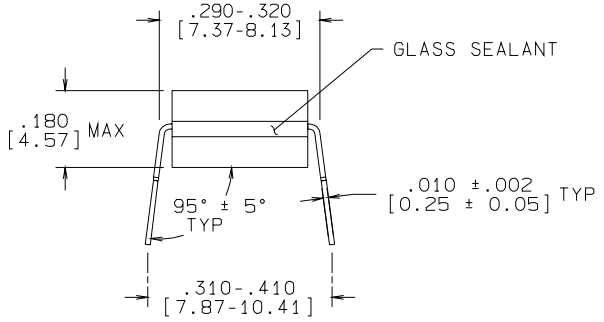
GRAPHICS#	DESCRIPTION
09173HRA2	CERDIP (J), 14 LEAD (B/I CKT)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
P000230A	CERDIP (J), 14 LEAD (PINOUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
H	REVISE PER CURRENT STD; REDRAW	10001	09/15/93	TL/







CONTROLLING DIMENSION: INCH

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

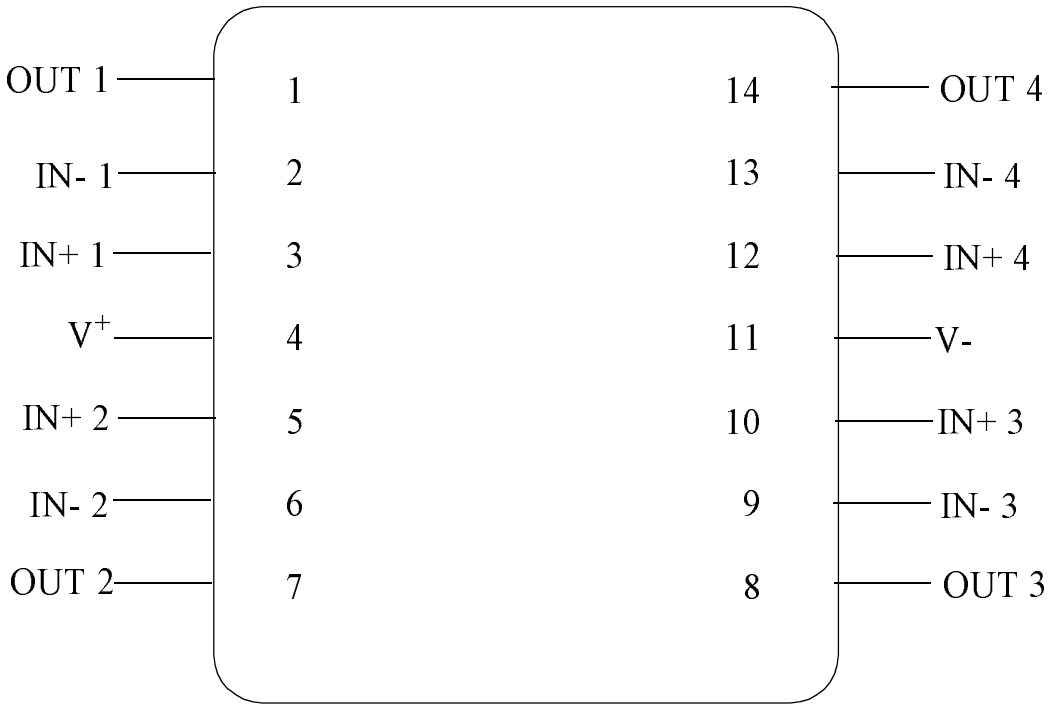
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 14 LEAD,

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J14A	H

DO NOT SCALE DRAWING | SHEET 1 OF 1



LM149J
14 - LEAD DIP
CONNECTION DIAGRAM
TOP VIEW
P000230A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0B1	M0002829	10/23/98	Barbara Lopez	Update MDS: MNLM149-X Rev. 0B0 to MNLM149-X Rev. 0B1. Updated Burn-in graphic and added pinout.