National Semiconductor

MICROCIRCUIT DATA SHEET

MNLM148-X REV 1B1

Original Creation Date: 08/08/95
Last Update Date: 04/14/98
Last Major Revision Date: 12/01/95

QUAD LM741 OP AMP

General Description

The LM148 is a true quad LM741. It consists of four independent, high gain, internally compensated, low power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar LM741 operational amplifier. In addition the total supply current for all four amplifiers is comparable to the supply current of a single LM741 type op amp. Other features include input offset currents and input bias current which are much less than those of a standard LM741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling.

The LM148 can be used anywhere multiple LM741 or LM1558 type amplifiers are being used and in applications where amplifier matching or high packing density is required.

Industry Part Number

LM148

NS Part Numbers

LM148E/883
LM148J/883

Prime Die

LM148

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{o}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 741 op amp operating characteristics
- Low supply current drain 0.6mA/Amplifier
- Class AB output stage-no crossover distortion
- Pin compatible with the LM124
- Low input offset voltage 1mV
- Low input offset current 4nA
- Low input bias current 30nA
- Gain bandwidth product (Unity Gain) 1.0Mhz
- High degree of isolation between amplifiers 120dB
- Overload protection for inputs and outputs

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage	± 22V
Differential Input Voltage	± 44V
Output Short Circuit Duration (Note 2)	Continuous
Power Dissipation (Note 3)	
(Pd at 25 C)	1100 mW
Maximum Junction Temperature (TjMAX)	150 C
Operating Temperature Range	-55 C ≤ TA ≤ +125 C
Storage Temperature Range	-65 C to +150 C
Lead Temperature (Soldering, 10 seconds)	300 C
Thermal Resistance	
ThetaJA	
CERDIP (Still Air)	103 C/W
CERDIP (500LF/Min Air flow)	52 C/W
LCC (Still Air)	90 C/W
LCC (500LF/Min Air flow)	66 C/W
ThetaJC	
CERDIP	19 C/W
LCC	21 C/W
ESD Tolerance (Note 4)	500V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: Any amplifier outputs can be shorted to ground indefinitely however, more that one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum available power dissipation at any temperature is Pdmax = (TjMAX - TA) ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 4: Human body model, 1.5K Ohms in series with 100pF.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = ±15V, Rs = 0 Ohms.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage	Vcm = 0V, Rs = 50 Ohms			-5	+5	mV	1
					-6	+6	mV	2, 3
Iio	Input Offset Current	Vcm = 0V			-25	+25	nA	1
					-75	+75	nA	2, 3
+Iib	Input Bias Current	Vcm = 0V			1	100	nA	1
					1	325	nA	2, 3
-Iib	Input Bias Current	Vcc = 0V			1	100	nA	1
					1	325	nA	2, 3
PSRR+	Power Supply Rejection Ratio	+Vcc = +15V and +5V, -Vcc = -15V, Rs = 50 Ohms			77		dB	1, 2, 3
PSRR-	Power Supply Rejection Ratio	+Vcc = +15V, -Vcc = -15V and -5V, Rs = 50 Ohms			77		dB	1, 2, 3
CMRR	Common Mode Rejection Ratio	Vcm = ± 12V, Rs = 50 Ohms			70		dB	1, 2, 3
Ios+	Short Circuit Current				-45	-14	mA	1
Ios-	Short Circuit Current				14	45	mA	1
Icc	Power Supply Current				.4	3.6	mA	1
					.4	4.5	mA	2, 3
Rin	Input Resistance		1		.8		MOhms	1
Avs+	Large Signal Voltage	Rl = 2K Ohms, Vo = 0 to +10V			50		V/mV	4
					25		V/mV	5, 6
Avs-	Large Signal Voltage	Rl = 2K Ohms, Vo = 0 to -10V			50		V/mV	4
					25		V/mV	5, 6
Vout+	Output Voltage Swing	Rl = 10K Ohms			+12		V	4, 5, 6
		Rl = 2K Ohms			+10		V	4, 5, 6
Vout-	Output Voltage Swing	Rl = 10K Ohms				-12	V	4, 5, 6
		Rl = 2K Ohms				-10	V	4, 5, 6

Electrical Characteristics

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = ±15V, Av = 1, Rs = 0.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Sr+	Slew Rate				0.2		V/uS	7, 8A, 8B
Sr-	Slew Rate				0.2		MHz	7, 8A, 8B
Gbw	Gain Bandwidth Product				.4	1.4	MHz	7, 8A, 8B

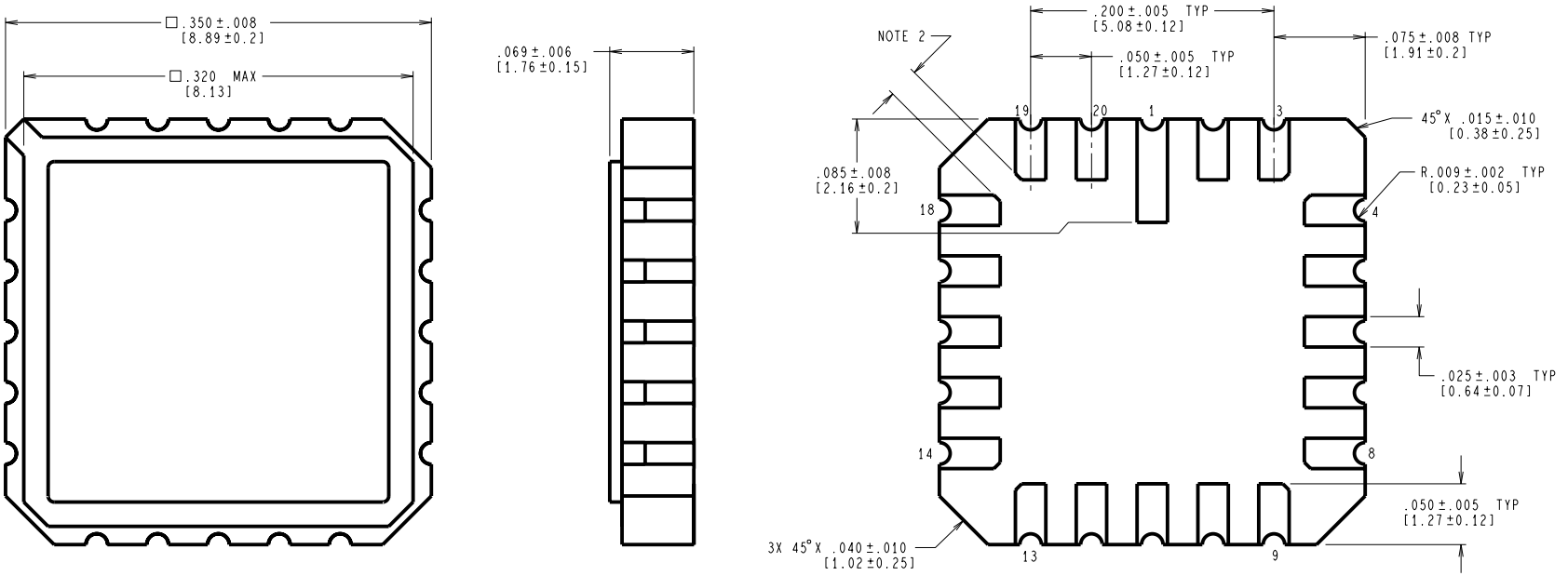
Note 1: Parameter tested go-no-go.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
05819HRA2	LDLESS CHIP CARRIER,TYPE C,20 TERMINAL(B/I CKT)
09173HRA2	CERDIP (J), 14 LEAD (B/I CKT)
E20ARE	LCC (E), TYPE C, 20 TERMINAL(P/P DWG)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
P000229A	CERDIP (J), 14 LEAD (PINOUT)
P000394A	LCC (E), TYPE C, 20 TERMINAL (PINOUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
E	REVISE AND REDRAW.	10005	02/10/94	DEG/



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

   a. 50 MICROINCHES/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICROINCHES/1.27-8.89 MICROMETERS NICKEL.

   b. SOLDER DIP.
   SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.

2. CORNER PADS MAY HAVE A 45°X.020IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE .015IN/0.38mm DIMENSION.

4. REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

MIL/AERO
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: Dwayne Grady	02/10/94
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION INCH [MM]

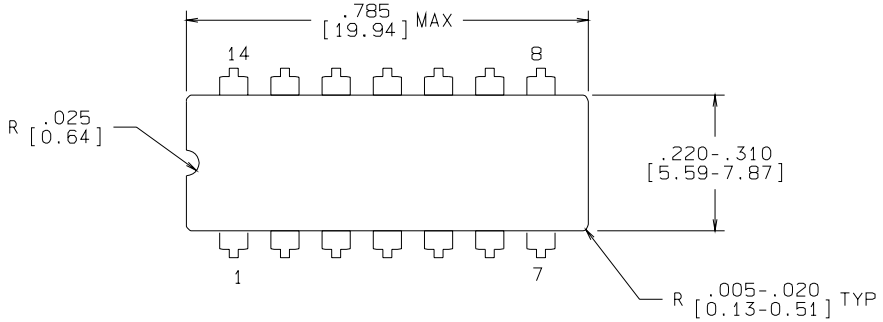
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

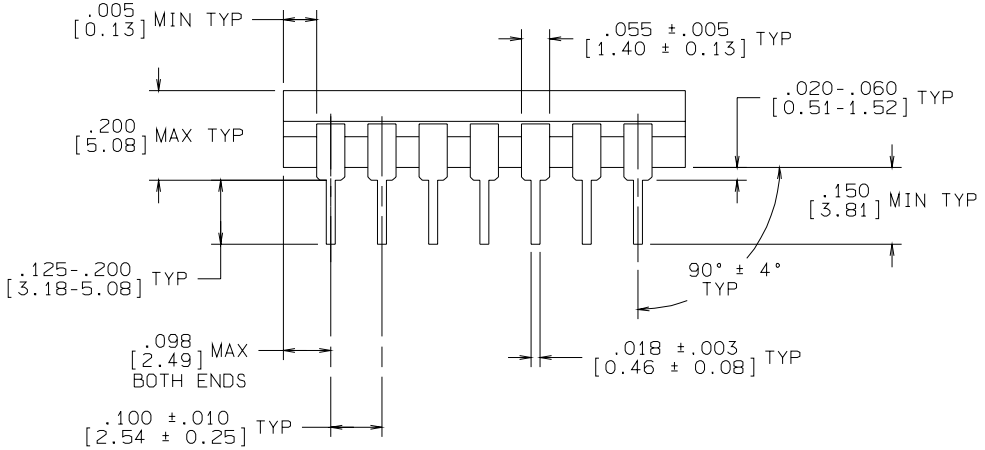
LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL

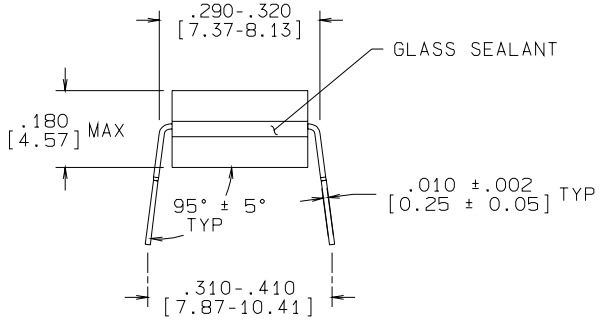
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-E20A	E

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
H	REVISE PER CURRENT STD; REDRAW	10001	09/15/93	TL/







CONTROLLING DIMENSION: INCH

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

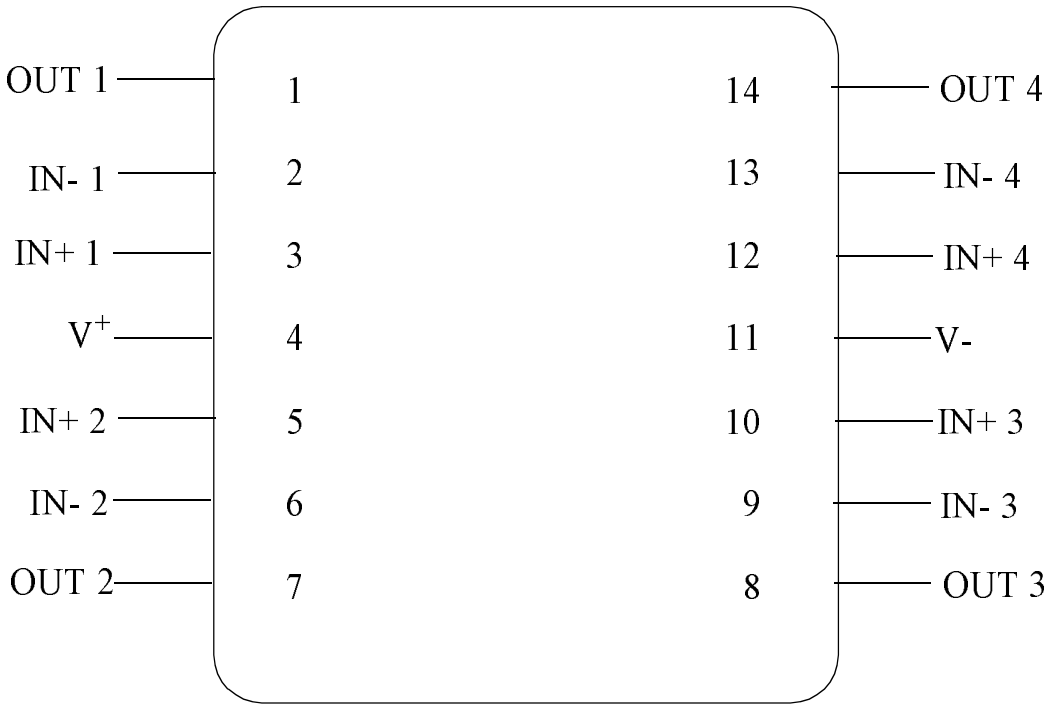
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 14 LEAD,

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J14A	H

DO NOT SCALE DRAWING | SHEET 1 OF 1



LM148J
14 - LEAD DIP
CONNECTION DIAGRAM
TOP VIEW
P000229A

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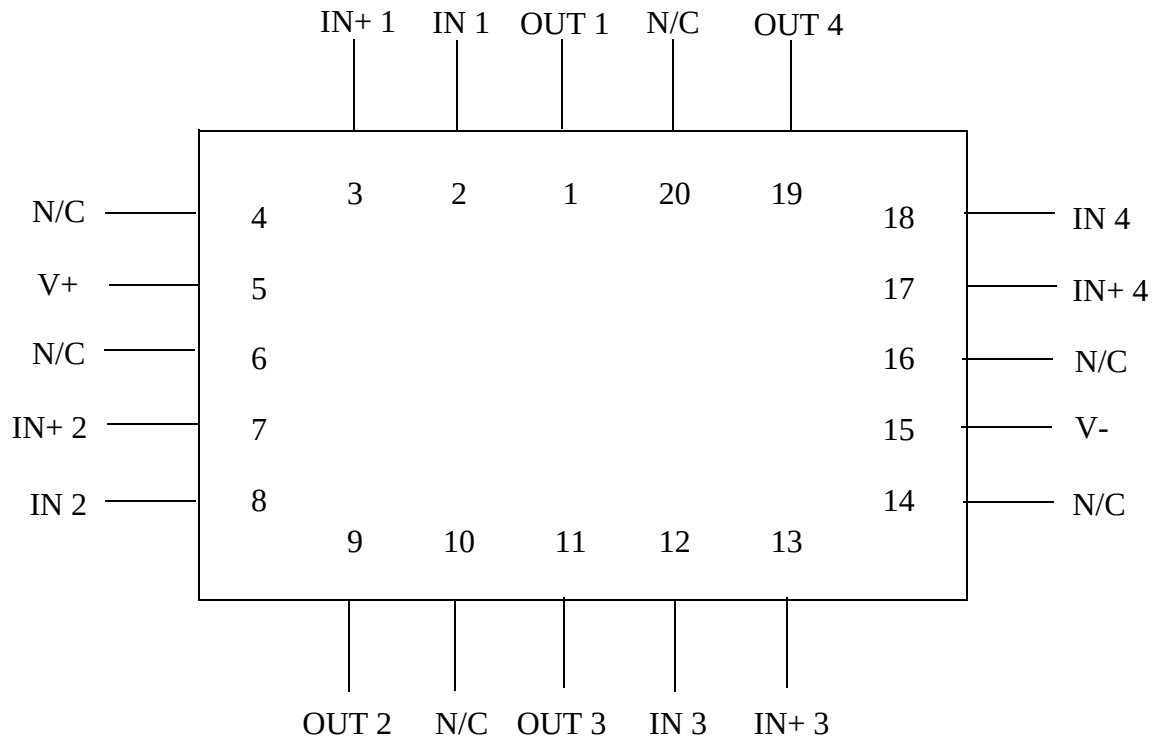
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM148E
20 - LEAD LCC
CONNECTION DIAGRAM
TOP VIEW
P000394A

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Revision History

Rev	ECN #	Rel Date	Originator	Changes
1B1	M0002837	04/14/98	Barbara Lopez	Update MDS: MNLM148-X Rev. 1A0 to MNLM148-X Rev. 1B1. Updated graphics. Deleted NSID LM148J-MLS Obsolete product per Spec Control.