National Semiconductor

MILITARY DATA SHEET

MNDS96F175M-X REV 0A0

Original Creation Date: 01/25/96
Last Update Date: 01/30/96
Last Major Revision Date: 01/25/96

RS-485 DIFFERENTIAL LINE RECEIVER

General Description

The DS96F175 is a high speed quad differential line receiver designed to meet EIA Standard RS-485. The DS96F175 offers improved performance due to the use of state-of-the-art L-Fast bipolar technology. The L-Fast technology allows for higher speeds and lower currents by utilizing extremely short gate delay times. Thus, the DS96F175 features lower power and an extended temperature range.

The DS96F175 has TRI-STATE outputs and is optimized for balanced multipoint data bus transmission at rates up to 15 Mbps. The receivers feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of 200mV over a common mode input voltage range of -7V to +12V. The receivers are therefore suitable for multipoint applications in noisy environments. The DS96F175 features separate active high Enables for each receiver pair.

Compatible RS-485 drivers, transceivers, and repeaters are also offered to provide optimum bus performance. The respective device types are DS96F172, DS96F174 and DS16F95.

Industry Part Number

DS96F175

NS Part Numbers

DS96F175ME/883 *
DS96F175MJ/883 **
DS96F175MW/883 ***

Prime Die

M175

Controlling Document

9076601M2A*,MEA**,MFA***

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Meets EIA Standard RS-485, RS-422A, RS-423A
- Designed for multipoint bus applications
- TRI-STATE outputs
- Common mode input voltage range: -7V to +12V
- Operates from single +5.0V supply
- Lower power version
- Input sensitivity of ±200mV over common mode range
- Input hysteresis of 50mV typical
- High input impedance
- DS96F173 and DS96F175 are lead and function compatible with SN75173/175 or the AM26LS32/MC3486

(Absolute Maximum Ratings)

(Note 1)

Storage Temperature Range	
Ceramic DIP	-65 C to +175 C
Lead Temperature	
(Soldering, 60 sec.)	300 C
Maximum Power Dissipation at 25 C (Note 2)	
Ceramic J Package	1500mW
Ceramic W Package	1034mW
Ceramic E Package	1500mW
Supply Voltage	7.0V
Input Voltage, A or B Inputs	±25V
Differential Input Voltage	±25V
Enable Input Voltage	7.0V
Low Level Output Current	50mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: *Derate J Package 10mW/ C above 25C; Derate W package 6.9mW/ C above 25 C; Derate E package 11.11mW/ C above 25 C.

Recommended Operating Conditions

Supply Voltage (Vcc)

Min.	Typ.	Max.	Units
4.50	5.0	5.50	V

Common Mode Input Voltage Vcm

Min.	Typ.	Max.	Units
-7		+12	V

Differential Input Voltage(Vid)

Min.	Typ.	Max.	Units
-7		+12	V

Output Current HIGH(Ioh)

Min.	Typ.	Max.	Units
		-400	uA

Output Current LOW(Iol)

Mix.	Typ.	Max.	Units
		16	mA

Operating Temperature (TA)

Min.	Typ.	Max.	Units
-55	25	125	C

Electrical Characteristics

DC PARAMETERS:

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Icc	Supply Current	Vcc = 5.5V, Venable = 0V, Vid = 2V	1			50	mA	1, 2, 3
Voh	Logical "1" Output Voltage	Vcc = 4.5V, Ioh = -400uA, Vid = .2V	2		2.5		V	1, 2, 3
Vol	Logical "0" Output Voltage	Vcc = 4.5V, Iol = 8mA, Vid = -.2V	2			.45	V	1, 2, 3
Vth Diff	Input Threshold Voltage	Vcc = 4.5V & 5.5V, Vcm = 0V, Vo = 2.5V, Io = -400uA	2			.20	V	1, 2, 3
		Vcc = 4.5V & 5.5V, Vcm = -12V, Vo = 2.5V, Io = -400uA	2			.20	V	1, 2, 3
		Vcc = 4.5V & 5.5V, Vcm = 12V, Vo = 2.5V, Io = -400uA	2			.20	V	1, 2, 3
Vtl Diff	Input Threshold Voltage	Vcc = 4.5V & 5.5V, Vcm = 0V, Vo = .5V, Io = 16mA	2		-.20		V	1, 2, 3
		Vcc = 4.5V & 5.5V, Vcm = -12V, Vo = .5V, Io = 16mA	2		-.20		V	1, 2, 3
		Vcc = 4.5V & 5.5V, Vcm = 12V, Vo = .5V, Io = 16mA	2		-.20		V	1, 2, 3
Ii	Input Line Current	Vcc = 4.5V, Vin = 12V Untested Inputs are 0V				1	mA	1, 2, 3
		Vcc = 5.5V, Vin = -7V Untested Inputs are 0V			-.8		mA	1, 2, 3
Iih	Logical "1" Enable Input Current	Vcc = 5.5V, Vih = 2.7V				10	uA	1, 2, 3
Iil	Logical "0" Enable Input Current	Vcc = 5.5V, Vil = .4V			-100		uA	1, 2, 3
Ios	Output Short Circuit Current	Vcc = 4.5V, Vo = 0V	2		-85	-15	mA	1, 2, 3
		Vcc = 5.5V, Vo = 0V	2		-85	-15	mA	1, 2, 3
Vik	Enable Input Clamp Voltage	Vcc = 4.5V, Ii = -18mA			-1.5		V	1, 2, 3
Ioz	High Impedance Output Current	Vcc = 5.5V, Venable = .8V, Vout = .4V, outputs disabled			-20	20	uA	1, 2, 3
		Vcc = 5.5V, Venable = .8V, Vout = 2.4V, outputs disabled			-20	20	uA	1, 2, 3
Vih	Logical "1" Enable Input Voltage		3		2		V	1, 2, 3

Electrical Characteristics

DC PARAMETERS:(Continued)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vil	Logical "0" Enable Input Voltage		4			.8	V	1, 2, 3
Rin	Input Resistance				10		K Ohms	1, 2, 3

AC PARAMETERS:

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = 5V

tPHL	Propagation Delay	Cl = 15pF				22	nS	1
						30	nS	2, 3
tPLH	Propagation Delay	Cl = 15pF				22	nS	1
						30	nS	2, 3
tPZH	Propagation Delay	Cl = 15pF				16	nS	1
						27	nS	2, 3
tPZL	Propagation Delay	Cl = 15pF				18	nS	1
						27	nS	2, 3
tPHZ	Propagation Delay	Cl = 5pF				20	nS	1
						27	nS	2, 3
		Cl = 20pF	5			30	nS	1
			5			37	nS	2, 3
tPLZ	Propagation Delay	Cl = 5pF				18	nS	1
						30	nS	2, 3
tPW	Propagation Delay					3	nS	1
						8	nS	2
						5	nS	3

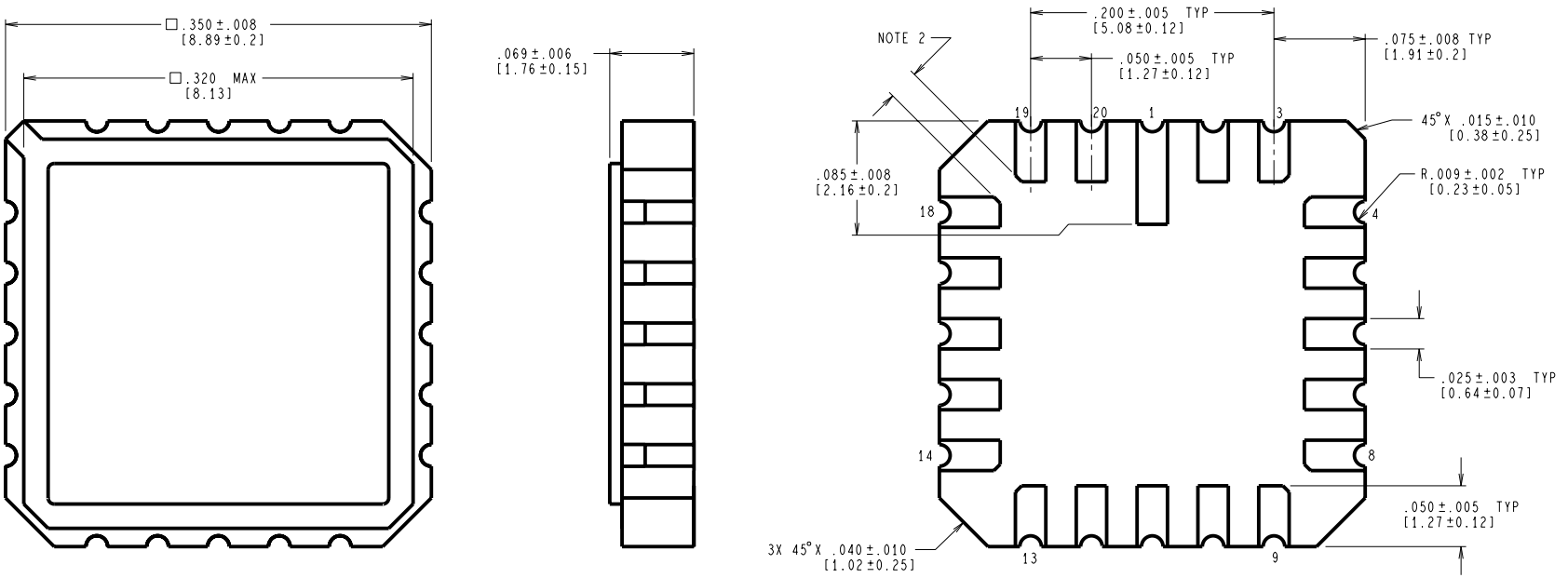
Note 1: Icc is tested with outputs disabled (worst case), Icc enabled is guaranteed by this test.
Note 2: Venable =2V. Voh & Vol are tested over common mode voltage range of +/-12V via the Vth/Vtl tests.
Note 3: Guaranteed by Vol & Voh tests.
Note 4: Guaranteed by Ioz test.
Note 5: Testing at 20pF assures conformance to spec at 5pF.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
E20ARE	LDLESS CHIP CARRIER, TYPE C 20 TERMINAL(P/P DWG)
J16ARL	CERDIP (J), 16 LEAD (P/P DWG)
W16ARL	CERPAC (W), 16 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
E	REVISE AND REDRAW.	10005	02/10/94	DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

   a. 50 MICROINCHES/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICROINCHES/1.27-8.89 MICROMETERS NICKEL.

   b. SOLDER DIP.
   SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.

2. CORNER PADS MAY HAVE A 45°X.020IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE .015IN/0.38mm DIMENSION.

4. REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL/AERO
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: Dwayne Grady	02/10/94
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION
INCH [MM]

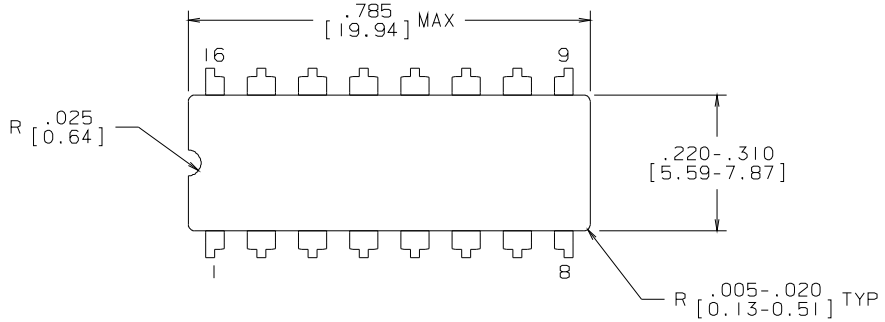
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

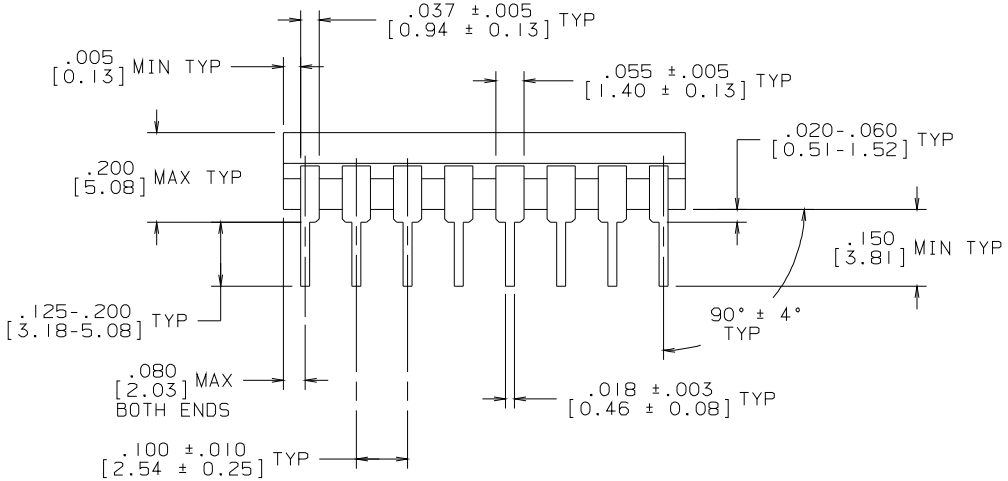
LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL

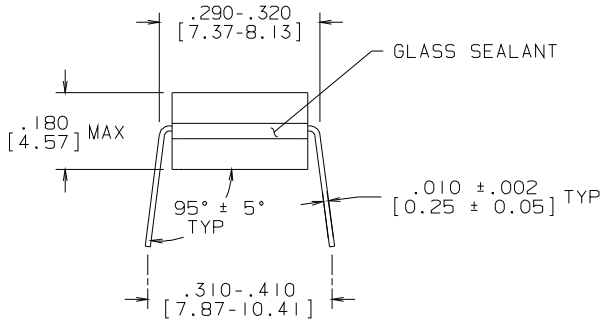
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-E20A	E

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	09996	09/15/93	TL/







MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AD, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH
[MM]

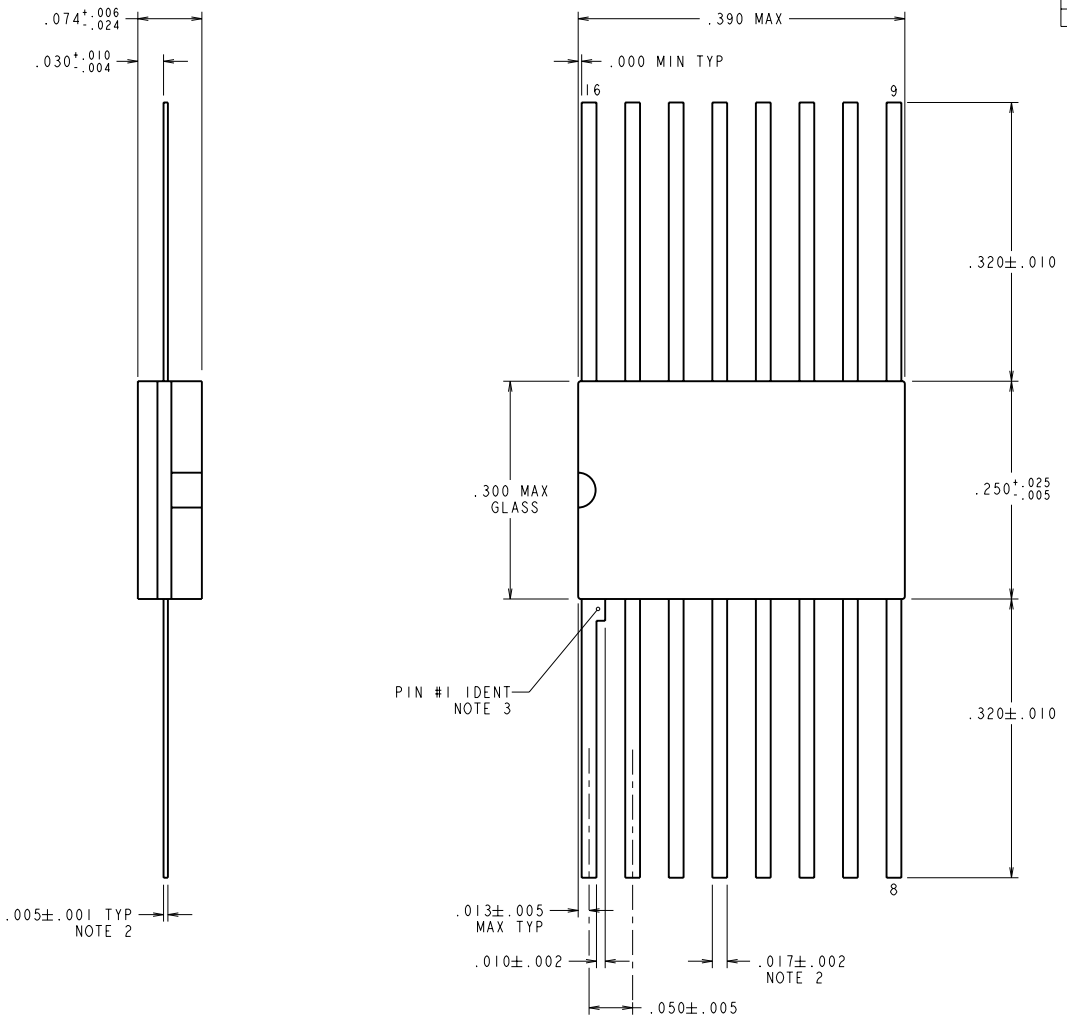
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 16 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J16A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
K	REVISE AND REDRAW PER NEW STANDARD.	10514	07/28/94	DEG/AEP
L	.017±.002 WAS .017±.020.	10656	10/21/94	DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
4. REFERENCE JEDEC REGISTRATION MO-092, VARIATION AC, DATED 04/89.

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: D.E.Grady	07/28/94
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 16 LEAD

PROJECTION

INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-W16A	L

DO NOT SCALE DRAWING | SHEET 1 of 1