National Semiconductor

MICROCIRCUIT DATA SHEET

MNDS90C031-X REV 0D0

Original Creation Date: 06/22/95
Last Update Date: 06/17/98
Last Major Revision Date: 06/22/95

LVDS Quad CMOS Differential Line Driver

General Description

The DS90C031 is a quad CMOS differential line driver designed for applications requiring low power dissipation and high data rates.

The DS90C031 accepts TTL/CMOS input levels and translates them to low voltage (350 mV) differential output siginals. In addition the driver supports a TRI-STATE function that may be used to disable the output stage, thus dropping the device to a low idle power state.

The DS90C031 and companion line receiver (DS90C032) provide a new alternative to high power pseudo-ECL devices for high speed point-to-point interface applications.

Industry Part Number

DS90C031

NS Part Numbers

DS90C031E-QML*
DS90C031W-QML**

Prime Die

DS90C031

Controlling Document

5962-9583301Q2A*, QFA**

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{o}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- +/- 350mV differential signaling
- Low power dissipation.
- Low differential skew.
- Low propagation delay
- Military operating temprature range
- Pin compatible with DS26C31.
- Compatible with IEEE 1596.3 SCI LVDS standard
- Compatible with proposed TIA LVDS standard
- Typical Rise/Fall time is TBD

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage (Vcc)	-0.3 to +6V
Input Voltage (Din)	-0.3 to (Vcc+0.3V)
Enable Input Voltage (EN, EN*)	-0.3 to (Vcc+0.3V)
Output Voltage (Dout+, Dout-)	-0.3 to (Vcc+0.3v)
Storage Temperature Range	-65C to +150C
Lead Temperature Soldering (4 sec)	260C
Maximum Package Power Dissipation @ +25C (Note 2)	
20 PIN LCC (E Pkg)	1900 mW
16 PIN CERPAK (W Pkg)	1450 mW
Thermal Resistance. (Theta JA)	
20 PIN LCC (E Pkg)	78 C/W
16 PIN CERPAK (W Pkg)	145 C/W
Thermal Resistance. (Theta JC)	
20 PIN LCC (E Pkg)	18 C/W
16 PIN CERPAK (W Pkg)	14 C/W
ESD Rating.	3500 Volts.

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
Note 2: Derate (E Pkg) @ 12.8mW/C above +25C. Derate (W Pkg) @ 6.9 mW/C above +25C.

Recommended Operating Conditions

Supply Voltage	4.5 to 5.5 V
Operating Free Air Temperature	-55 to +125 C

Electrical Characteristics

DC PARAMETERS

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vod1	Differential Ouput Voltage	RL = 100 Ohms		Dout-, Dout+	250	450	mV	1, 2, 3
DVod1	Change in Magnitude of Vod1 for complementary output States	RL = 100 Ohms		Dot-, Dout+		35	mV	1, 2, 3
Vos	Offset Voltage	RL = 100 Ohms		Dout-, Dot+	1.125	1.375	mV	1, 2, 3
DVos	Change in Magnitude of Vos for Complementary Output States	RL = 100 Ohms		Dout-, Dot+		25	mV	1, 2, 3
Voh	Output Voltage High	RL = 100 Ohms		Dout-, Dot+		1.6	V	1, 2, 3
Vol	Output Voltage Low	RL = 100 Ohms		Dout-, Dot+	.9		V	1, 2, 3
Vih	Input Voltage High		1	Din, EN, EN*	2.0	Vcc	V	1, 2, 3
Vil	Input Voltage Low		1	Din, EN, EN*	Gnd	0.8	V	1, 2, 3
Ii	Input Current	Vin = Vcc, Gnd, 2.5, or 0.4V		Din, EN, EN*		$\pm$10	uA	1, 2, 3
Vcl	Input Clamp Voltage	Icl = -18mA		Din, EN, EN*		-1.5	V	1, 2, 3
Ios	Output Short Circuit Current	Vout = 0V		Dout-, Dout+		-5.0	mA	1, 2, 3
Ioz	Output TRI-STATE Current	EN = 0.8V and EN* = 2.0V VOUT = 0V or VCC		Dout-, Dout+		$\pm$10	uA	1, 2, 3
Icc	Drivers Enabled Supply Current	Din = Hi or Low		Vcc		25	mA	1, 2, 3
Iccz	Drivers Disabled Supply Current.	Din = Hi or Low, En = Gnd, En* = Vcc		Vcc		10	mA	1, 2, 3

Electrical Characteristics

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: VCC = 4.5/5.0V/5.5V, RL = 100 Ohms (Between outputs), CL = 20pF (Each output to GND)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tPHLD	Differential Propagation Delay High to Low				0.5	5.0	ns	9, 10, 11
tPLHD	Differential Propagation Delay Low to High				0.5	5.0	ns	9, 10, 11
tSKD	Differential Skew |tPHLD-tPLHD|					3	ns	9, 10, 11
tSK1	Channel to Channel Skew		2			3	ns	9, 10, 11
tSK2	Chip to Chip Skew		3			4.5	ns	9, 10, 11
tPHZ	Disable Time High to Z		4			20	ns	9, 10, 11
tPLZ	Disable Time Low To Z		4			20	ns	9, 10, 11
tPZH	Enable Time Z to High		4			20	ns	9, 10, 11
tPZL	Enable Time Z to Low		4			20	ns	9, 10, 11

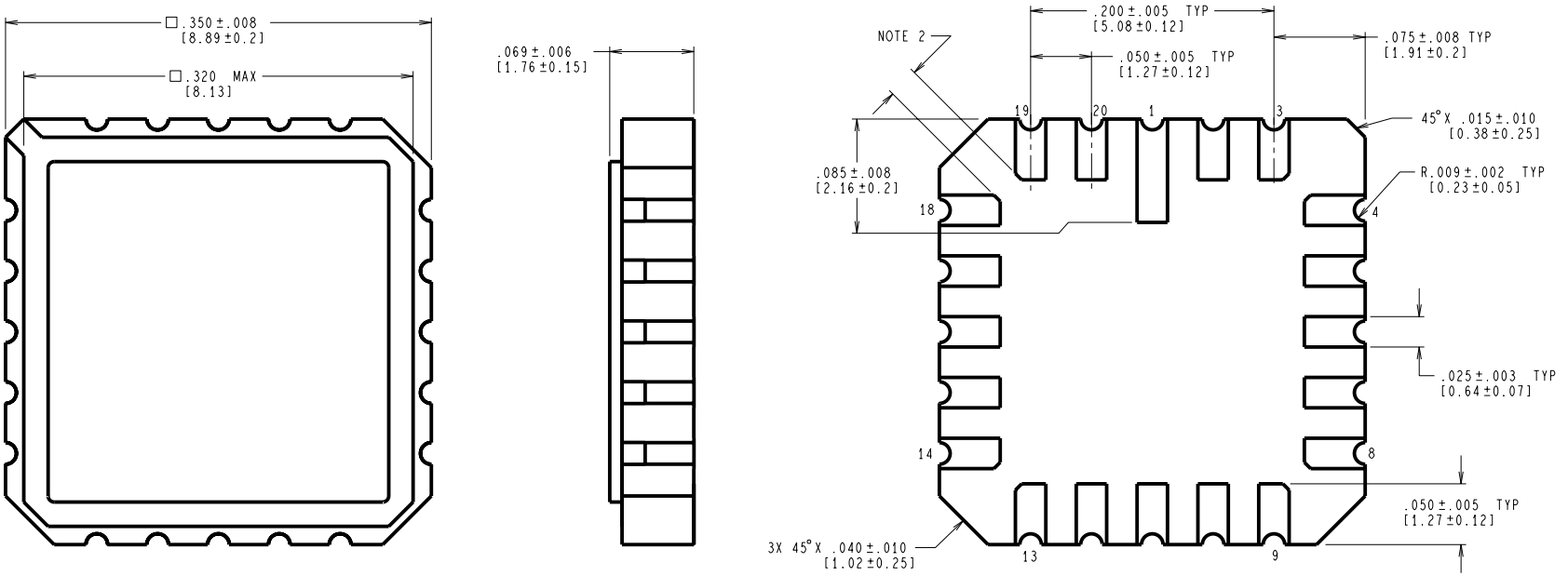
Note 1: Tested during VOH/VOL tests.
Note 2: Channel to Channel Skew is defined as the difference between the propagation delay of one channel and that of the others on the same chip with an event on the inputs.
Note 3: Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.
Note 4: Parameter guaranteed, not tested 100%

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
E20ARE	LCC (E), TYPE C, 20 TERMINAL(P/P DWG)
W16ARL	CERPACK (W), 16 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
E	REVISE AND REDRAW.	10005	02/10/94	DEG/



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

   a. 50 MICROINCHES/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICROINCHES/1.27-8.89 MICROMETERS NICKEL.

   b. SOLDER DIP.
   SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.

2. CORNER PADS MAY HAVE A 45°X.020IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE .015IN/0.38mm DIMENSION.

4. REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

MIL/AERO
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: Dwayne Grady	02/10/94
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION INCH [MM]

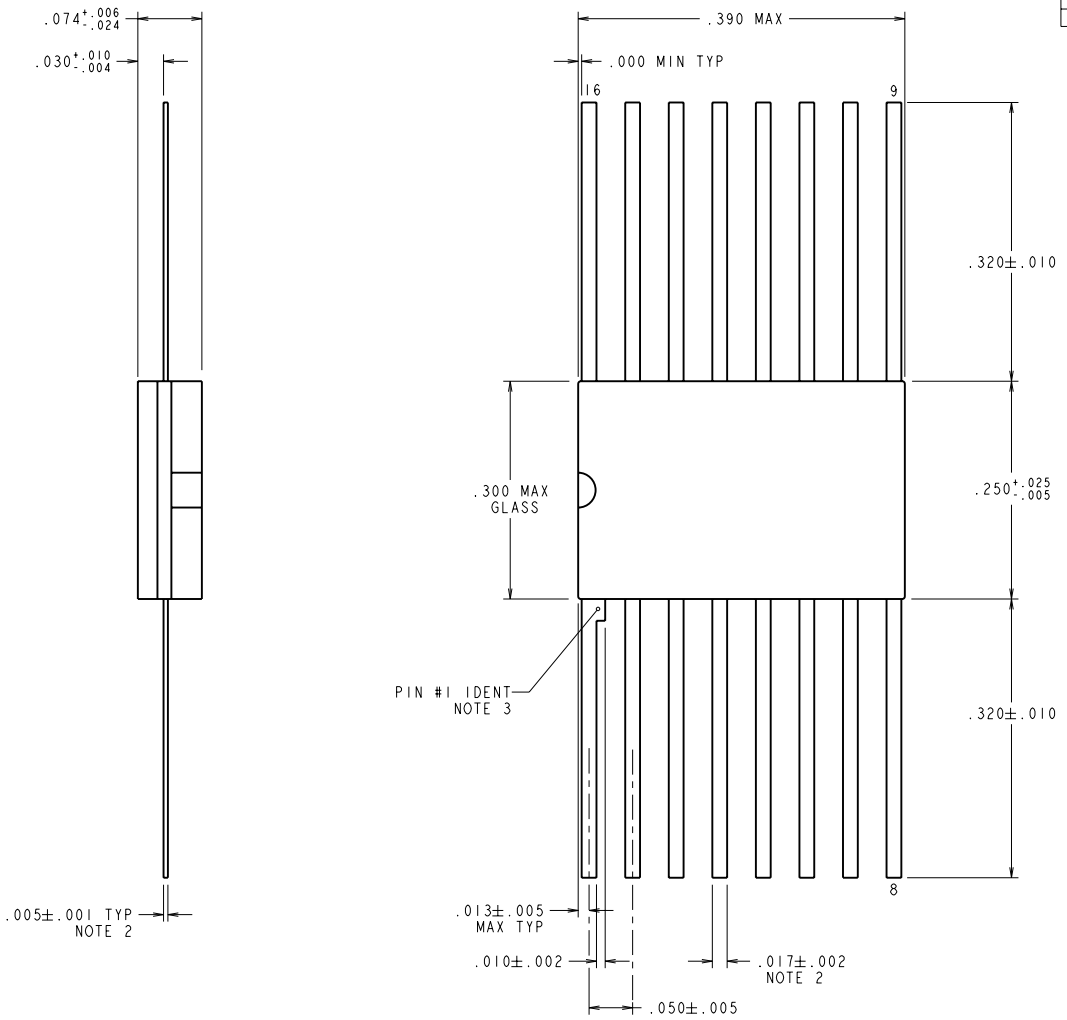
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-E20A	E

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
K	REVISE AND REDRAW PER NEW STANDARD.	10514	07/28/94	DEG/AEP
L	.017±.002 WAS .017±.020.	10656	10/21/94	DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
4. REFERENCE JEDEC REGISTRATION MO-092, VARIATION AC, DATED 04/89.

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: D.E.Grady	07/28/94
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 16 LEAD

PROJECTION

INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-W16A	L

DO NOT SCALE DRAWING | SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0C0	M0002700	06/17/98	Mike Fitzgerald	1). Add NS Part Numbers DS90C031E-QML, and DS90C031W-QML, and remove DS90C031E-MPR. 2). Added Max Power Dissipation for the W pkg, and Thermal Resistance ratings for both E and W pkgs.
0D0	M0002914	06/17/98	Mike Fitzgerald	Revised thermal resistance ratings and derate factor for the W-pkg.