National Semiconductor

MICROCIRCUIT DATA SHEET

MNCLC420A-X REV 0A0

Original Creation Date: 04/07/98
Last Update Date: 02/03/99
Last Major Revision Date: 04/07/98

HIGH SPEED, VOLTAGE FEEDBACK OPERATIONAL AMPLIFIER

General Description

The CLC420A is an operational amplifier designed for applications requiring matched inputs and integration or transimpedance amplification. Utilizing voltage feedback architecture, the CLC420A offers a 300MHz bandwidth, a 1100V/us slew rate and a 4mA supply current (power consumption of 40mW, ±5V supplies).

Applications such as differential amplifiers will benefit from 70dB common mode rejection ratio and an input offset current of 0.2uA(typ). With its unity-gain stability, 2pA/SqRtHz current noise(typ), combined with a settling time of 18ns to 0.01% make the CLC420A ideal for D/A converters, pin diode receivers and photo multiplier amplifiers. All applications will find 70dB power supply rejection ratio attractive.

Industry Part Number

CLC420A

NS Part Numbers

CLC420AE-QML
CLC420AJ-QML
CLC420AWG-QML

Prime Die

UB1366A

Controlling Document

SEE FEATURES SECTION

Processing

(blank)

Quality Conformance Inspection

(blank)

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 300MHz small signal bandwidth
- 1100V/us slew rate
- Unity-gain stability
- Low distortion, -60dBc at 20MHz
- 0.01% settling in 18ns
- 0.2uA input offset current
- 2pASqRtHz current noise
- Controlling Document-

CLC420AJ-QML	5962-9175801MPA
CLC420AE-QML	5962-9175801M2A
CLC420AWG-QML	5962-9175801MXA

Applications

- Active filters/integrators
- Differential amplifiers
- Pin diode receivers
- Log amplifiers
- D/A converters
- Photo multiplier amplifiers

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage (V±)		±7 Vdc
Output Current (Iout)		70 mA
Common Mode Input Voltage (Vcm)		V±
Differential Input Voltage		10 V
Power Dissipation (Pd) (Note 2)		112 mW
Thermal Resistance		
(ThetaJA) Junction to Ambient		
LCC	(Still Air)	100 C/W
	(500 LFPM)	68 C/W
Ceramic DIP	(Still Air)	125 C/W
	(500 LFPM)	72 C/W
Ceramic SOIC	(Still Air)	205 C/W
	(500 LFPM)	125 C/W
(ThetaJC) Junction to Case		
LCC		25 C/W
Ceramic DIP		23 C/W
Ceramic SOIC		24 C/W
Junction Temperature (Tj)		+175 C
Storage Temperature Range		-65 C to +150 C
Lead Temperature (Soldering, 10 seconds)		+300 C
Package Weight (Typical)		
Ceramic SOIC		220 mg
Ceramic DIP		1075 mg
LCC		470 mg
ESD Tolerance (Note 3)		
ESD Rating		2000V

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 100pF discharged through 1.5K Ohms.

Recommended Operating Conditions

Supply Voltage (V±)	±5 Vdc
Gain Range (Av)	±1 to ±10
Ambient Operating Temperature Range (TA)	-55 C to +125 C

Electrical Characteristics

DC PARAMETERS: Open Loop Characteristics

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: V+ = ±5 Vdc, Av = +1, Load Resistance Rl = 100 Ohms, tested parameters use Rs = 500 Ohms, otherwise, feedback resistance (Rf) = 0 Ohms. Temp. Range: -55 C ≤ TA ≤ +125 C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
+Iin	Input Bias Current (NonInverting)				-10	+10	uA	1, 2
					-20	+20	uA	3
-Iin	Input Bias Current (Inverting)				-10	+10	uA	1, 2
					-20	+20	uA	3
Vio	Input Offset Voltage				-2.0	+2.0	mV	1
					-3.5	+3.5	mV	2
					-3.2	+3.2	mV	3
Tc (+Iin)	Average +Input Bias Current Drift		1			60	nA/C	2
			1			120	nA/C	3
Tc (-Iin)	Average -Input Bias Current Drift		1			60	nA/C	2
			1			120	nA/C	3
Tc (Vio)	Average Input Offset Voltage Drift		1			15	uV/C	2, 3
Iio	Input Offset Current					1.0	uA	1
						2.0	uA	2
						2.6	uA	3
Tc (Iio)	Average Input Offset Current Drift		1			10	nA/C	2
			1			20	nA/C	3
Aol	Open Loop Gain				56		dB	1, 2
					52		dB	3
Icc	Quiescent Supply Current (No Load)					5.0	mA	1, 2, 3
PSRR	Power Supply Rejection Ratio	V+ = +4.5V to +5.0V, V- = -4.5V to -5.0V			60		dB	1, 2
					55		dB	3
CMRR	Common Mode Rejection Ratio	Vcm = ±1V			65		dB	1, 2
		Vcm = ±1V			60		dB	3
Rind	Differential Mode Input Resistance		1		1		MOhm	4, 5
			1		0.5		MOhm	6
Cind	Differential Mode Input Capacitance		1			2	pF	4, 5, 6

Electrical Characteristics

DC PARAMETERS: Open Loop Characteristics(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: V+ = +5 Vdc, Av = +1, Load Resistance Rl = 100 Ohms, tested parameters use Rs = 500 Ohms, otherwise, feedback resistance (Rf) = 0 Ohms. Temp. Range: -55 C ≤ TA ≤ +125 C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Rinc	Common Mode Input Resistance		1		0.5		MOhm	4, 5
			1		0.25		MOhm	6
Cinc	Common Mode Input Capacitance		1			2	pF	4, 5, 6
+Vcm	Common Mode Input Voltage		1		+2.8		V	4, 5
			1		+2.5		V	6
-Vcm	Common Mode Input Voltage		1			-2.8	V	4, 5
			1			-2.5	V	6
+Iout	Output Current		1		+50		mA	4, 5
			1		+30		mA	6
-Iout	Output Current		1			-50	mA	4, 5
			1			-30	mA	6
Rout	Output Impedance	At dc	1			0.2	Ohm	4, 5
			1			0.3	Ohm	6
+Vo	Output Voltage Swing	No Load	1		+3		V	1, 2
			1		+2.8		V	3
		Rl = 100 Ohms			+2.5		V	1, 2, 3
-Vo	Output Voltage Swing	No Load	1			-3	V	1, 2
			1			-2.8	V	3
		Rl = 100 Ohms				-2.5	V	1, 2
						-2.2	V	3

Electrical Characteristics

AC PARAMETERS: Frequency Domain Response

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: V+ = +5 Vdc, Av = +1, Load Resistance Rl = 100 Ohms, tested parameters use Rs = 500 Ohms, otherwise, feedback resistance (Rf) = 0 Ohms. Temp. Range: -55 C ≤ TA ≤ +125 C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
GFPL	Gain Flatness Peaking Low	At 0.1 MHz to 100 MHz, Vout < 0.4 Vpp				1.4	dB	4
			2			1.6	dB	5
			2			1.4	dB	6
GFPH	Gain Flatness Peaking High	At 100 MHz, Vout < 0.4 Vpp				3.0	dB	4
			2			3.0	dB	5
			2			5.0	dB	6
GFR	Gain Flatness Rolloff	At 0.1 MHz to 100 MHz, Vout < 0.4 Vpp	1			1.0	dB	4, 6
			1			2.0	dB	5
		At 0.1 MHz to 30 MHz, Av = -1, Rf = 500 Ohms, Vout < 0.4 Vpp				1.4	dB	4
			2			1.6	dB	5
			2			1.4	dB	6
SSBW	Small Signal Bandwidth	-3dB bandwidth, Vout < 0.4 Vpp	1		200		MHz	4, 6
			1		130		MHz	5
		-3dB bandwidth, Av = -1, Rf = 500 Ohms, Vout < 0.4 Vpp			65		MHz	4
			2		65		MHz	6
			2		45		MHz	5
LSBW	Large Signal Bandwidth	-3dB bandwidth, Vout < 5Vpp	1		25		MHz	4
			1		20		MHz	5, 6
		-3dB bandwidth, Av = -1, Rf = 500 Ohms, Vout < 5 Vpp	1		35		MHz	4
			1		30		MHz	5, 6
Lpd	Linear Phase Deviation	At 0.1 MHz to 100 MHz	1			1.8	Deg.	4, 6
			1			2.5	Deg.	5

Electrical Characteristics

AC PARAMETERS: Distortion and Noise

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: V+ = +5 Vdc, Av = +1, Load Resistance Rl = 100 Ohms, tested parameters use Rs = 500 Ohms, otherwise, feedback resistance (Rf) = 0 Ohms. Temp. Range: -55 C ≤ TA ≤ +125 C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
HD2	2nd Harmonic Distortion	2 Vpp at 20 MHz	1			-40	dBc	4
			1			-40	dBc	5, 6
		2 Vpp at 20 MHz, Av = -1				-40	dBc	4
			2			-40	dBc	5, 6
HD3	3rd Harmonic Distortion	2 Vpp at 20 MHz	1			-45	dBc	4, 6
			1			-40	dBc	5
		2 Vpp at 20 MHz, Av = -1				-40	dBc	4
			2			-35	dBc	5
			2			-40	dBc	6
Vn	Input Referred Noise Voltage	At 1 MHz to 200 MHz	1			5.3	mV/Hz	4, 6
			1			6	mV/Hz	5
Icn	Input Referred Noise Current	At 1 MHz to 200 MHz	1			2.6	pA/Hz	4
			1			2.3	pA/Hz	5
			1			2.9	pA/Hz	6

Electrical Characteristics

AC PARAMETERS: Time Domain Response

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: V± = ±5 Vdc, Av = +1, Load Resistance Rl = 100 Ohms, tested parameters use Rs = 500 Ohms, otherwise, feedback resistance (Rf) = 0 Ohms. Temp. Range: -55 C ≤ TA ≤ +125 C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Trs	Rise and Fall Time	0.4 V step, Cl < 10pF, measured between 10% and 90% points	1			2	nS	9, 11
			1			3	nS	10
		0.4 V step, Av = -1, Rf = 500 Ohms, Cl < 10 pF, measured between 10% and 90% points	1			5.5	nS	9, 11
			1			7.8	nS	10
Trl	Rise and Fall Time	5 V step Cl < 10 pF, measured between 10% and 90% points	1			20	nS	9, 10
			1			25	nS	11
		5 V step, Av = -1, Rf = 500 Ohms, Cl < 10 pF, measured between 10% and 90% points	1			9.5	nS	9
			1			10	nS	10, 11
Ts	Settling Time	2V step at 0.01% of the final value, Cl < 10 pF	1			25	nS	9, 10, 11
		2V step at 0.1% of the final value, Cl < 10 pF	1			18	nS	9, 10, 11
Os	Overshoot	0.4 V step, Cl < 10 pF	1			25	%	9, 10
			1			35	%	11
+Sr	Slew Rate	Rising edge, Measured ±1 V with 5 V step, Cl < 10 pF	1		750		V/uS	9
		Rising edge, Measured ±1 V with 5 V step, Cl < 10 pF	1		600		V/uS	10, 11
		Rising edge, Av = -1, Measured ±1 V with 5 V step, Rf = 500 Ohms, Cl = < 10 pF	1		500		V/uS	9
		Rising edge, Av = -1, Measured ±1 V with 5 V step, Rf = 500 Ohms, Cl = < 10 pF	1		430		V/uS	10, 11
-Sr	Slew Rate	Falling Edge, Measured ±1 V with 5 V step, Cl < 10 pF	1		750		V/uS	9
		Falling Edge, Measured ±1 V with 5 V step, Cl < 10 pF	1		600		V/uS	10, 11
		Falling Edge, Av = -1, Measured ±1 V with 5 V step, Rf = 500 Ohms, Cl < 10 pF	1		500		V/uS	9
		Falling Edge, Av = -1, Measured ±1 V with 5 V step, Rf = 500 Ohms, Cl < 10 pF	1		430		V/uS	10, 11

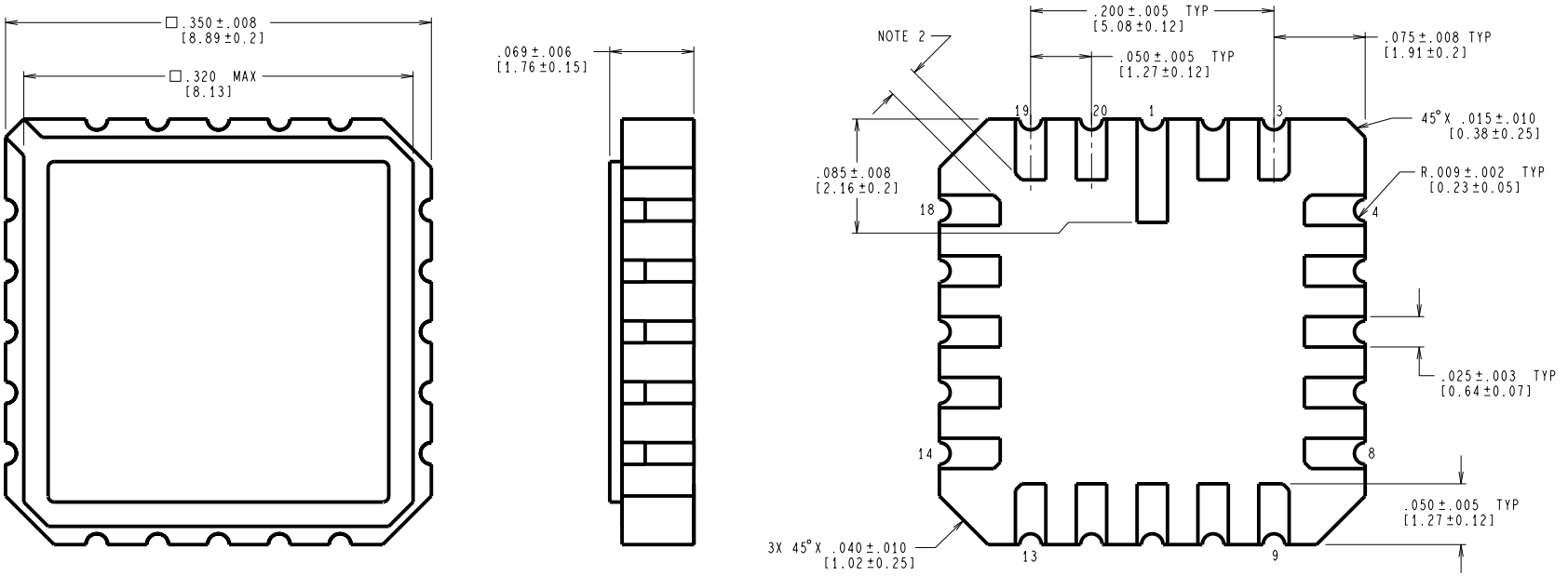
Note 1: If not tested, shall be guaranteed to the limits specified in table I herein.
Note 2: Group A testing only.
Note 3: The algebraic convention, whereby the most negative value is a minimum and the most positive is a maximum, is used in this table. Negative current shall be defined as conventional flow out of a device terminal.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
07070HRA2	CERAMIC SOIC (WG), 10 LEAD (B/I CKT)
07081HRA3	CERDIP (J), 8 LEAD (B/I CKT)
07086HRA2	LCC (E), TYPE C, 20 TERMINAL (B/I CKT)
E20ARE	LCC (E), TYPE C, 20 TERMINAL(P/P DWG)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000376A	CERAMIC SOIC, 10 LEAD (PINOUT)
P000430A	CERDIP (J), 8 LEAD (PINOUT)
P000444A	LCC (E), TYPE C, 20 TERMINAL (PINOUT)
WG10ARC	CERAMIC SOIC (WG), 10 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
E	REVISE AND REDRAW.	10005	02/10/94	DEG/



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

   a. 50 MICROINCHES/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICROINCHES/1.27-8.89 MICROMETERS NICKEL.

   b. SOLDER DIP.
   SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.

2. CORNER PADS MAY HAVE A 45°X.020IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE .015IN/0.38mm DIMENSION.

4. REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

MIL/AERO
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: Dwayne Grady	02/10/94
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION INCH [MM]

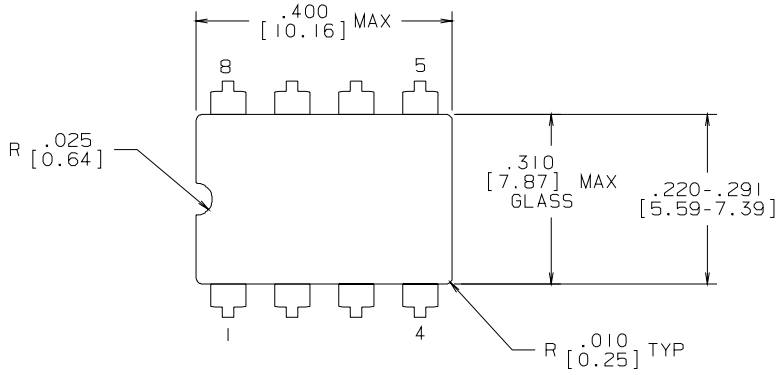
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

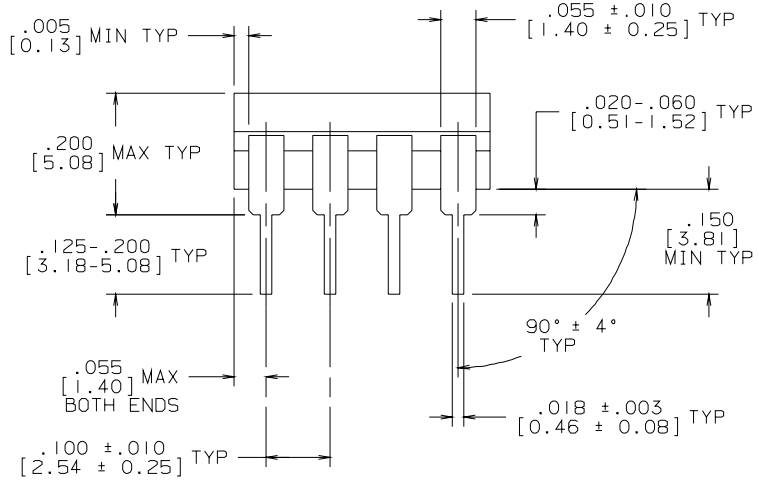
LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL

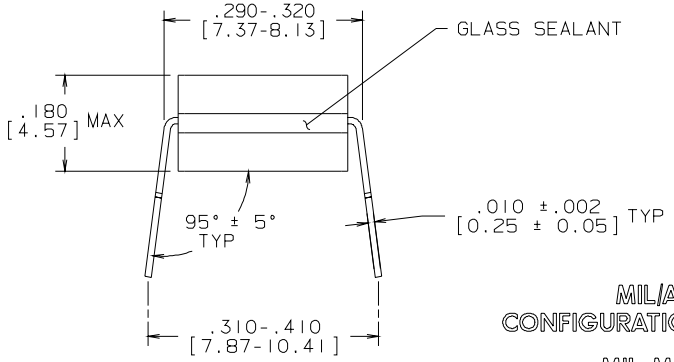
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-E20A	E

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

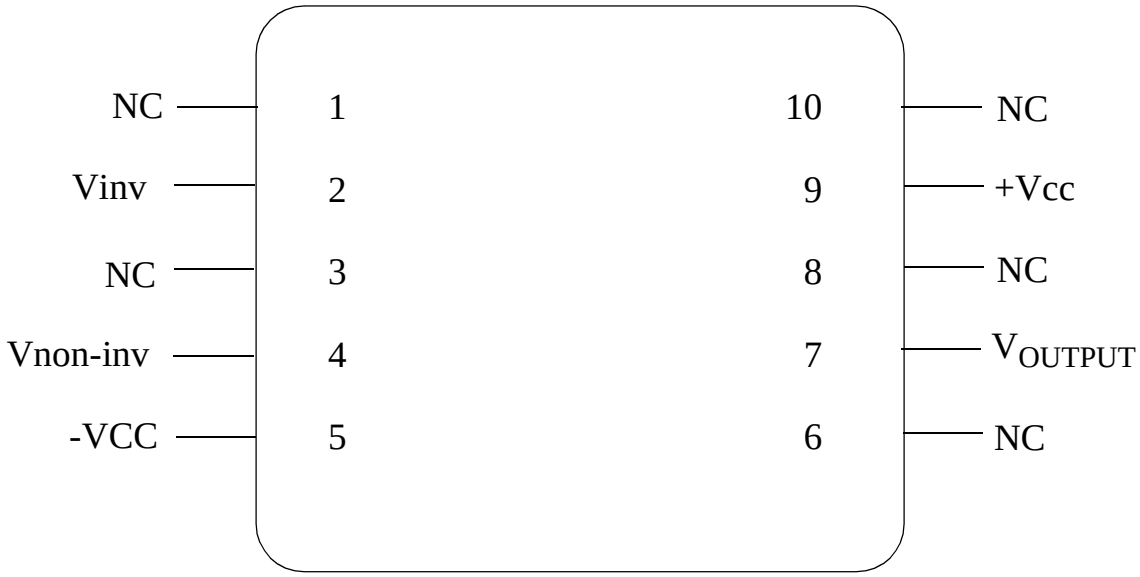
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



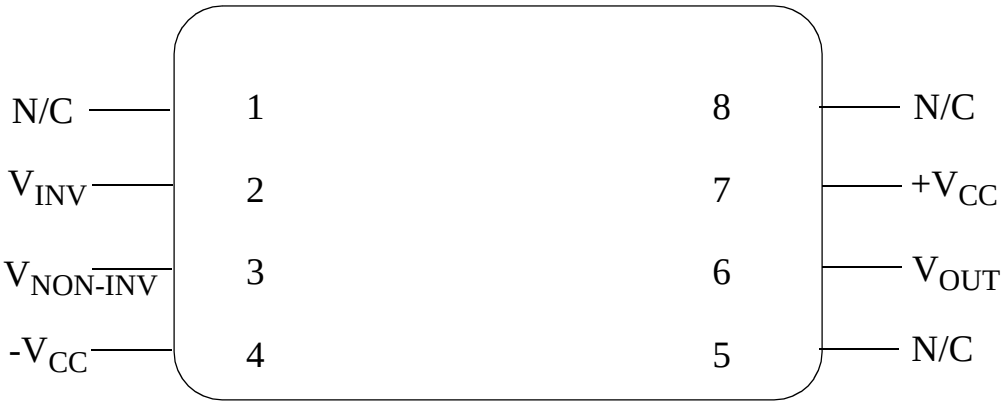
CLC420AWG-QML

10 - LEAD CERAMIC SOIC

CONNECTION DIAGRAM
TOP VIEW

P000376A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



CLC420J

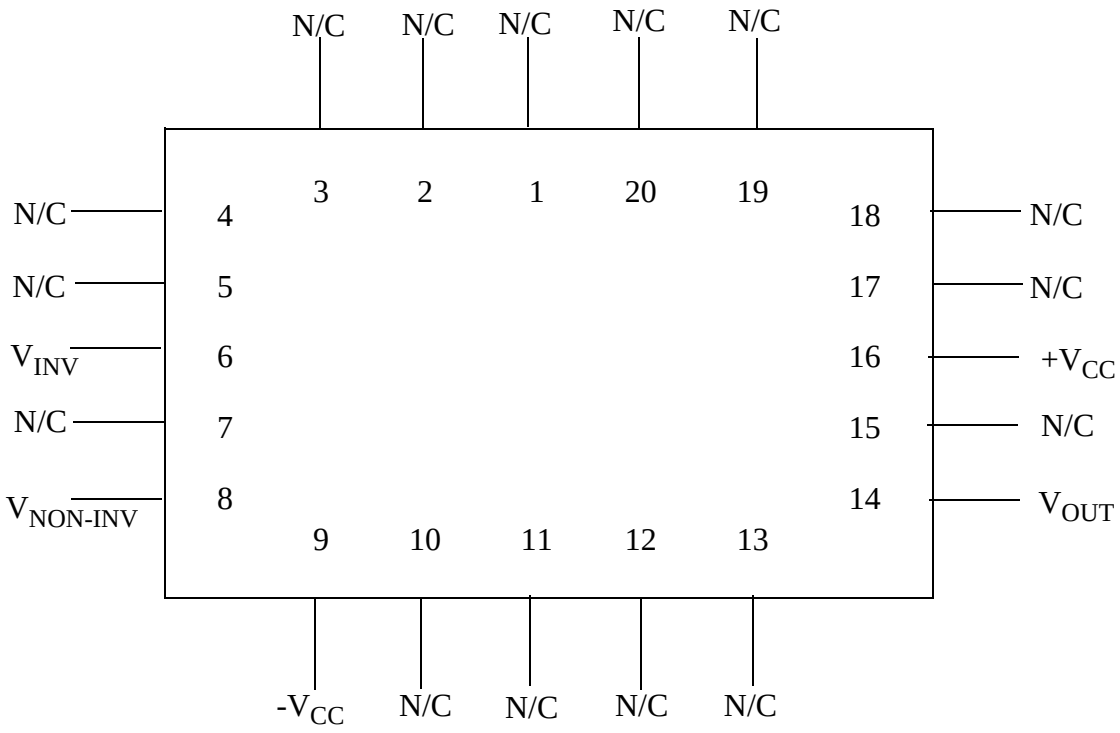
8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000430A

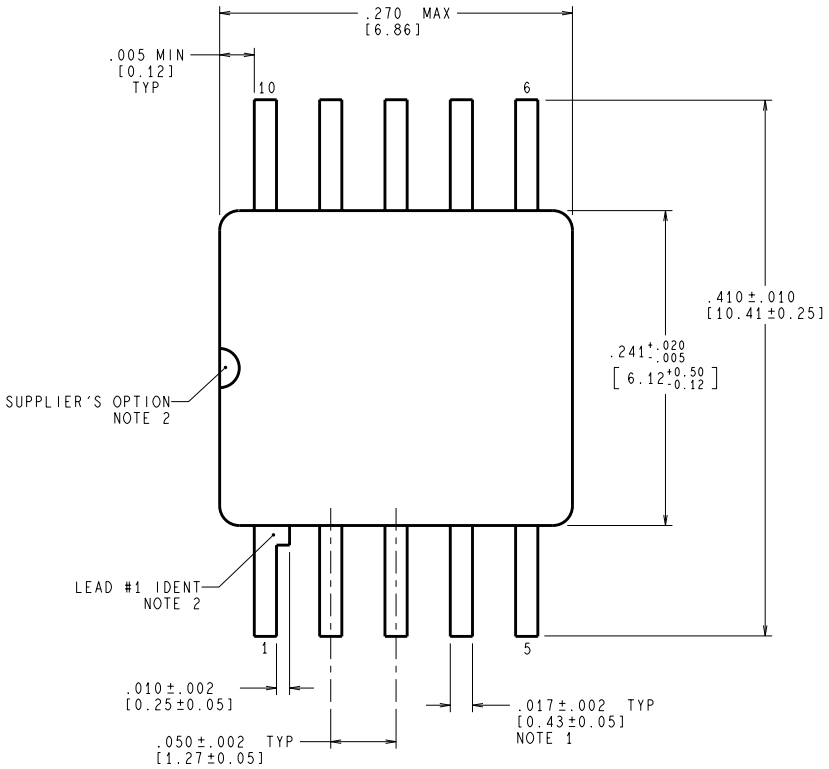
National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

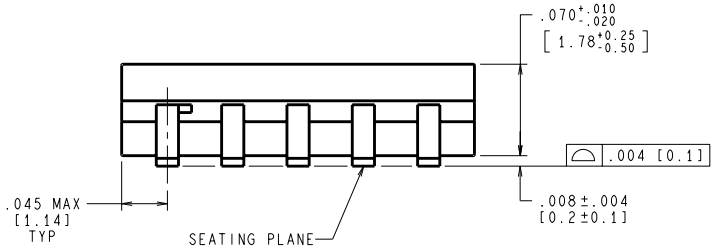


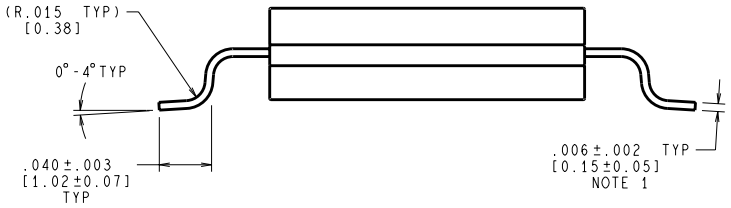
CLC420E
20 - LEAD LCC
CONNECTION DIAGRAM
TOP VIEW
P000444A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11374	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002 DIM .040±.003 WAS .037±.003	11441	04/19/1996	MS/KH
C	R .015[0.38] WAS R .006[0.15]	11838	10/08/1997	TL/







NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 10 LEAD, GULL WING

PROJECTION
INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-WG10A	C

DO NOT SCALE DRAWING | SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003230	02/03/99	Shaw Mead	Initial MDS Release -TRL typo corrected. -Controlling Document format change.