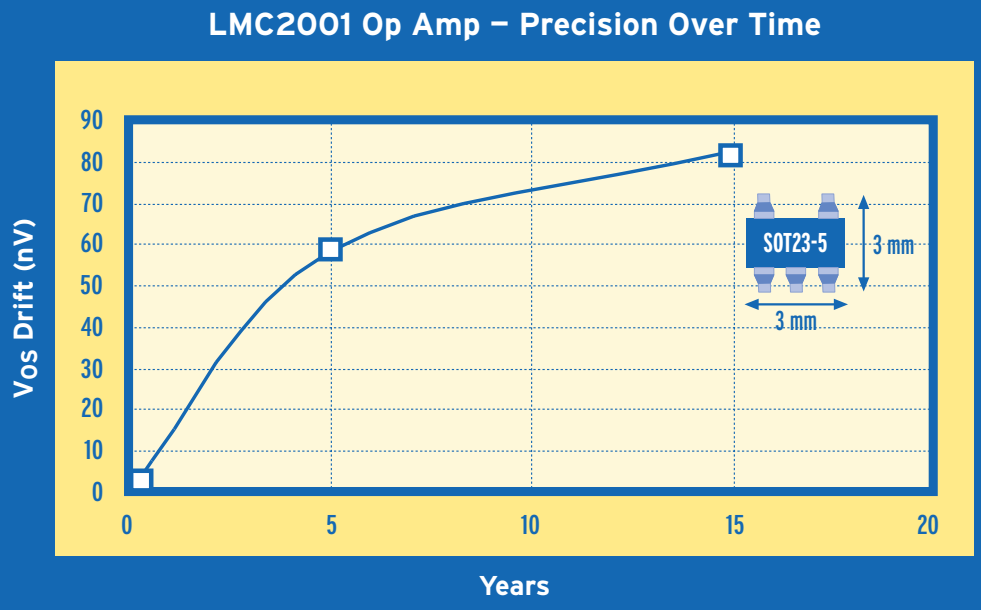
LMC2001 Qualification Package

Precision Over Time

LMC2001 Op Amp



Industry's most precise Op Amp ever in a very small package – the SOT23-5.

- V_{OS} Drift: 5µV Over 10 Years Guaranteed!
- No 1/f Noise at Any Frequency
- 6MHz Gain Bandwidth Product 750µA Supply Current @ 5V
- SOT23-5 Packaging

National Semiconductor

National
Semiconductor

LMC2001
QUALIFICATION PACKAGE

Fall 1998

Table of Contents

1.0 INTRODUCTION

1.1 General Product Description

This qualification booklet covers a general purpose Op Amp. It is available in 2 different package.

Single Op Amp	LMC2001ACM5/ACM5X (5 lead SOT-23 package) LMC2001AIM/AIMX (8 lead SOIC package)

It features low voltage operation (4.75V to 5.25V) and is designed for applications where low power, small size, and price are main objectives. LMC2001 Op Amp offers enhanced performance over that of the OP0x series Op Amps. The LMC2001 offers precision at a price you can afford.

1.2 Technical Product Description

The LMC2001 is manufactured using National's advanced Submicron Silicon Gate BiCMOS process. The Internal name for this process is CS80CBi, which uses 6-inch wafers.

The LMC2001 is a unique precision amplifier which features a low (<40µV) offset combined with a high 6MHz-gain bandwidth. The LMC2001 still fits in an SOT23-5 package and combines excellent precision performance with a superb transient response. The LMC2001 can therefore be used in dynamic applications where conventional chopper amplifiers could not deliver the desired AC performance. The quiescent current is still a mere 750µA. The LMC2001 obtains these features by using a proprietary dynamic offset correction technique and will meet full precision spec within 30ms of power-up. This technique offers continuous offset correction, eliminating offset drift caused by supply voltage and temperature changes.

1.3 Reliability/Qualification Overview

LMC2001

Because the same wafer fab process and package types are used on the LMV324 product, LMC2001 is qualified by reliability testing and qualified by extension.

Copies of all reliability test reports listed below can be found under Reliability Reports section 5.0 later in this qualification booklet.

Q19960526	LMC2001 in SOT-23 and SOIC

1.4 Technical Assistance

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2.0 DEVICE INFORMATION

2.1 Datasheet

National Semiconductor

October 1998

LMC2001
High Precision, 6MHz Rail-To-Rail Output Operational Amplifier

General Description

The LMC2001 is a new precision amplifier that offers unprecedented accuracy and stability at an affordable price and is offered in miniature (SOT23-5) package. This device utilizes patented techniques to measure and continually correct the input offset error voltage. The result is an amplifier which is ultra stable over time, and temperature. It has excellent CMRR and PSRR ratings, and does not exhibit the familiar 1/f voltage and current noise increase that plagues traditional amplifiers. The combination of the LMC2001 characteristics makes it a good choice for transducer amplifiers, high gain configurations, ADC buffer amplifiers, DAC I-V conversion, and any other 5V application requiring precision and/or stability.

Other useful benefits of the LMC2001 are rail-to-rail output, low supply current of 750µA, and wide gain-bandwidth product of 6MHz. The LMC2001 comes in 5 pin SOT23 and 8 pin SOIC. These extremely versatile features found in the LMC2001 provide high performance and ease of use.

Features

(Vs = 5V, R_L = 10K to V^+ /2, Typ. Unless Noted)

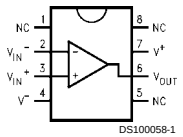
- Low Guaranteed V_{os} 40µV
- e_n With No 1/f 85nV/$\sqrt{Hz}$
- High CMRR 120dB
- High PSRR 120dB
- High A_{VOL} 137dB
- Wide Gain-Bandwidth Product 6MHz
- High Slew Rate 5V/µs
- Low Supply Current 750µA
- Rail-To-Rail Output 30mV from either rail
- No External Capacitors Required

Applications

- Precision Instrumentation Amplifiers
- Thermocouple Amplifiers
- Strain Gauge Bridge Amplifier

Connection Diagrams

8-Pin SO



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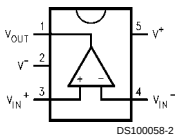
Top View

5-Pin SOT23



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Top View

Ordering Information

Package	Temperature Range		Package Marking	Transport Media	NSC Drawing
	Commercial 0˚C to +70˚C	Industrial −40˚C to +85˚C			
8-pin Small Outline		LMC2001AIM	LMC2001AIM	Rails	M08A
		LMC2001AIMX		2.5K Tape and Reel	
5-pin SOT23-5	LMC2001ACM5		A09A	250 Tape and Reel	MA05B
	LMC2001ACM5X			3K Tape and Reel	

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	2500V
Machine Model	150V
Differential Input Voltage	± Supply Voltage
Supply Voltage (V^+ - V^-)	5.6V
Current At Input Pin	30mA
Current At Output Pin	30mA
Current At Power Supply Pin (Note 3)	50mA
Lead Temperature (soldering, 10 sec)	260˚C
Storage Temperature Range	-65˚C to 150˚C
Junction Temperature (T_J) (Note 4)	150˚C

Operating Ratings (Note 1)

Supply voltage	4.75V to 5.25V
Temperature Range	
LMC2001AI	-40˚C ≤ T_J ≤ 85˚C
LMC2001AC	0˚C ≤ T_J ≤ 70˚C
Thermal resistance (θ_{JA})	
M Package, 8-pin Surface Mount	180˚C /W
M5 Package, SOT23-5	274˚C /W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, V_O = 2.5V and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	(Note 11)	0.5	40 **60**	µV max
	Offset Calibration Time		5	30	ms
TCV_{OS}	Input Offset Voltage	(Note 12)	0.015		µV/˚C
	Long-Term Offset Drift	(Note 8)	0.006		µV/month
	Lifetime V_{OS} drift	(Note 8)	2.5	5	µV Max
I_{IN}	Input Current	(Note 9)	-3		pA
I_{OS}	Input Offset Current		6		pA
R_{IND}	Input Differential Resistance		9		MΩ
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 3.5V	120	100	dB min
		0.1V ≤ V_{CM} ≤ 3.5V	**110**	**90**	dB min
PSRR	Power Supply Rejection Ratio	4.75V ≤ V^+ ≤ 5.25V	120	95 **90**	dB min
A_{VOL}	Large Signal Voltage Gain (Note 7)	R_L= 10kΩ	137	105 **100**	dB min
		R_L = 2kΩ	128	95 **90**	
V_O	Output Swing	R_L = 10kΩ to 2.5V V_{IN}(diff) = ±0.5V	4.975	4.955 **4.955**	V min
			0.030	0.060 **0.060**	V max
		R_L = 2kΩ to 2.5V V_{IN}(diff) = ±0.5V	4.936		V
			0.075		V
I_O	Output Current	Sourcing, V_O = 0V V_{IN}(diff) = ±0.5V	5.9	4.1 **1.5**	mA min
		Sinking, V_O = 5V V_{IN}(diff) = ±0.5V	14.5	4.5 **1.5**	mA min
I_S	Supply Current		0.75	1.0 **1.2**	mA max

AC Electrical Characteristics

T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, V_O = 2.5V, and R_L > 1MΩ.

Symbol	Parameter	Conditions		Typ (Note 5)	Units
SR	Slew Rate	A_V = +1, V_{in}=3.5Vpp		5	V/µs
GBW	Gain-Bandwidth Product			6	MHz
θ_m	Phase Margin			75	Deg
G_m	Gain Margin			12	dB
e_n	Input-Referred Voltage Noise	f = 0.1Hz		85	$nV/\sqrt{Hz}$
e_np-p	Input-Referred Voltage Noise	R_S = 100Ω, DC to 10Hz		1.6	µVpp
i_n	Input-Referred Current Noise	f = 0.1Hz		180	$fA/\sqrt{Hz}$
THD	Total Harmonic Distortion	f = 1kHz, Av = -2 R_L = 10kΩ,V_O = 4.5Vpp		0.02	%
trec	Input Overload Recovery Time			50	ms
T_S	Output Settling time	(Note 10) A_V= +1, 1V step	1%	250	ns
			0.1%	400	
			0.01%	3200	
		(Note 10)A_V= −1, 1V step	1%	80	
			0.1%	860	
			0.01%	1400	

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5kΩ in series with 100pF. Machine model, 200Ω in series with 100pF.

Note 3: Output currents in excess of ±30mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis, unless otherwise noted.

Note 7: V^+ = 5V, V_{CM} = 2.5V, and R_L connected to 2.5V. For Sourcing tests, 2.5V ≤ V_O ≤ 4.8V. For Sinking tests, 0.2V ≤ V_O ≤ 2.5V.

Note 8: Guaranteed Vos Drift is based on 280 devices operated for 1000 hrs at 150°C (equivalent to 30 years 55ºC).

Note 9: Guaranteed by design only.

Note 10: Settling times shown correspond to the worse case (positive or negative step) and does not include slew time. See the Application Note section for test schematic.

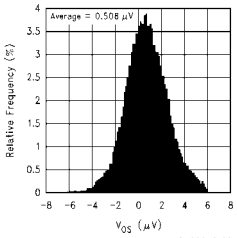
Note 11: The limits are set by the accuracy of high speed automatic test equipment. For the typical V_{OS} distribution, see the curve on page 4.

Note 12: Precision bench measurement of more than 300 units. More than 65% of units had less than 15nV /°C V_{OS} drift.

Typical Performance Characteristics

T_A=25C, V_S= 5V unless otherwise specified.

V_{OS} Distribution



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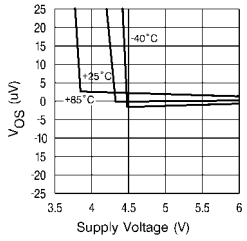
V_{OS} vs V_S



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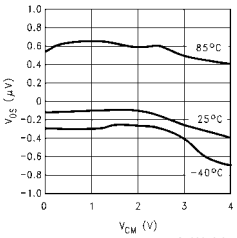
V_{OS} vs V_{CM}



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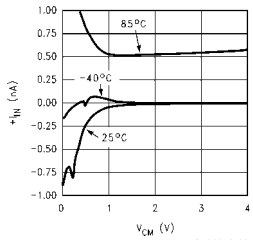
+I_{IN} vs V_{CM}



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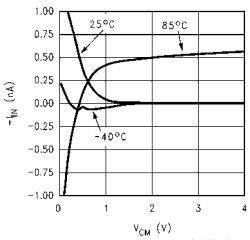
−I_{IN}vs V_{CM}



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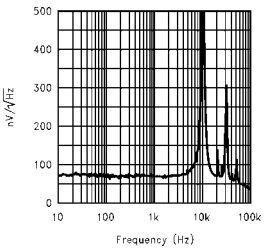
e_N vs Frequency



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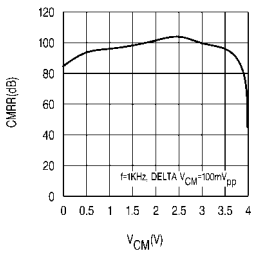
CMR vs V_{CM}



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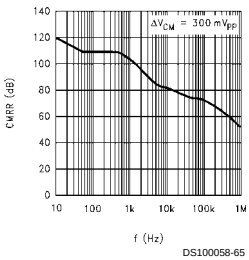
CMR vs Frequency



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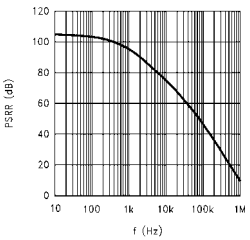
PSR vs Frequency



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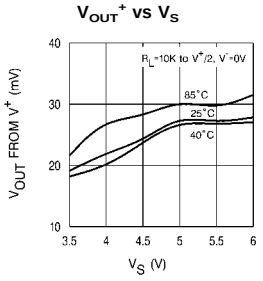
V_{OUT}^+ vs V_S



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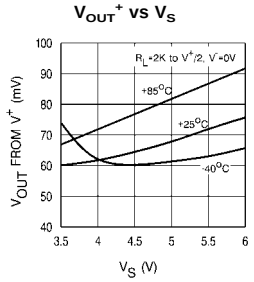
V_{OUT}^+ vs V_S



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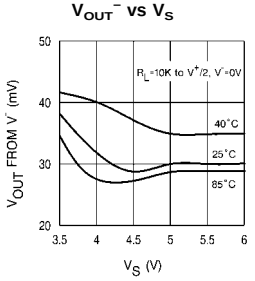
V_{OUT}^- vs V_S



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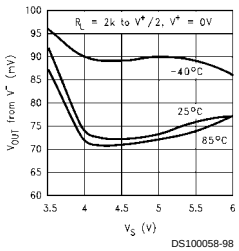
Typical Performance Characteristics (Continued)

V_{OUT}^- vs V_S



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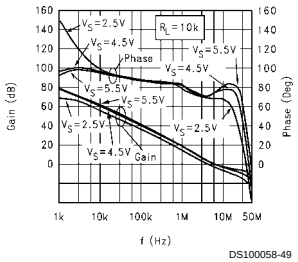
Gain-Phase vs V_S



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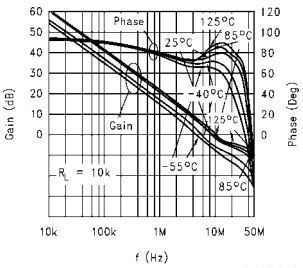
Gain-Phase vs Temp



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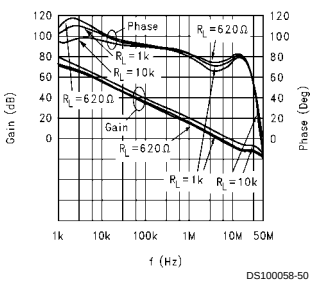
Gain-Phase vs R_L



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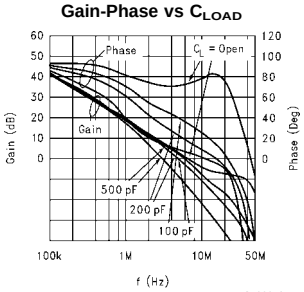
Gain-Phase vs C_{LOAD}



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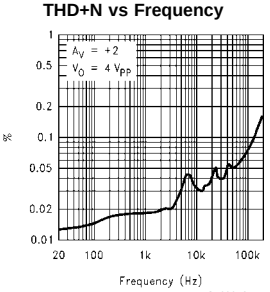
THD+N vs Frequency



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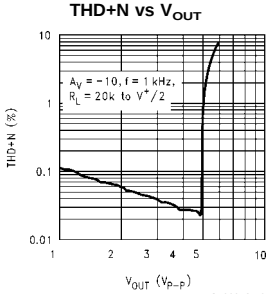
THD+N vs V_{OUT}



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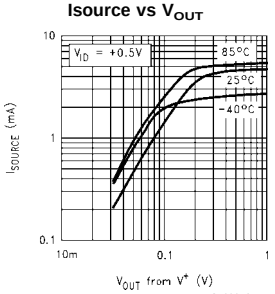
Isource vs V_{OUT}



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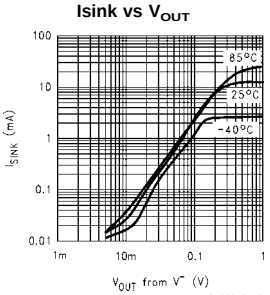
Isink vs V_{OUT}



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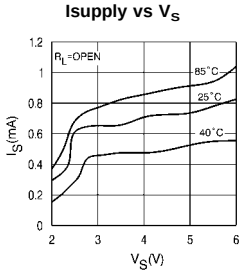
Isupply vs V_S



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Application Notes

The Benefits of LMC2001

No 1/f Noise

Using patented methods, the LMC2001 eliminates the 1/f noise present in other amplifiers. This noise which increases as frequency decreases is a major source of measurement error in all DC coupled measurements. Low frequency noise appears as a constantly changing signal in series with any measurement being made. As a result, even when the measurement is made rapidly, this constantly changing noise signal will corrupt the result. The value of this noise signal can be surprisingly large. For example: If a conventional amplifier has a high frequency noise level of 10nV/$\sqrt{Hz}$ and a noise corner of 10 Hz, the RMS noise at 0.001 Hz is 1µV/$\sqrt{Hz}$

This is equivalent to a 6µV peak-to-peak error. In a circuit with a gain of 1000, this produces a 6mV peak-to-peak output error. This number of 0.001 Hz might appear unreasonably low but when a data acquisition system is operating for 17 minutes it has been on long enough to include this error. In this same time, the LMC2001 will only have a 0.51mV output error. This is more than 13.3 times less error.

Keep in mind that this 1/f error gets even larger at lower frequencies.

At the extreme, many people try to reduce this error by integrating or taking several samples of the same signal. This is also doomed to failure because the 1/f nature of this noise means that taking longer samples just moves the measurement into lower frequencies where the noise level is even higher.

The LMC2001 eliminates this source of error. The noise level is constant with frequency so that reducing the bandwidth reduces the errors caused by noise.

Another source of error that is rarely mentioned is the error voltages caused by the inadvertent thermocouples created when the common “Kovar type” package lead materials are soldered to a copper printed circuit board. These steel based leadframe materials can produce over 35uV/°C when soldered onto a copper trace. This can result in thermocouple noise that is equal to the LMC2001 noise when there is a temperature difference of only 0.0014°C between the lead and the board!

For this reason, the leadframe of the LMC2001 is made of copper. This results in equal and opposite junctions which cancel this effect. The extremely small size of the SOT-23 package results in the leads being very close together. This further reduces the probability of temperature differences and hence decreases thermal noise.

Overload Recovery

The LMC2001 recovers from input overload much faster than most chopper stabilized opamps. Recovery, from driving the amplifier to 2X the full scale output, only requires about 50ms. Most chopper stabilized amplifiers will take from 250ms to several seconds to recover from this same overload. This is because large capacitors are used to store the unadjusted offset voltage.

The wide bandwidth of the LMC2001 enhances performance when it is used as an amplifier to drive loads that inject transients back into the output. A to Ds and multiplexers are examples of this type of load. To simulate this type of load, a pulse generator producing a 1V peak square wave was connected to the output through a 10pF capacitor. (*Figure 1*) The typical time for the output to recover to 1% of the applied pulse is 80ns. To recover to 0.1% requires 860ns. This rapid recovery is due to the wide bandwidth of the output stage and large total GBW.

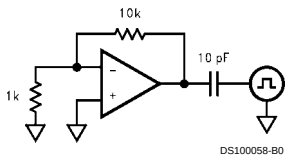


FIGURE 1.

No External Capacitors Required

The LMC2001 does not need external capacitors. This eliminates the problems caused by capacitor leakage and dielectric absorption, which can cause delays of several seconds from turn-on until the amplifier is settled.

More Benefits

The LMC2001 offers the benefits mentioned above and more. It is rail-to-rail output and consumes only 750µA of supply current while providing excellent DC and AC electrical performance. In DC performance, the LMC2001 achieves 120dB of CMRR, 120dB of PSRR and 137dB of open loop gain. In AC performance, the LMC2001 provides 6MHz of gain-bandwidth product and 5V/µs of slew rate.

How the LMC2001 Works

The LMC2001 uses new, patented techniques to achieve the high DC accuracy traditionally associated with chopper stabilized amplifiers without the major drawbacks produced by chopping. The LMC2001 continuously monitors the input offset and corrects this error. The conventional chopping process produces many mixing products, both sums and differences, between the chopping frequency and the incoming signal frequency. This mixing causes large amounts of distortion, particularly when the signal frequency approaches the chopping frequency. Even without an incoming signal, the chopper harmonics mix with each other to produce even more trash. If this sounds unlikely or difficult to understand, look at the plot (*Figure 2*), of the output of a typical (MAX432) chopper stabilized opamp. This is the output when there is no incoming signal, just the amplifier in a gain of -10 with the input grounded. The chopper is operating at about 150Hz, the rest is mixing products. Add an input signal and the mess gets much worse. Compare this plot with *Figure 3* of the LMC2001. This data was taken under the exact same conditions. The auto zero action is visible at about 11kHz but note the absence of mixing products at other frequencies. As a result, the LMC2001 has very low distortion of 0.02% and very low mixing products.

Input Currents

The LMC2001 input current is different than standard bipolar or CMOS input currents in that it appears as a current flowing in one input and out the other. Under most operating conditions, these currents are in the picoamp level and will have little or no effect in most circuits. These currents increase to the nA level when the common-mode voltage is near the minus supply. (see the typical curves) At high temperatures such as 85°C, the input currents become larger, 0.5nA typical, and are both positive except when the Vcm is near V^-. If operation is expected at low common-mode voltages and high temperature, do not add resistance in series with the inputs to balance the impedances. Doing this can cause an increase in offset voltage.

Application Notes (Continued)

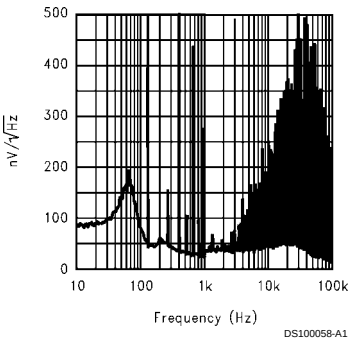


FIGURE 2.

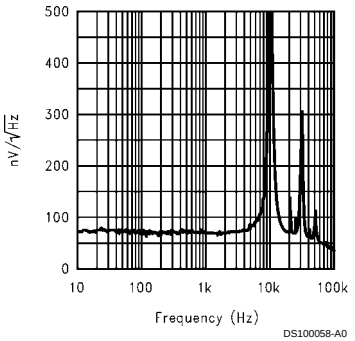


FIGURE 3.

This Strain-Gauge (*Figure 4*) amplifier provides high gain (1006 or 60 dB) with very low offset and drift. Using the resistors tolerance as shown, the worst case CMRR will be greater than 90 dB. The common-mode gain is directly related to the resistor mismatch and is independent of the differential gain that is set by R3. The worst case common-mode gain is −54 dB. This gain becomes even lower, improving CMRR, if the resistor ratio matching is improved.

$$A_V \text{ Diff} = 1 + \frac{R1}{R2} + \frac{2R1}{R3}$$

Extending Supply Voltages and Output Swing by Using a Composite Amplifier Configuration:

In cases where substantially higher output swing is required with higher supply voltages, arrangements like the ones shown in *Figure 5*, and *Figure 6* could be used (pin numbers shown are for SO-8 package). These configurations utilize the excellent DC performance of the LMC2001 while at the same time allow the superior voltage and frequency capabilities of the LM6171 to set the dynamic performance of the overall amplifier. For example, it is possible to achieve ±12V output swing with 300MHz of overall GBW (Av=100) while keeping the worst case output shift due to Vos less than 4mV. The LMC2001 output voltage is kept at about mid-point of it's overall supply voltage and it's input common mode voltage range allows the V^- terminal to be grounded in one case (*Figure 5*, inverting operation) and tied to a small non-critical negative bias in another (*Figure 6*, non-inverting operation). Higher closed loop gains are also possible with a corresponding reduction in realizable bandwidth. Table 1 shows some other closed loop gain possibilities along with the measured performance in each case

Application Circuits

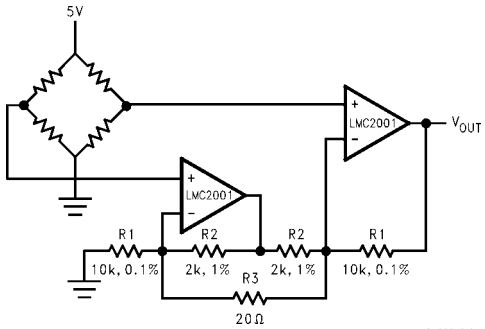


FIGURE 4. Single Supply Strain- Gauge Amplifier

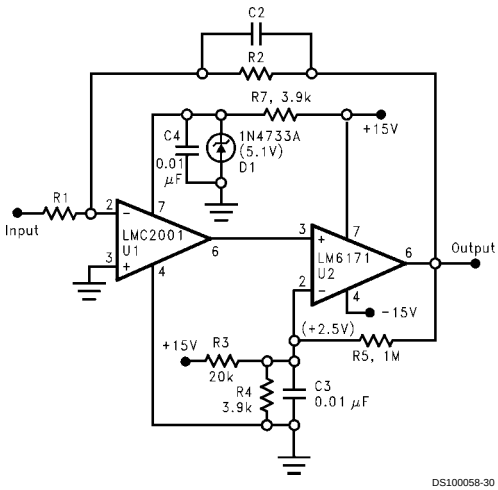


FIGURE 5. Inverting Composite Amplifier

Application Notes (Continued)

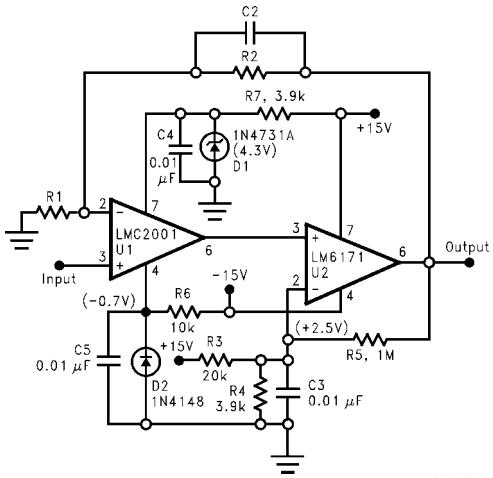


FIGURE 6. Non-Inverting Composite Amplifier

TABLE 1. Composite Amplifier Measured Performance

Av	R1	R2	C2	BW	SR	e_{npp}
	(ohm)	(ohm)	(pF)	(MHz)	(V/us)	(mVpp)
50	200	10K	8	3.3	178	37
100	100	10K	10	2.5	174	70
100	1K	100K	0.67	3.1	170	70
500	200	100K	1.75	1.4	96	250
1000	100	100K	2.2	0.98	64	400

In terms of the measured output peak-to-peak noise, the following relationship holds between output noise voltage, e_{npp}, for different closed loop gain, A_v, settings, where -3dB Bandwidth is BW:

$$\frac{e_{npp1}}{e_{npp2}} = \sqrt{\frac{BW1}{BW2}} \bullet \frac{A_V1}{A_V2} \quad (1)$$

It should be kept in mind that in order to minimize the output noise voltage for a given closed loop gain setting, one could minimize the overall bandwidth. As can be seen from Equation 1 above, the improvement in output noise has a square law relationship to the reduction in BW.

In the case of the inverting configuration, it is also possible to increase the input impedance of the overall amplifier, by raising the value of R1, without having to increase the feedback resistor, R2, to impractical values, by utilizing a "T" network as feedback. See the LMC6442 data sheet (Application Notes section) for more details on this.

LMC2001 as ADC Input Amplifier

The LMC2001 is a great choice for an amplifier stage immediately before the input of an A/D converter (AC or DC coupled) see *Figure 7* and *Figure 8* because of the following important characteristics:

a) Very low offset voltage and offset voltage drift over time and temperature allow a high closed loop gain setting without introducing any short term or long term errors. For example, when set to a closed loop gain of 100 as the analog input amplifier of a 12 bit A/D converter, the overall conversion error over full operation temperature and 30 years life of the part (operating at 50˚C) would be less than 5LSB.

b) Fast large signal settling time to 0.01% of final value (1.4 us) allows 12 bit accuracy at 100KHz or more sampling rate.

c) No flicker (1/f) noise means unsurpassed data accuracy over any measurement period of time, no matter how long. Consider the following opamp performance, based on a typical commercially available device, for comparison:

Opamp flatband noise	$8nV/\sqrt{Hz}$
$1/f^{0.94}$ corner frequency	100Hz
f(max)	100Hz
Av	100
Measurement time	100 sec

The example above, will result in about 3mVpp (2.5LSB) of output noise contribution due to the opamp alone, compared to about 420 uVpp (less than 1LSB) when that opamp is replaced with the LMC2001 which has no 1/f contribution. If the measurement time is increased from 100 sec. to 1 hr., the improvement realized by using the LMC2001 would be a factor of about 44 times (18.5mVpp compared to 420uV when LMC2001 is used) mainly because the LMC2001 accuracy is not compromised by increasing the observation time.

d) Copper lead frame construction minimizes any thermocouple effects which would degrade low level/high gain data conversion application accuracy (see discussion under "The Benefits of the LMC2001" section above).

e) Rail-to-Rail output swing maximized the ADC dynamic range in 5V single supply converter applications. Below are some typical block diagrams showing the LMC2001 used as an ADC amplifier (*Figure 7* and *Figure 8*).

Application Notes (Continued)

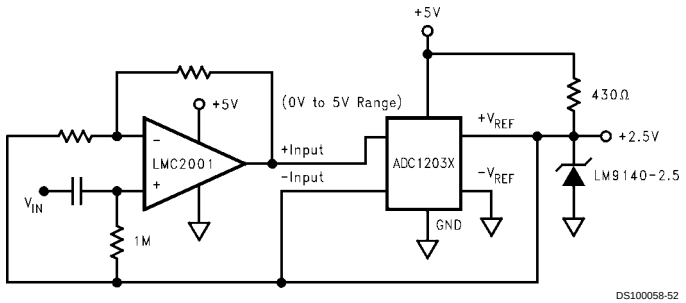


FIGURE 7.

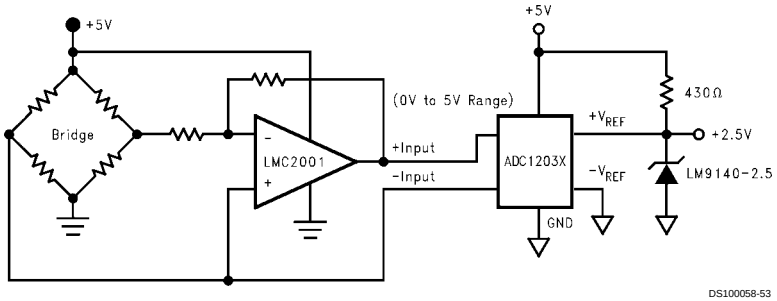
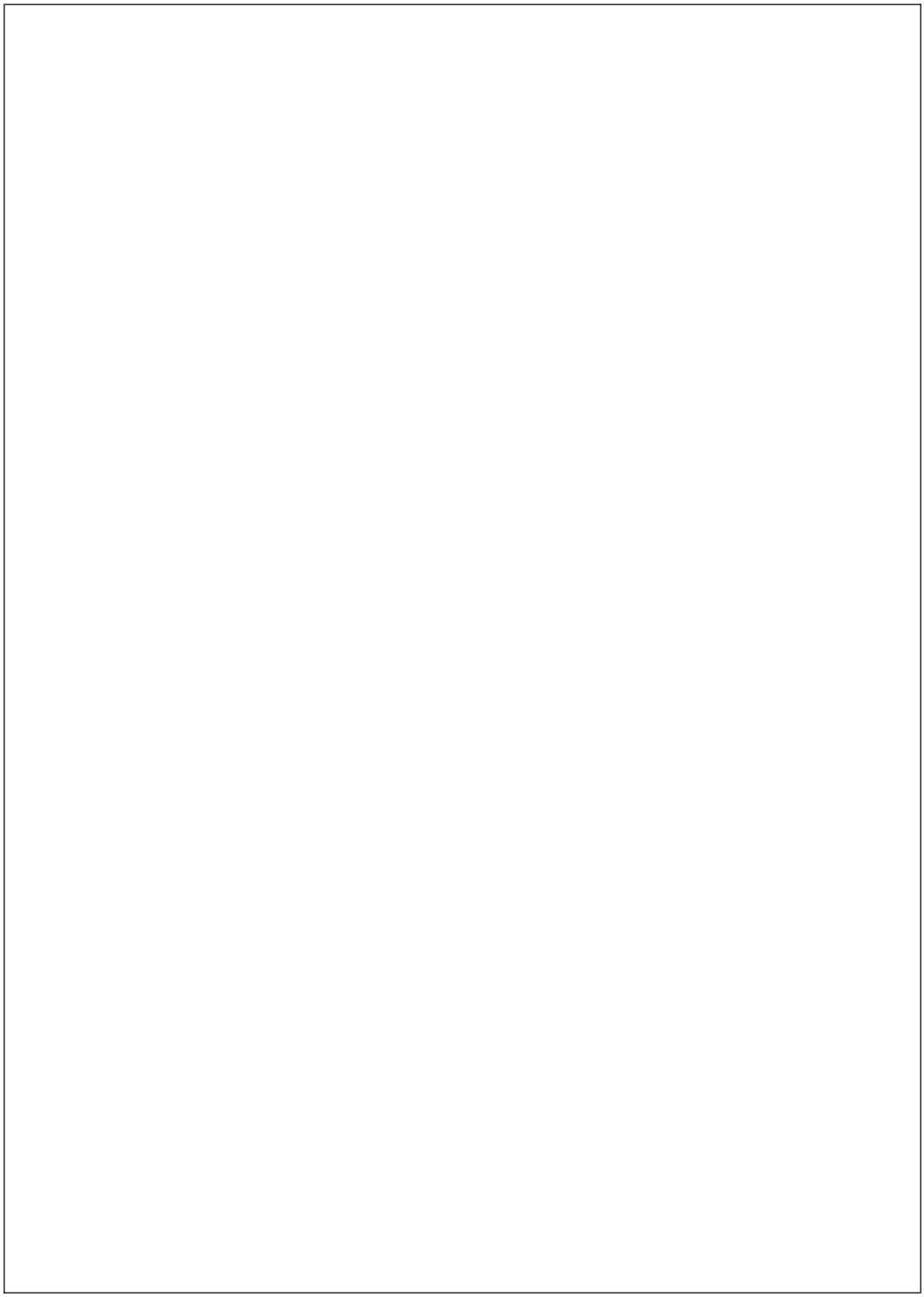
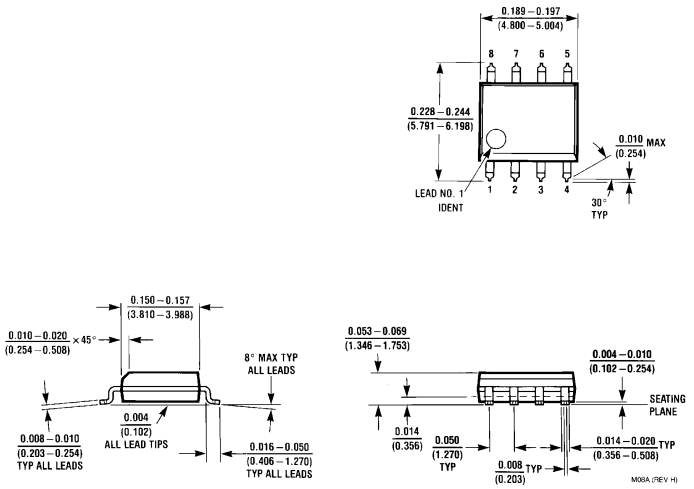


FIGURE 8.



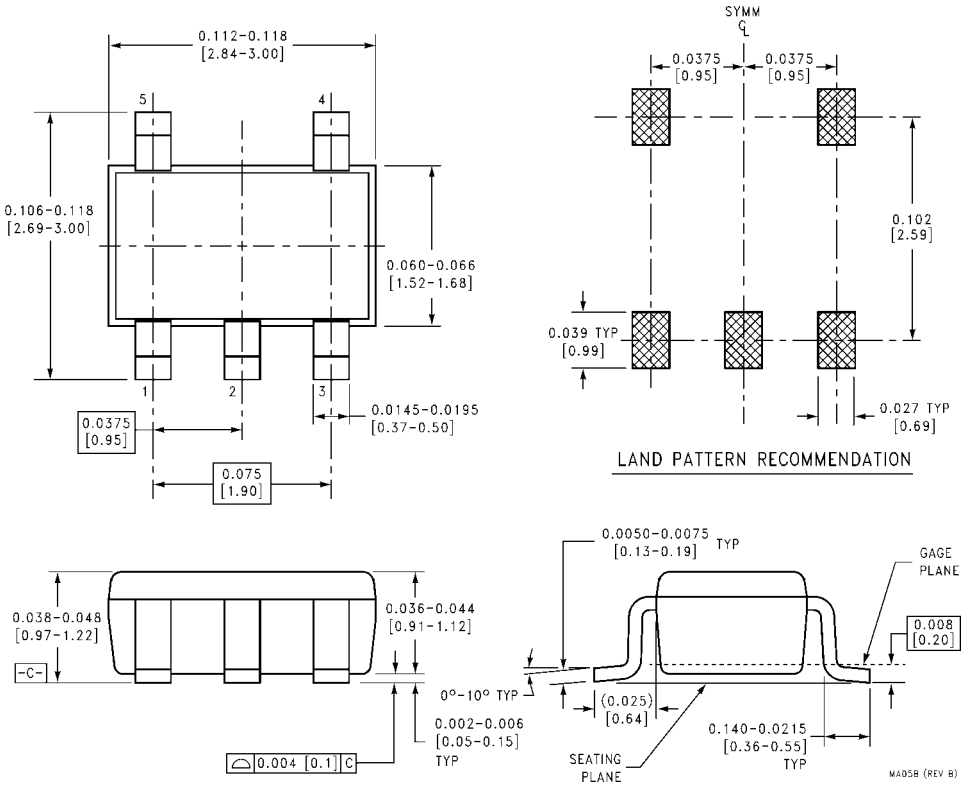
10

Physical Dimensions inches (millimeters) unless otherwise noted



M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



MA05B

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3.0 PROCESS INFORMATION

3.1 Process Flow

Fabrication Site: South Portland Fairchild
Process Technology: CS80CBI(Submicron Silicon Gate CMOS/Bipolar)
Wafer Diameter: 6 inches
Number of Masks: 17
Metallization: 0.5% Copper, dual layer Aluminum metal
1st layer = 7,500 Å thick
2nd layer = 12,000 Å thick

Top Side Passivation: Polyamide (30,000 Å thick)

Over Nitride (11,500 Å thick)
Over Oxide (5,000 Å thick)

3.2 Process Detail & Masks

STAGE 1: Intial Ox
STAGE 2: Trench Define & Etch
STAGE 3: **Mask 0.6**, N-Iso
STAGE 4: N-Iso Implant
STAGE 5: N-Iso Drive
STAGE 6: N-Iso Ox Strip & Screen Ox
STAGE 7: **Mask 0.8**, N+ Buried layer
STAGE 8: N+ Buried Layer Implant
STAGE 9: **Mask 0.9**,P+ Buried Layer
STAGE 10: P+ Buried Layer Implant
STAGE 11: Buried Layer Anneal
STAGE 12: Epi Growth
STAGE 13: Pad Oxide & Nitride
STAGE 14: **Mask 1.0**, N-Well
STAGE 15: N-Well Implant
STAGE 16: Selective Oxide
STAGE 17: N-Well Nitride Strip
STAGE 18: P-Well implant
STAGE 19: Selective Oxide Etch
STAGE 20: N-Well & P-Well Drive-In Oxide
STAGE 21: Drive-In Oxide Strip
STAGE 22: **Mask 2.0**, Composite
STAGE 23: Composite Pad Oxide & Composite Nitride
STAGE 24: Composite Mask Etch
STAGE 25: **Mask 3.0**, P-Field
STAGE 26: P-Field Implant
STAGE 27: Iso Field Oxide
STAGE 28: Active (Composite Area) Nitride Strip
STAGE 29: Pad Oxide Removal & Sacrificial Oxide Growth & Vt Adjust Implant
STAGE 30: Sacrificial Oxide Strip & Gate Oxide & Poly Deposition
STAGE 31: Poly Dope, Poly Anneal
STAGE 32: **Mask 4.0**, Poly
STAGE 33: Poly Etch
STAGE 34: Poly Seal Oxide
STAGE 35: Mask 4.3, P-LDD
STAGE 36: P-LDD Implant

STAGE 37: **Mask 4.5**, N-LDD
STAGE 38: N-LDD Implant
STAGE 39: Spacer Oxide Deposit & Etch
STAGE 40: **Mask 5.0**, N+
STAGE 41: N+ Implnat
STAGE 42: **Mask 5.5**, Base
STAGE 43: Base Etch & Base Implant
STAGE 44: N+ Drive
STAGE 45: **Mask 6.0**, P+
STAGE 46: P+ Implant
STAGE 47: Dielectric Layer1 & P+ Anneal
STAGE 48: SOG
STAGE 49: **Mask 7.0**, Window
STAGE 50: Window Etch & Contact Dielectric
STAGE 51: **Mask 7.1**, Contact
STAGE 52: Contact Etch
STAGE 53: Contact Plug & Etchback
STAGE 54: Metal 1 Deposition
STAGE 55: **Mask 8.0**, Metal 1
STAGE 56: Metal 1 Etch
STAGE 57: Metal 1 Alloy
STAGE 58: Dielectric Layer2
STAGE 59: **Mask 9.0**, Via
STAGE 60: Via Etch
STAGE 61: Via Deposition & Metal 2 Deposit
STAGE 62: **Mask 10.0**, Metal 2
STAGE 63: Metal 2 Etch
STAGE 64: Passivation Oxide/Nitride?Polyamide
STAGE 65: **Mask 13.0**, Passivation
STAGE 66: Passivation Etch

3.3 Masking Sequence

Layer title	**Mask**
0.8	N+ Buried Layer
0.9	P+ Buried Layer
1.0	N-Well
2.0	Composite
3.0	P-Field
3.5	Cap Implant
4.0	Poly
4.3	P-LDD
4.5	N-LDD
5.0	N+
5.5	BASE
6.0	P+
7.0A	Window
7.1	Contact
8.0	Metal 1
9.0	Via
10.0	Metal 2
13.0	Passiavation

4.0 PACKAGING INFORMATION

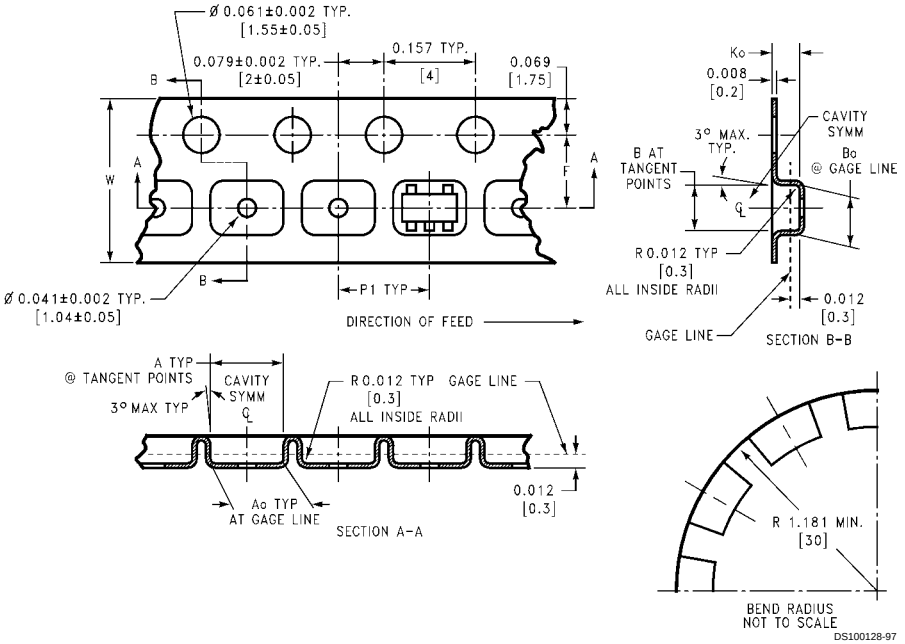
4.1 Package Material

Generic Package Type	5 Lead SOT-23	8 Lead SOIC
NS Package Number	MA05B	MO8A
Package/Compound/ Manufacturer	Epoxy Cresol Novolac Sumitomo	Epoxy Cresol Novolac Sumitomo
Package/Compound Mfg's Designation	Sumitomo EME-6710 NSC B18	Sumitomo EME-1100R NSC B14
Lead Frame Material Manufacturer	Copper NSC-DCI	Copper NSC-DCI
External Lead Frame Coating	Solder Plate Sn/Pb	Solder Plate Sn/Pb
Pins	Gull Wing, 6mils Thick	Gull Wing, 9mils Thick
Die Attached Method	Eutectic, Cr/Ag/Sn	Poly 6
Bond Wire	Gold, 1.0mils	Gold, 0.9mils
Bond Type	Hot Thermosonic Ball	Hot Thermosonic Ball
Package Thermal	265°C/W	190°C/W

4.2 PACKAGE DIMENSIONS

4.2.1 Tape & Reel

Tape Dimensions



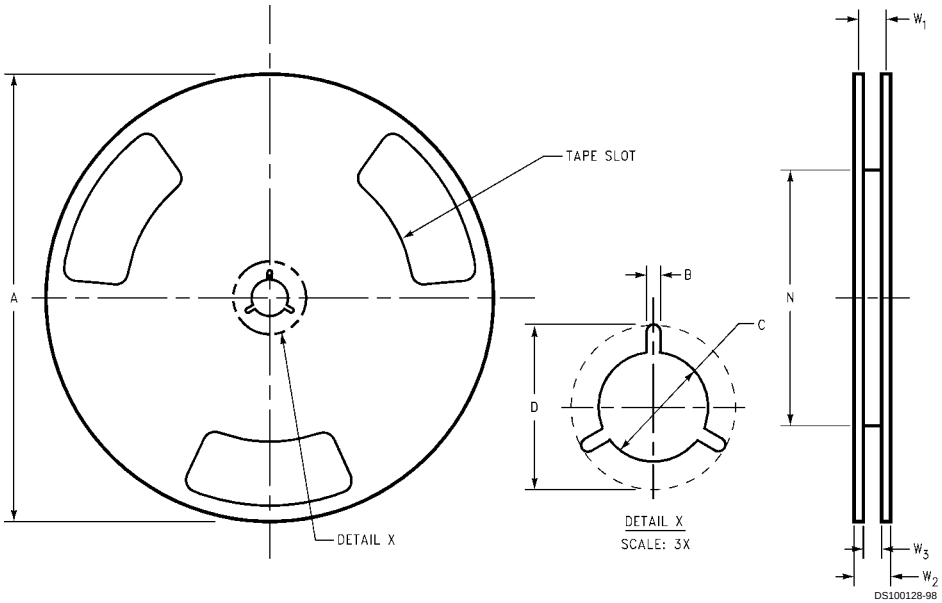
8 mm	0.130 (3.3)	0.124 (3.15)	0.130 (3.3)	0.126 (3.2)	0.138 ±0.002 (3.5 ±0.05)	0.055 ±0.004 (1.4 ±0.11)	0.157 (4)	0.315 ±0.012 (8 ±0.3)
Tape Size	DIM A	DIM Ao	DIM B	DIM Bo	DIM F	DIM Ko	DIM P1	DIM W

SOT-23-5 Tape and Reel Specification

Tape Format

Tape Section	# Cavities	Cavity Status	Cover Tape Status
Leader	0 (min)	Empty	Sealed
(Start End)	75 (min)	Empty	Sealed
Carrier	3000	Filled	Sealed
	250	Filled	Sealed
Trailer	125 (min)	Empty	Sealed
(Hub End)	0 (min)	Empty	Sealed

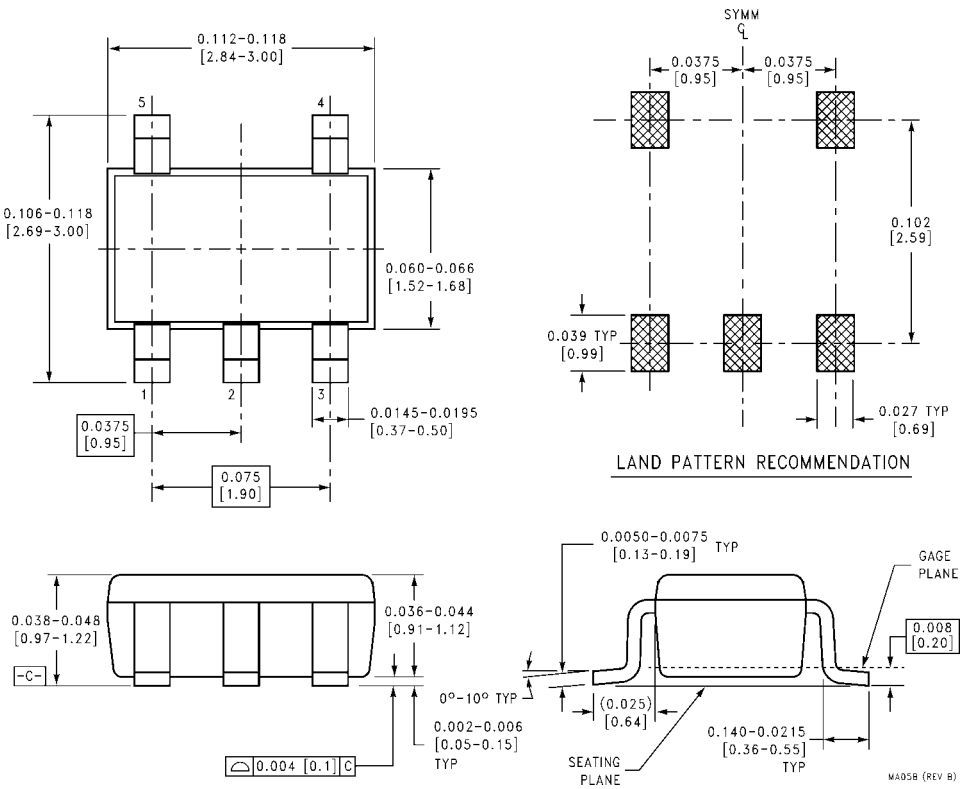
Reel Dimensions



8 mm	7.00 330.00	0.059 1.50	0.512 13.00	0.795 20.20	2.165 55.00	0.331 + 0.059/−0.000 8.40 + 1.50/−0.00	0.567 14.40	W1+ 0.078/−0.039 W1 + 2.00/−1.00
Tape Size	A	B	C	D	N	W1	W2	W3

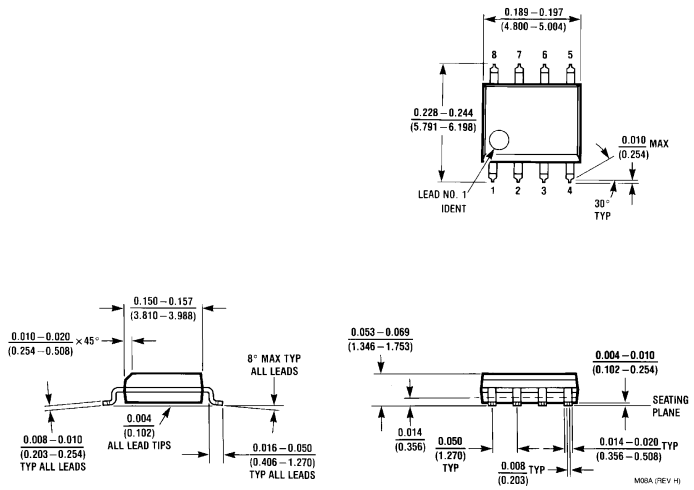
4.2.2 Package Dimensions

Physical Dimensions inches (millimeters) unless otherwise noted



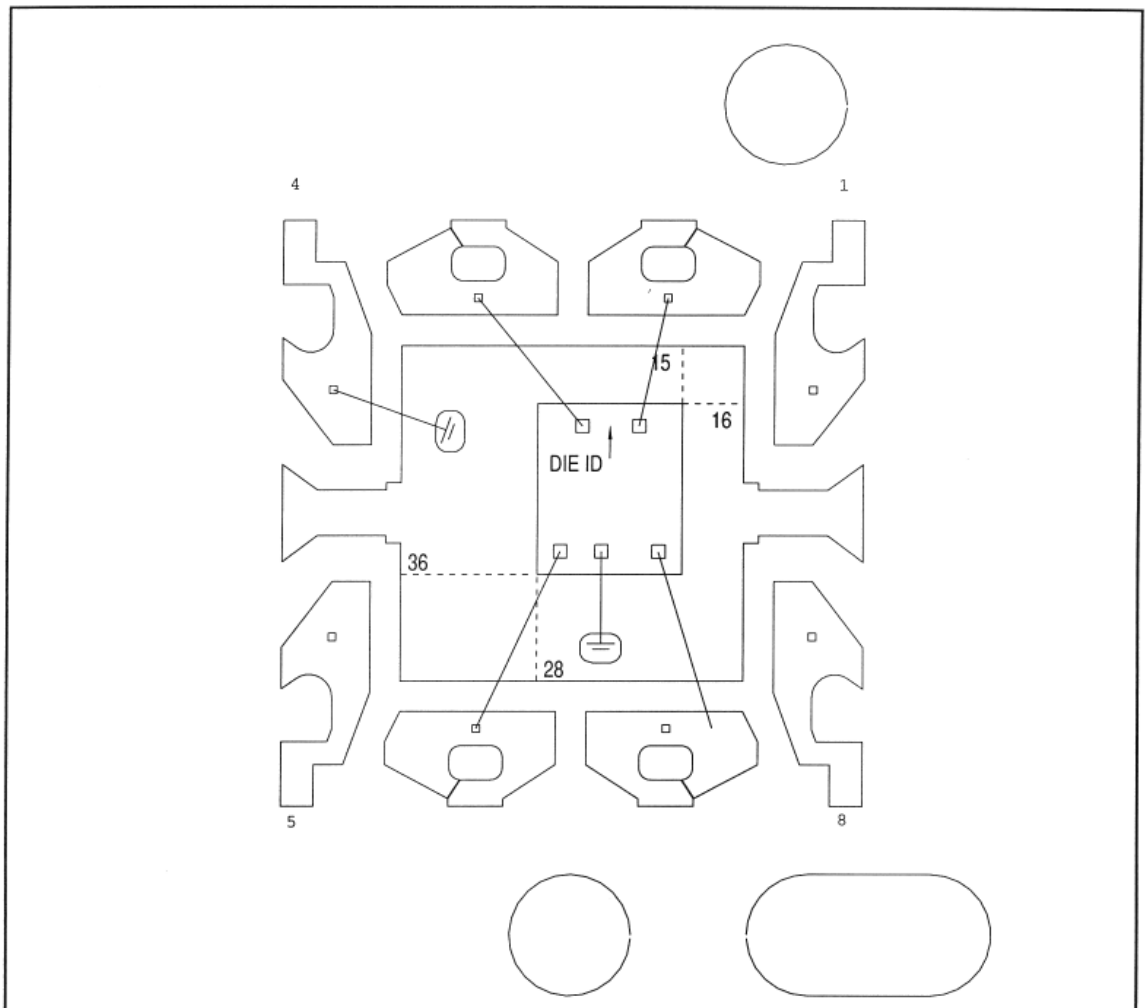
SOT 23-5
Order Number LMC2001
NS Package Number MA05B

Physical Dimensions inches (millimeters) unless otherwise note

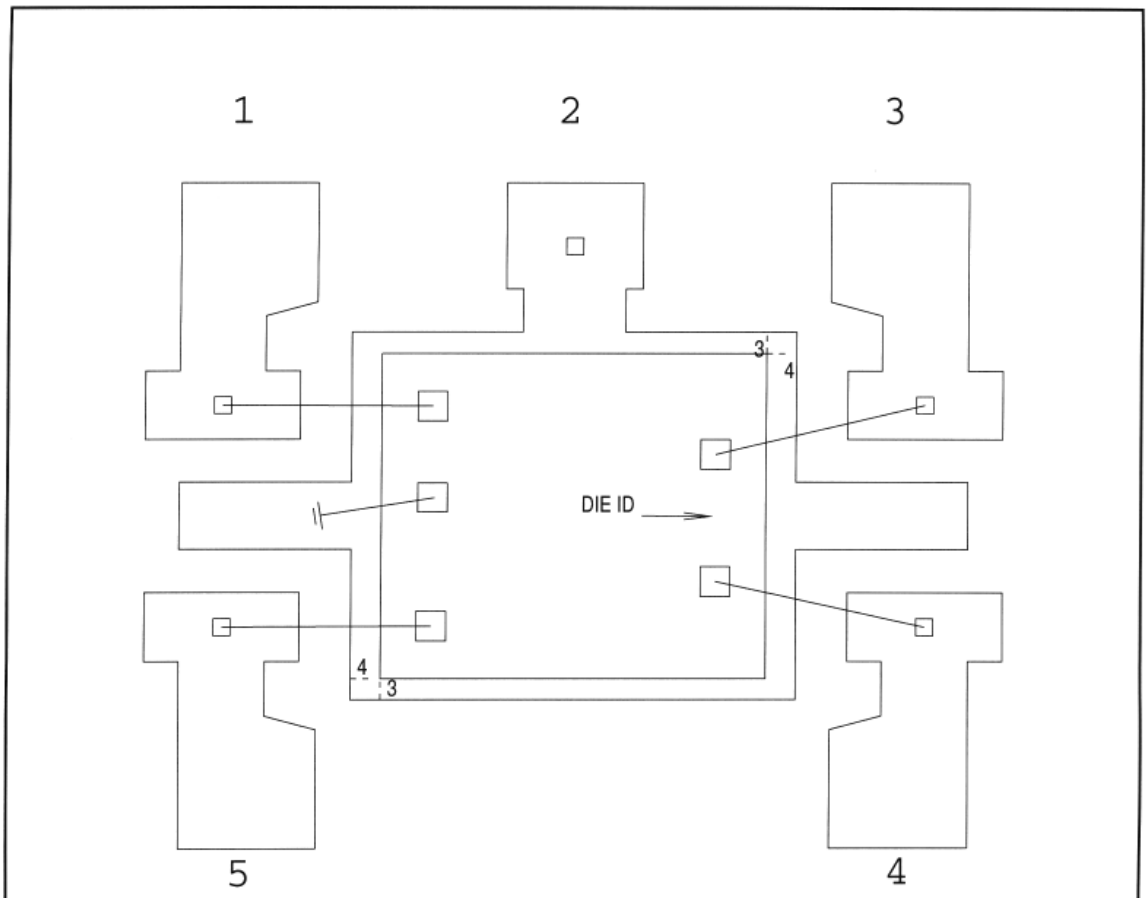


8-Pin Small Outline
Order Number LMC2001
NS Package Number M08A

4.3 Bonding Diagrams



□FRAME DWG: 36-0663-04 SK: 056271 PAD: .088 X .090	AD- MA008ACI MB REV: C PKG: MA DIE ID: LMC2001B STEP/REV: B	Metalization: BOND-CODE: 0.5% CU, DLM	
□DIE ATTACH SK: 010137 TYPE: POLY 6 □WIRE SK: 021566 TYPE: AU DIA = .0009 # WIRES: 6 □MOLD COMPOUND SK: 010426 TYPE: B14	DIE SIZE(* CALCULATED) (MIL): 38 X 45 (MIC): 965 X 1143 * DIE PLACEMENT X= 36 Y= 28 ANGLE= 0.0 □ADHESIVE SK: N/A □HEAT SINK SK: N/A □CHIP CAPS SK: N/A QTY: N/A DWG: N/A	MBS NOTE	1. SO-8, .150 WIDE, MATRIX 2. STAMPED FRAME.
	NOTE: USE D/A TOOL SIZE 30 X 50 GROUND BOND WITHIN CIRCLE	04/13/98 04/13/98	CLCTEM CDKSSC
MIN. PAD PITCH: MILS	ASS'Y : LMC2001M	DASH- 02	REV: A PDCN: BHJ172



□FRAME DWG: 36-0831-01 SK: 061543 PAD: .052 X .043	AD- MA005ACI MB REV: A PKG: MA DIE ID: LMC2001BZ STEP/REV: B	Metalization: BOND-CODE: 0.5% CU, DLM	
□DIE ATTACH SK: N/A TYPE: N/A □WIRE SK: 022628 TYPE: AU DIA = .001 # WIRES: 5 □MOLD COMPOUND SK: 058072 TYPE: B18	DIE SIZE(* CALCULATED) (MIL): 45 X 38 (MIC): 1143 X 965 * DIE PLACEMENT X= 4 Y= 3 ANGLE= 0.0 □ADHESIVE SK: N/A □HEAT SINK SK: N/A □CHIP CAPS SK: N/A QTY: N/A DWG: N/A	MBS NOTE	
	NOTE: PHYSICAL DIE ID: LMC2001B DIE ATTACH TYPE: EUTECTIC	02/04/98 CLLHEM 02/09/98 CDKSSC	
MIN. PAD PITCH: 10.74 MILS	ASS'Y : LMC2001M5 DASH- 03 REV: A PDCN: BGH380		

5.0 RELIABILITY DATA

National Semiconductor

Reliability Test Report

File Number: FSC19980198
Originator: Nick Stanco
Date: May 5, 1998

Purpose

LMC2001 NEW DEVICE QUALIFICATION

Approvals

Reliability Engineer

Mgr Ref Engineering

Reference File Numbers

RSC199800644
RSC199702347
RSC199702260
RSC199700160
Q19960526

Distribution List

Solaiman Harooni
Nick Stanco

Abstract

The LMC2001 is a new low power, low voltage precision op-amp device fabricated on the CS80CBI process in the 6 inch fab line in NSFM. This device was subjected to reliability testing in the 8L MDIP, 5L SOT-23 and 8L SOIC packages for qualification as a new device for the Amplifiers product line. The device has successfully completed all required reliability tests except for the final DOPL lot required for qualification of the final silicon revision which is now in progress. This preliminary report will be updated to included the final DOPL test results once available and to release this device if warranted.

Description

Test Request	Device Name	Sbgp	Wafer Die Run	Fab Loc	Fab Line	Pkg Code	# Leads	Assy Loc	Mold Cmpd
RSC199700160	LMC2001AIN	A	W#10	FM	CS80CBI	N\MDIP	8	SC	B8
RSC199702260	LMC2001ST(005)	A		FM	6 INCH	N\TG23	5	EM	
RSC199702347	LMC2001M(008)	A	B0081794	FM	6 INCH	N\MSON	8	EM	B14
RSC199800644	LMC2001M(008)	B	B00800MC4C	FM	6 INCH	N\MSON	8	EM	B14

Tests Performed

Test: Autoclave Test (ACLV)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199702260	LMC2001ST(005)	A	100%	15 PSIG	121C	
RSC199702347	LMC2001M(008)	A	100%	15 PSIG	121C	

Test: Operating Life Test (Dynamic) (DOPL)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199702347	LMC2001M(008)	A			150C	
RSC199800644	LMC2001M(008)	B			150C	

Test: Operating Life Test (Static) (SOPL)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199700160	LMC2001AIN	A			150C	

Tests Performed (cont)

Test: Temperature Cycle (TMCL)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199702260	LMC2001ST(005)	A			150C	-65C
RSC199702347	LMC2001M(008)	A			150C	-65C

Test: Temperature Humidity Bias Test (THBT)

Test Request	Device	Sbgrp	Rel Humidity	Pressure	High Temp	LowTemp
RSC199702260	LMC2001ST(005)	A	85%		85C	
RSC199702347	LMC2001M(008)	A	85%		85C	

Preconditioning: All DOPL, THBT, TMCL and ACLV parts were preconditioned per RAI-5-039 using the "IB1" flow with a 168 hour 85C, 85% RH moisture soak and 3 passes of IR reflow at 235C.

Results/Discussion

Package	Test	Timepoint	Lot 1 REJ/SS	Lot 2 REJ/SS
8L SOIC	DOPL-IB1	168 HOURS	0/77	0/76
		500 HOURS	0/77	0/76
		1000 HOURS	0/77	0/77
	THBT-IB1	168 HOURS	0/76	
		500 HOURS	0/76	
		1000 HOURS	0/76	
	ACLV-IB1	96 HOURS	0/77	
		168 HOURS	0/77	
	TMCL-IB1	500 CYCLES	0/77	
		1000 CYCLES	0/77	
5L SOT-23	THBT-IB1	168 HOURS	0/76	
		500 HOURS	0/76	
		1000 HOURS	0/76	
	ACLV-IB1	96 HOURS	0/77	
		168 HOURS	0/77	
	TMCL-IB1	500 CYCLES	0/77	
		1000 CYCLES	0/77	
8L MDIP	SOPL	168 HOURS	0/77	
		500 HOURS	0/77	
		1000 HOURS	0/77	

LATCH-UP: PASSED +/- 200 MA AT BOTH 25C AND 85C PER JEDEC 17 STANDARDS

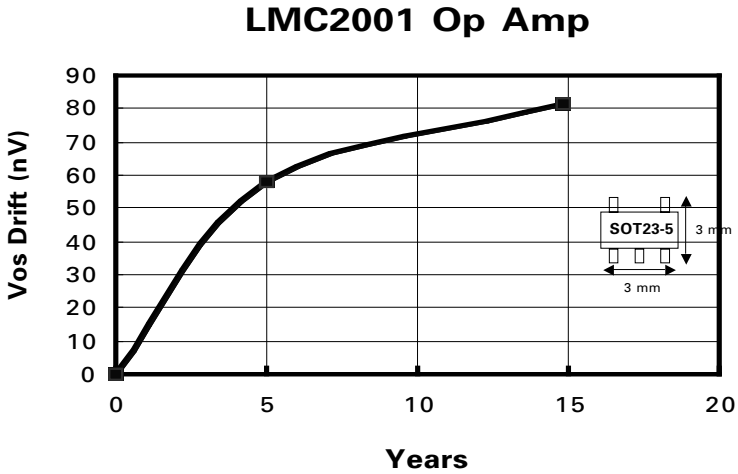
ESD Testing	Human Body Model	REJ/SS	Machine Model	REJ/SS
	500V	0/5	100V	0/5
	1000V	0/5	125V	0/5
	1500V	0/5	150V	0/5
	2000V	0/5	175V	2/5
	2500V	0/5	200V	5/5
	3000V	5/5	250V	5/5
	3500V	5/5		

Conclusion

This is a preliminary report covering all reliability testing to date on the LMC2001. The device has not yet been approved for release by Corporate Reliability.

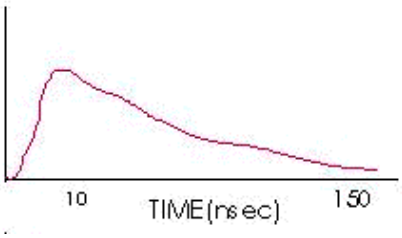
Operational Life Hour Conversion to Years

Enter Accl. Temperature (C)	150
Enter Operating Temperature (C)	55
Enter Activation Energy (ev)	0.7
The estimated Acc. Factor is	258.2380605
Test Time Points of OPL(hrs)	Est. Life time of the device (yrs)
24	0.709445221
48	1.418890442
72	2.128335663
96	2.837780884
120	3.547226105
168	4.966116547
500	14.78010877
1000	29.56021754

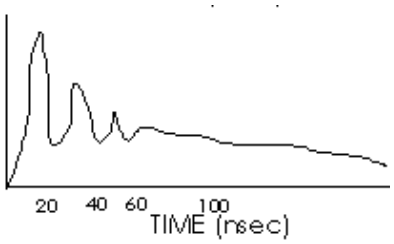


5.2 ESD/LATCH-UP

Human Body Model (HBM)
• R = 1500 ohms and C = 100pF
• rise time = 10ns



Machine Model (MM)
• R = 0 ohms and C = 200pF
• rise time = <8ns

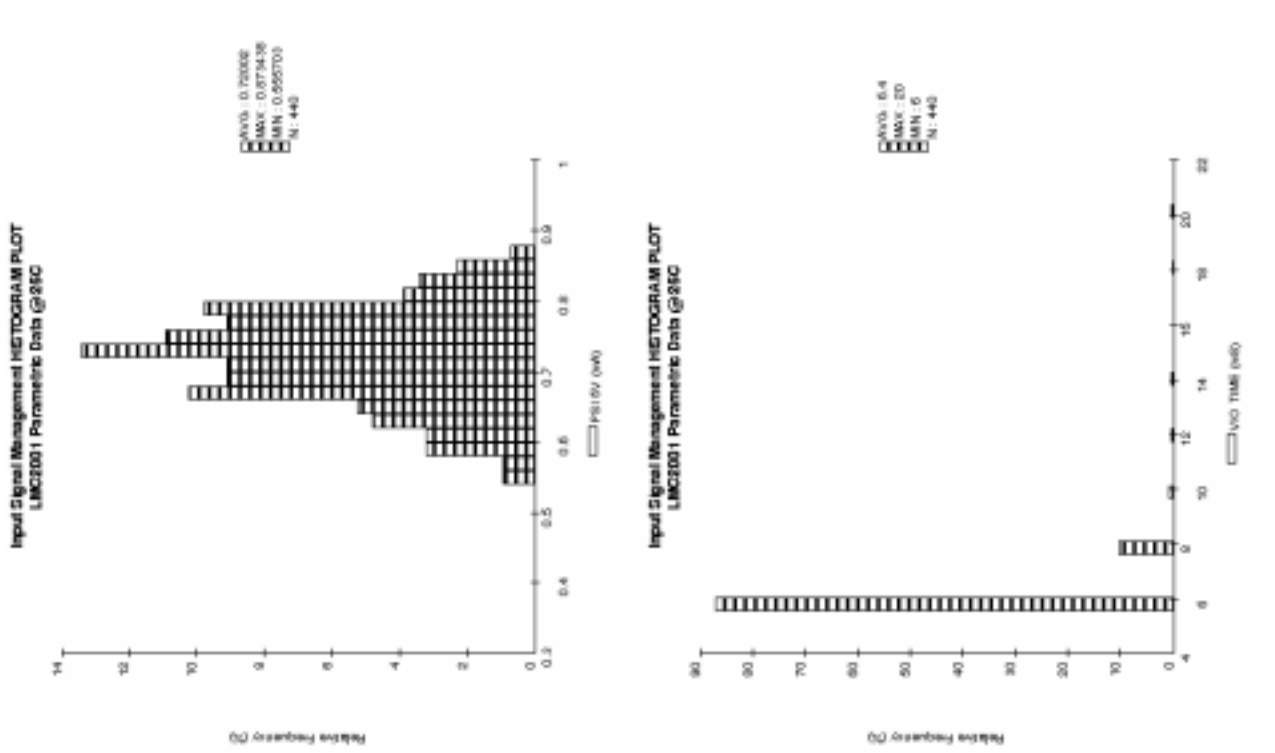


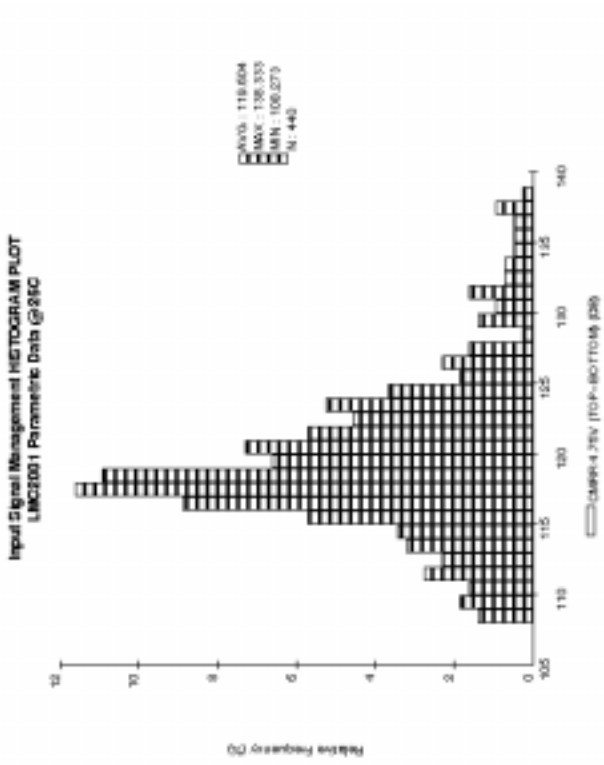
6.0 CHARACTERIZATION DATA

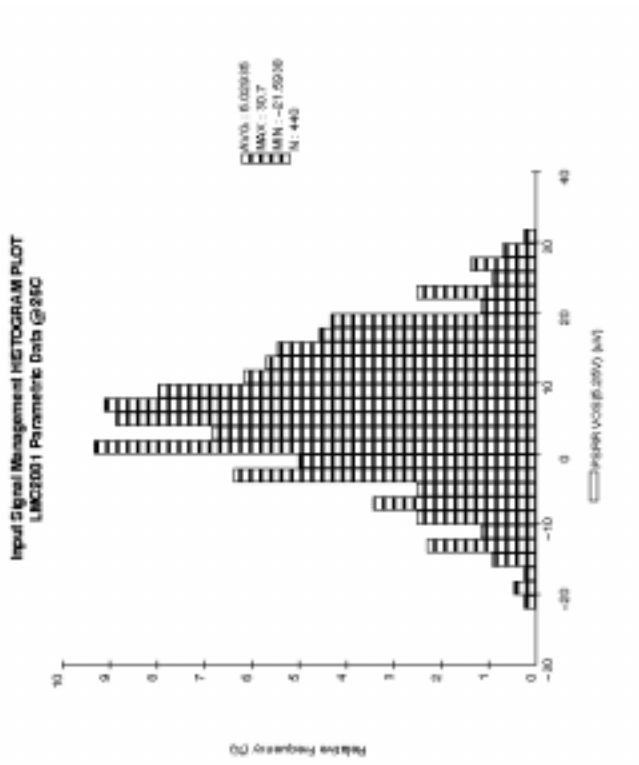
6.1 Test Summary

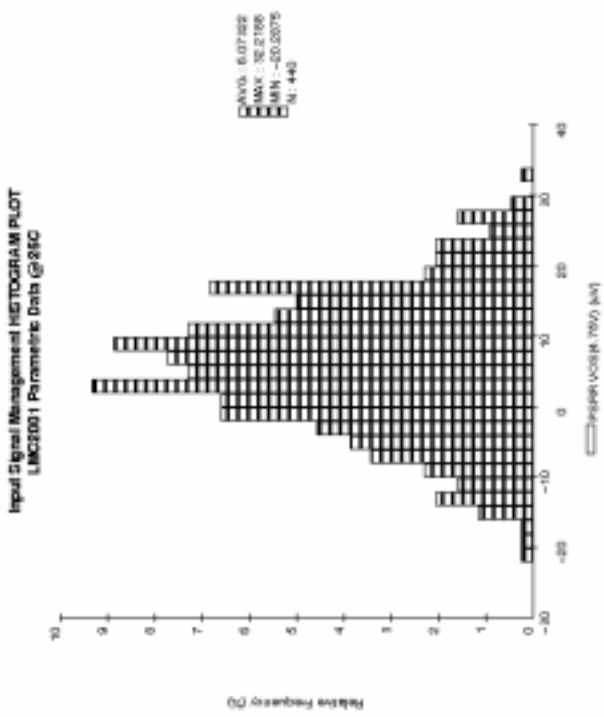
Test#	Test Name	Temp (C)	Supply Voltage	Obs.	Avg.	Min.	Max.	Units
1	PSI	25	± 2.50V	440	0.720	0.556	0.873	mA
3	Autozero Delay	25	± 2.50V	440	6.400	6.000	20.000	mS
4	VOS	25	± 2.50V	440	4.875	-21.30	27.794	µV
210	CMRR 5.25V	25	± 2.50V	440	120.878	105.328	148.328	db
216	CMRR 4.75V	25	± 2.50V	440	119.604	108.273	139.333	db
229	VOS @ PSRR(5.25V)	25	± 2.50V	440	6.029	-21.594	30.7	µV
230	VOS @ PSRR(4.75V)	25	± 2.50V	440	6.073	-20.288	32.219	µV
237	Gain RL 2k source	25	± 2.50V	440	132.547	117.719	167.795	db
240	Gain RL 2k sink	25	± 2.50V	440	130.966	116.873	149.379	db
243	Gain RL 10k source	25	± 2.50V	440	133.282	119.825	158.253	db
246	Gain RL 10k sink	25	± 2.50V	440	132.642	118.052	158.253	db
247	Swing RL 2k source	25	± 2.50V	440	2.436	2.415	2.440	V
248	Swing RL 2k sink	25	± 2.50V	440	-2.424	-2.435	-2.405	V
250	Swing RL 10k source	25	± 2.50V	440	2.471	2.463	2.473	V
249	Swing RL 10k sink	25	± 2.50V	440	-2.470	-2.478	-2.463	V
251	Iout source	25	± 2.50V	440	6.096	5.16	7.005	mA
252	Iout sink	25	± 2.50V	440	20.260	8.565	31.41	mA

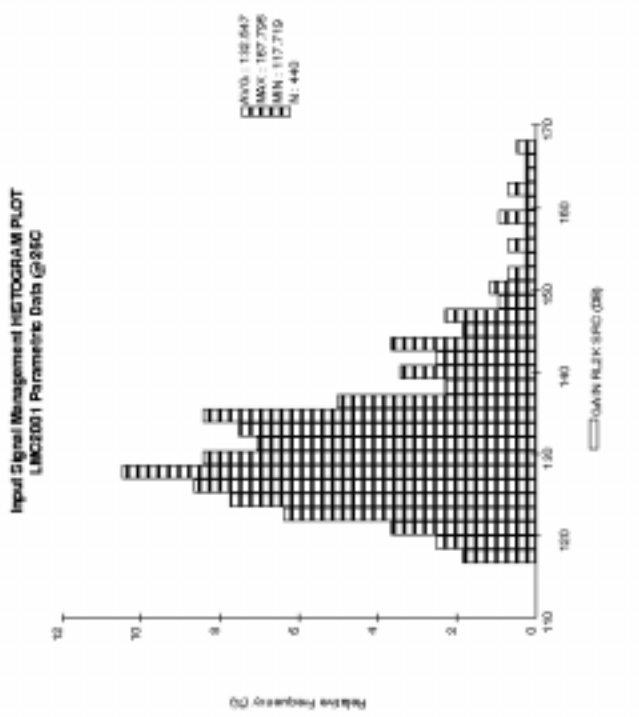
6.2 Test Graphs

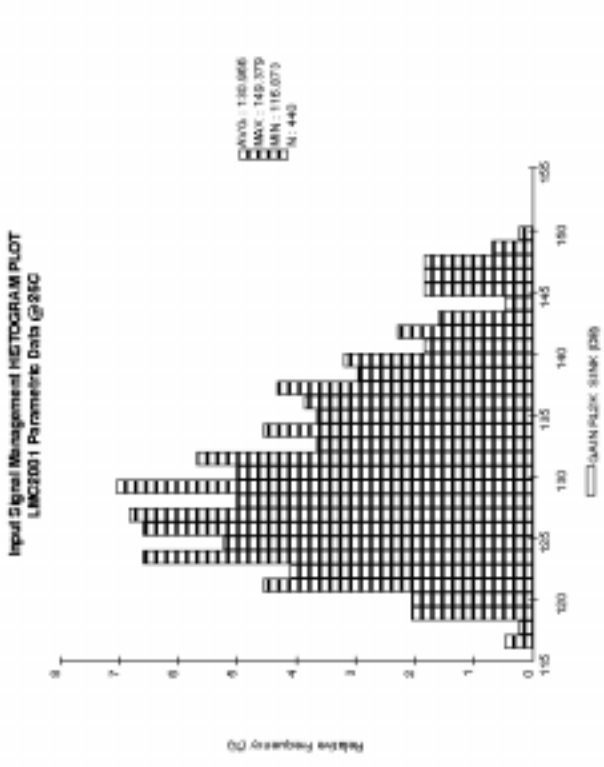


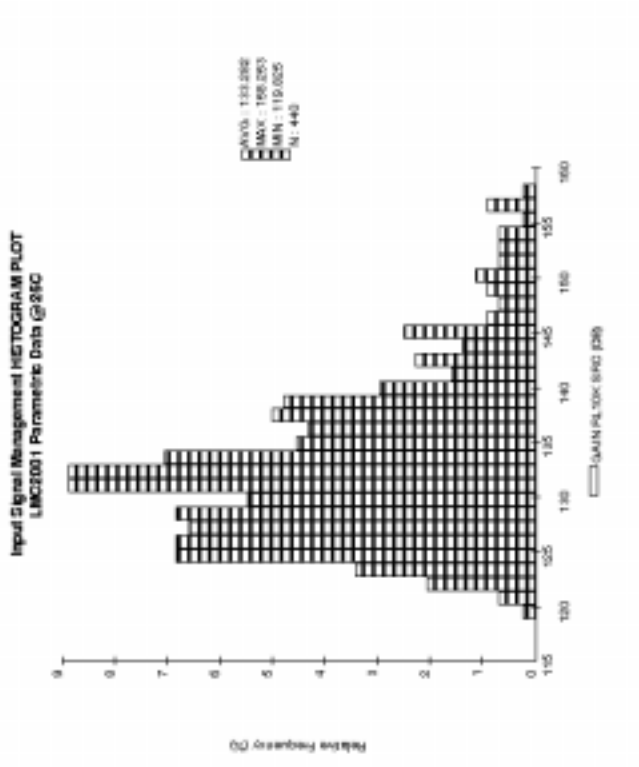

Input Signal Management HISTOGRAM PLOT
LMC2001 Parametric Data @25C
AVG : 119.604
MAX : 138.333
MIN : 106.273
N : 440
Relative Frequency (%)

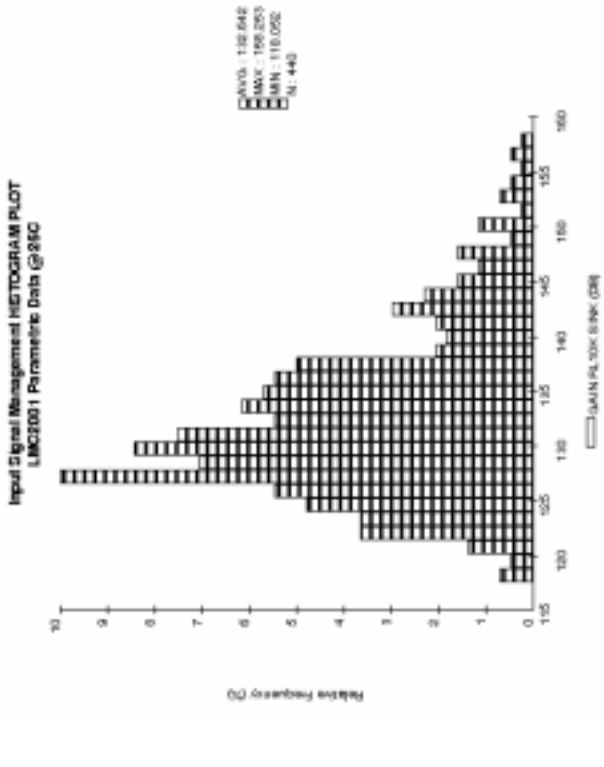

Input Signal Management HISTOGRAM PLOT
LMC2001 Parametric Data @25C
AVG : 6.029545
MAX : 30.7
MIN : -21.5938
N : 440
Relative Frequency (%)

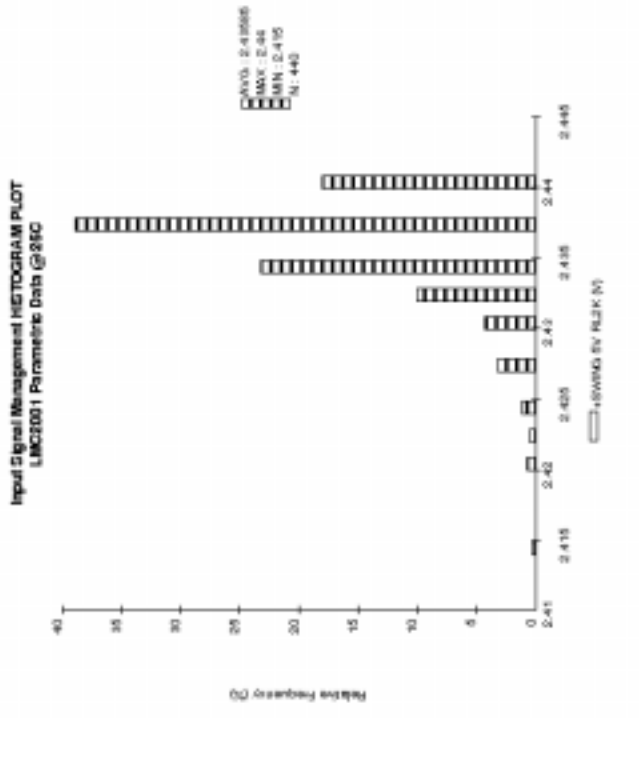

Input Signal Management HISTOGRAM PLOT
LMC2001 Parametric Data @25C
AVG : 6.071932
MAX : 32.21768
MIN : -20.0375
N : 440
Relative Frequency (%)

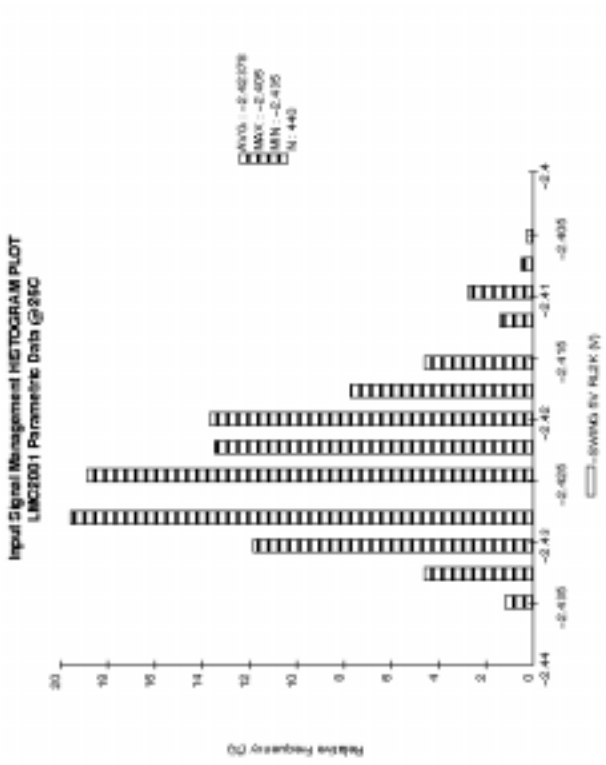

Input Signal Management HISTOGRAM PLOT
LMC2001 Parametric Data @25C
AVG : 132.647
MAX : 167.795
MIN : 117.719
N : 440
Relative Frequency (%)

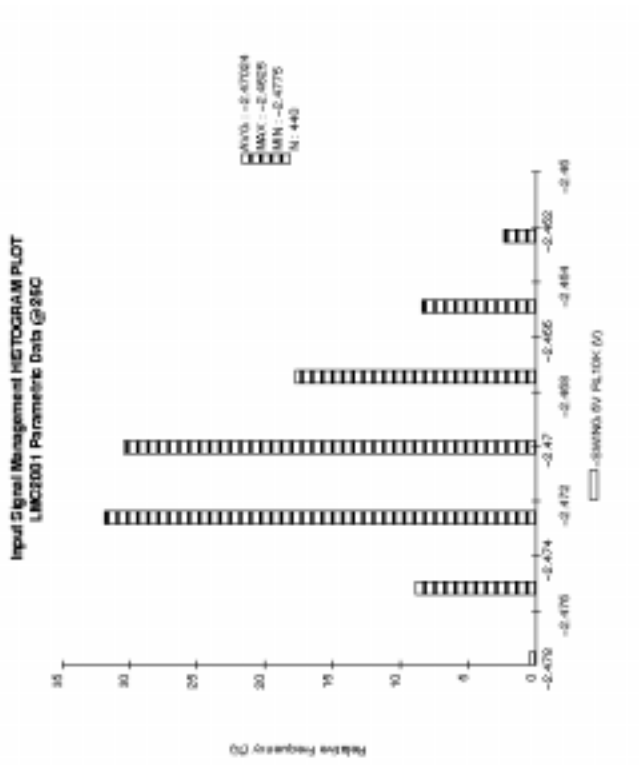

Input Signal Management HISTOGRAM PLOT
LMC2001 Parametric Data @25C
AVG : 130.686
MAX : 149.379
MIN : 116.073
N : 440
GAIN RL10K SINK (DB)
Relative Frequency (%)

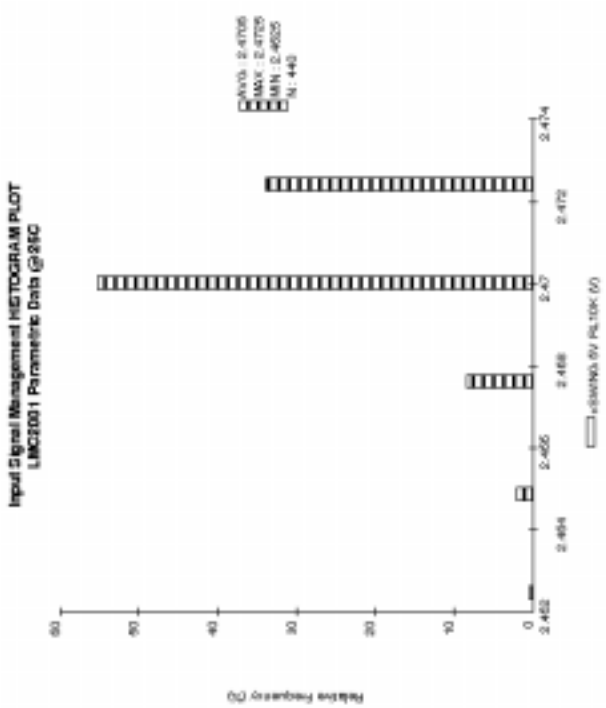

Input Signal Management HISTOGRAM PLOT
LMC2001 Parametric Data @25C
AVG : 133.282
MAX : 156.253
MIN : 119.025
N : 440
GAIN RL10K SRC (DB)
Relative Frequency (%)

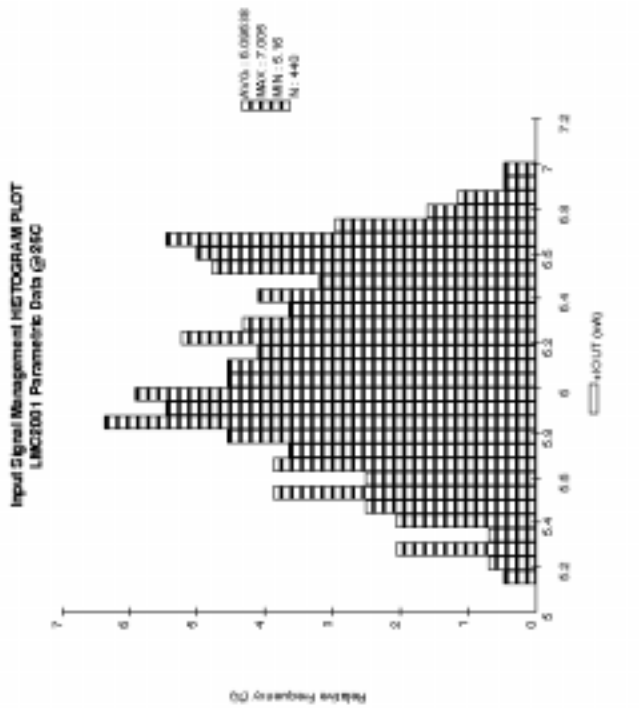

Input Signal Management HISTOGRAM PLOT
LMC2001 Parametric Data @25C
AVG : 132.648
MAX : 156.253
MIN : 116.052
N : 440
GAIN RL10K SINK (DB)
Relative Frequency (%)

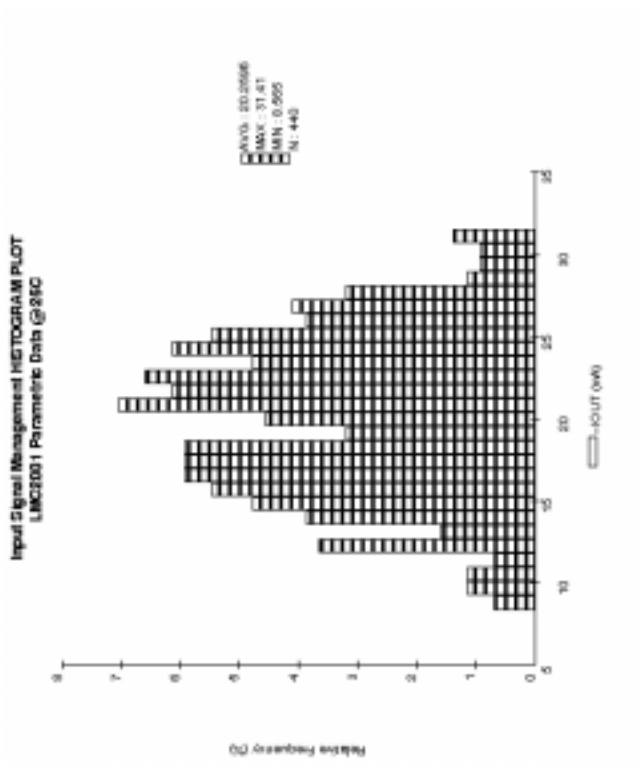

Input Signal Management HISTOGRAM PLOT
LMC2001 Parametric Data @25C
AVG : 2.419565
MAX : 2.44
MIN : 2.415
N : 440
VSWING 5V RL2K (V)
Relative Frequency (%)


Input Signal Management HISTOGRAM PLOT
LMC2001 Parametric Data @25C
AVG : -2.42378
MAX : -2.405
MIN : -2.435
N : 440
-SWING 5V RL2K (V)
Relative Frequency (%)

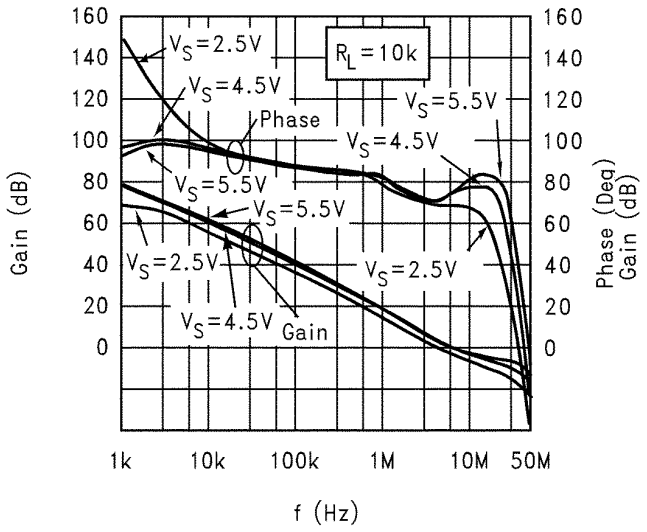

Input Signal Management HISTOGRAM PLOT
LMC2001 Parametric Data @25C
AVG : -2.47024
MAX : -2.4625
MIN : -2.4775
N : 440
-SWING 5V RL10K (V)
Relative Frequency (%)


Input Signal Management HISTOGRAM PLOT
LMC2001 Parametric Data @25C
AVG : 2.47035
MAX : 2.4725
MIN : 2.4625
N : 440
+SWING 5V RL10K (V)
Relative Frequency (%)

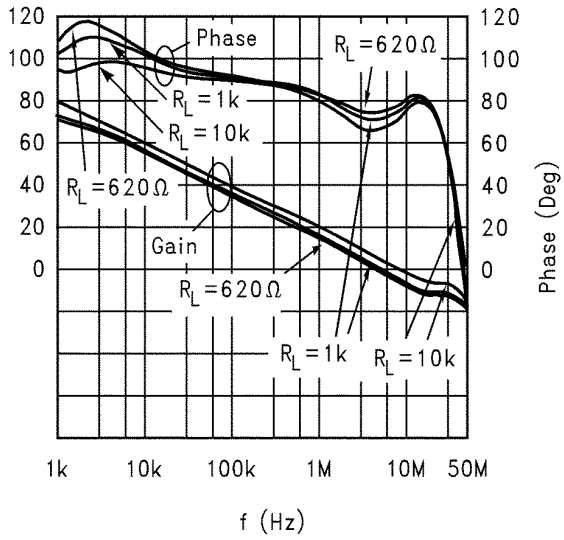

Input Signal Management HISTOGRAM PLOT
LMC2001 Parametric Data @25C
AVG : 6.036538
MAX : 7.005
MIN : 5.95
N : 440
+VOUT (mV)
Relative Frequency (%)


Input Signal Management HISTOGRAM PLOT
LMC6001 Parametric Data @25C
Mean : 20.0566
MAX : 31.41
MIN : 8.995
N : 440
Relative Frequency (%)
0
1
2
3
4
5
6
7
8
10
15
20
25
30
35
-IOUT (mA)

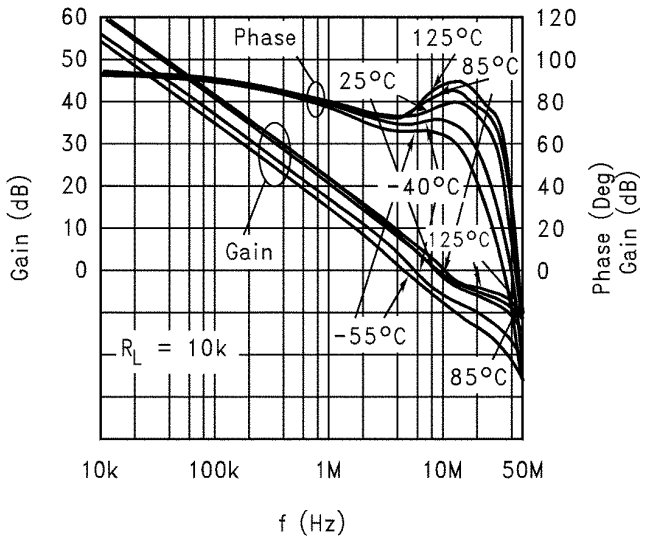
Gain-Phase vs V_s



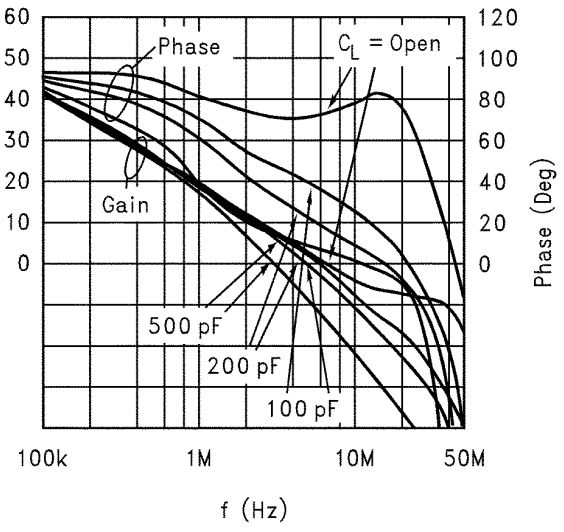
Gain-Phase vs R_L



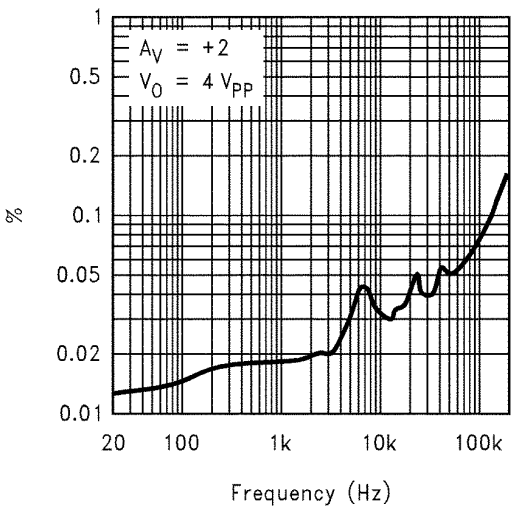
Gain-Phase vs Temp



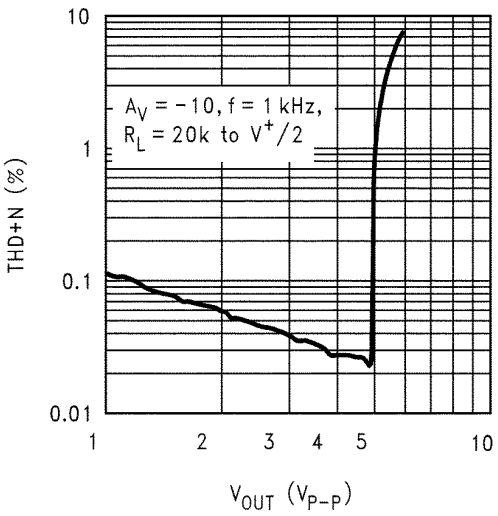
Gain-Phase vs C_{Load}



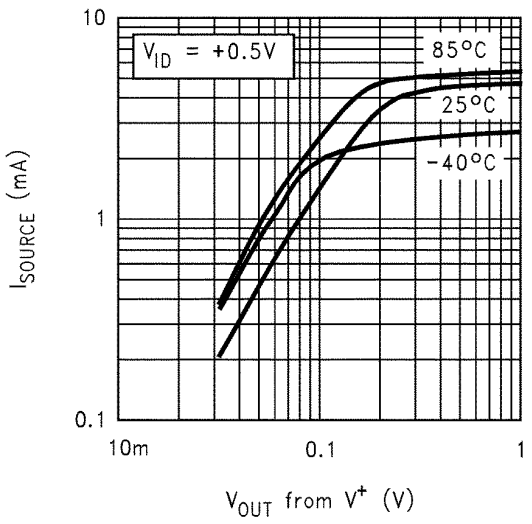
THD+N vs Frequency



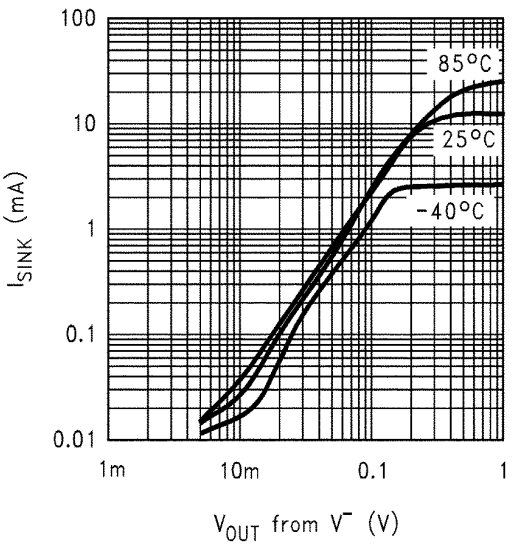
THD+N vs V_{OUT}

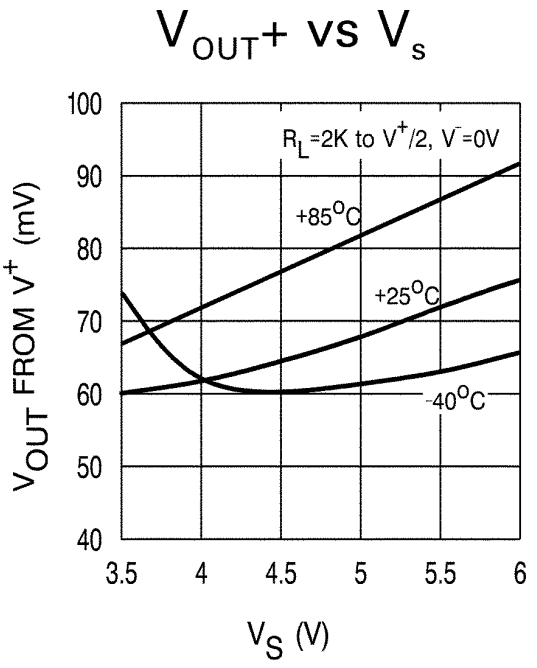


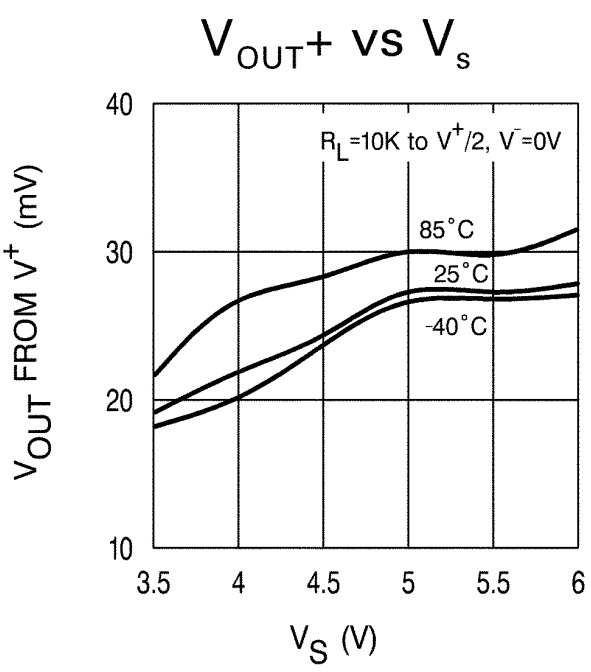
I_{SOURCE} vs V_{OUT}

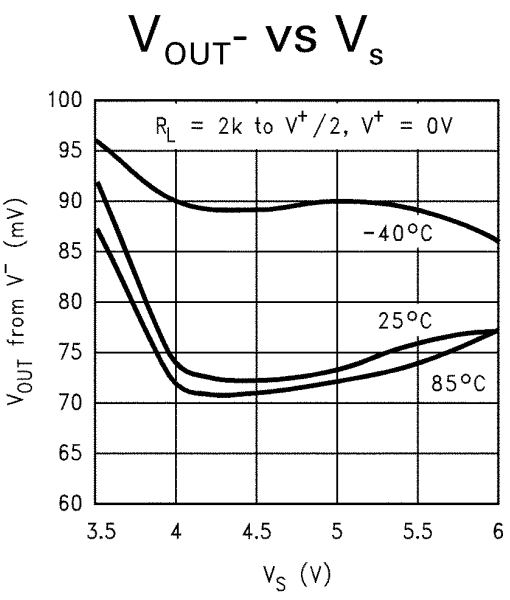


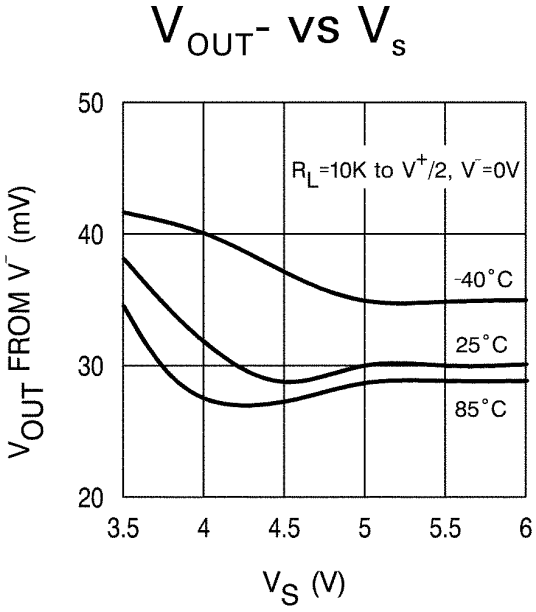
I_{SINK} vs V_{OUT}



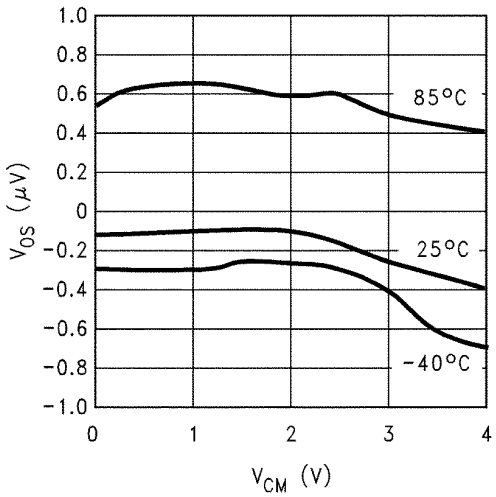

V_{OUT}+ vs V_s
R_L=2K to V^+/2, V^-=0V
+85°C
+25°C
-40°C
V_{OUT} FROM V^+ (mV)
V_S (V)
100
90
80
70
60
50
40
3.5
4
4.5
5
5.5
6


V_{OUT}+ vs V_s
R_L=10K to V^+/2, V^-=0V
85°C
25°C
-40°C
V_{OUT} FROM V^+ (mV)
V_S (V)
40
30
20
10
3.5
4
4.5
5
5.5
6

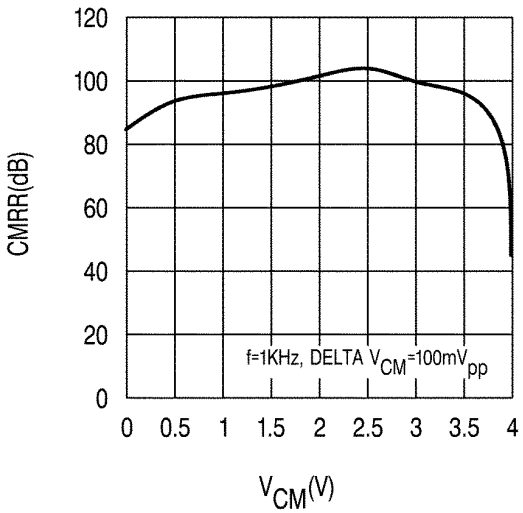

V_{OUT}- vs V_s
R_L = 2k to V^+/2, V^+ = 0V
-40°C
25°C
85°C
V_{OUT} from V^- (mV)
V_S (V)
100
95
90
85
80
75
70
65
60
3.5
4
4.5
5
5.5
6


V_{OUT}- vs V_s
R_L=10K to V^+/2, V^-=0V
-40°C
25°C
85°C
V_{OUT} FROM V^- (mV)
V_S (V)
50
40
30
20
3.5
4
4.5
5
5.5
6

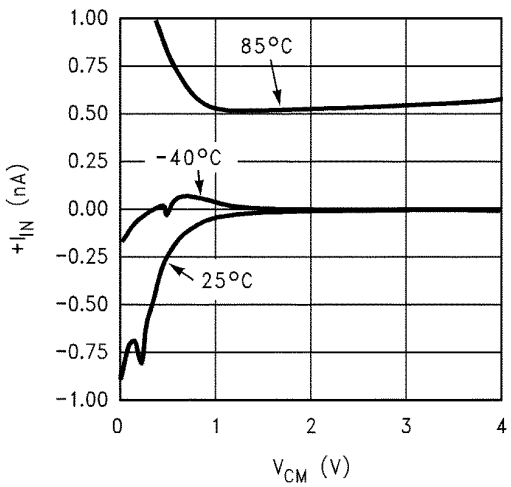
V_{OS} vs V_{CM}



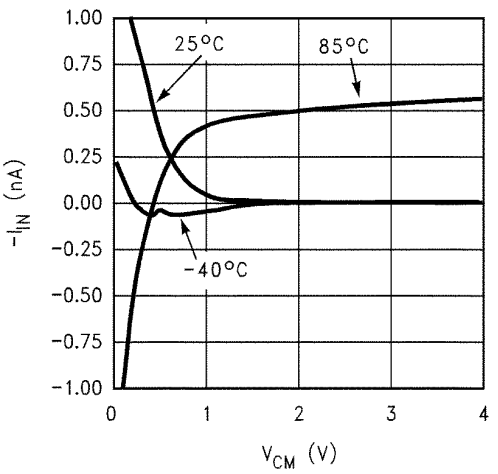
CMR vs V_{CM}



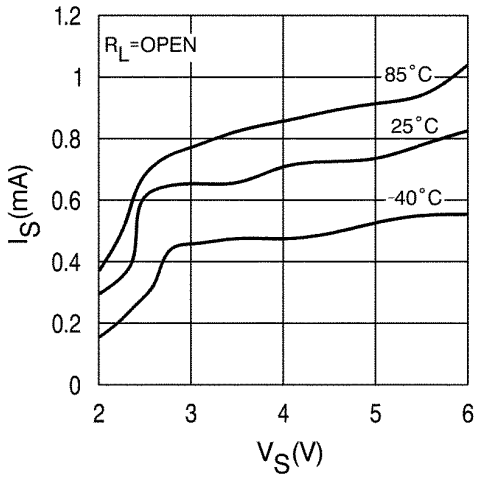
$+I_{IN}$ vs V_{CM}



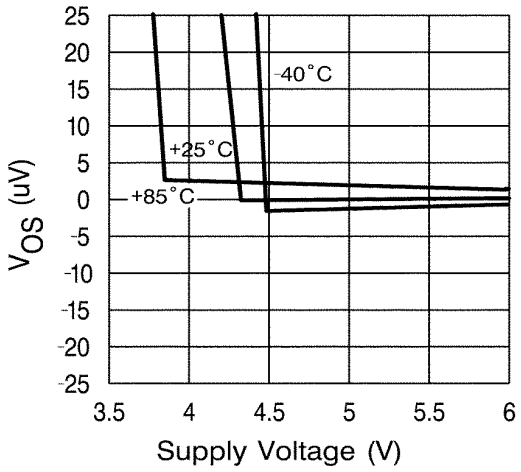
$-I_{IN}$ vs V_{CM}



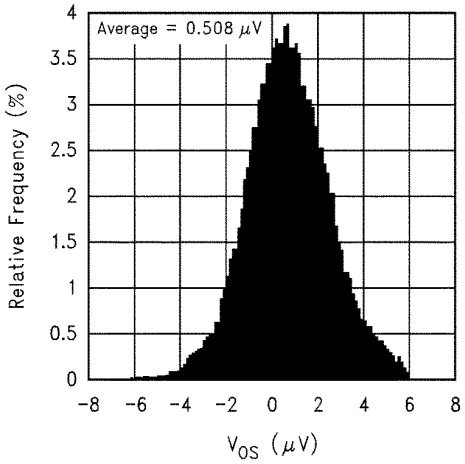
Isupply vs V_S



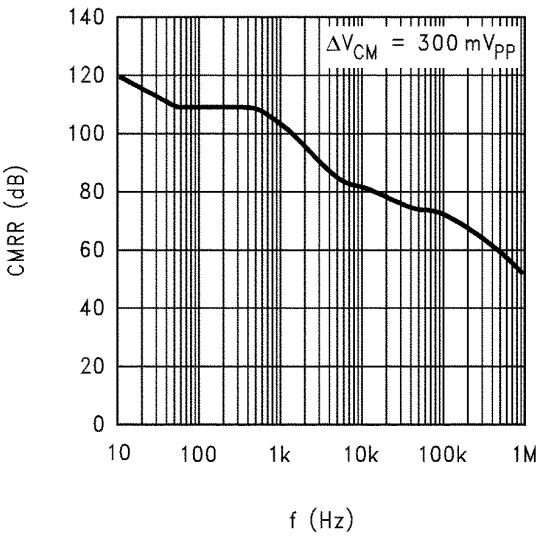
V_{OS} vs V_S



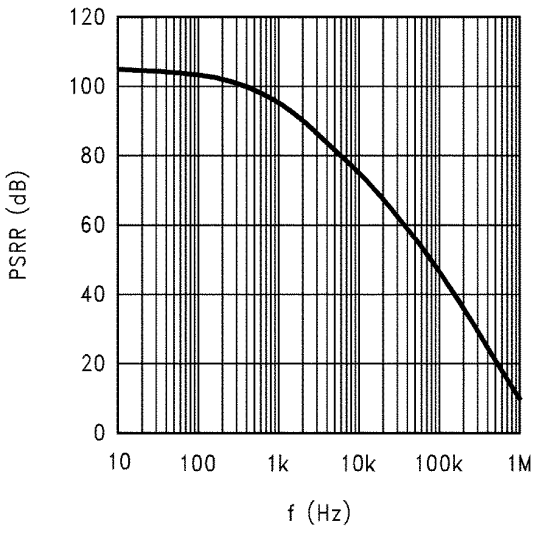
V_{OS} Distribution



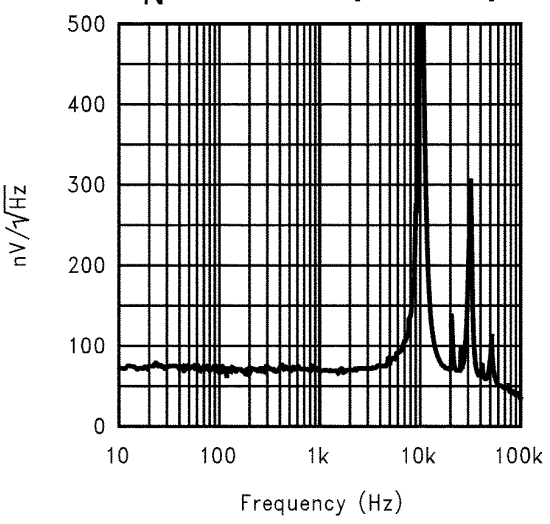
CMR vs Frequency



PSR vs Frequency



e_N vs Frequency



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