Nordic VLSI ASA

# Single chip 915 MHz Transmitter **nRF904**

## FEATURES

- True single chip FSK transmitter in a small 8-pin package
- Adjustable output power up to +1dBm
- FSK data rate up to 50kbits/s
- Controllable modulation deviation
- Very few external components
- Improved frequency stability compared to SAW solutions
- Wide power supply range: 2.4 to 3.6 V
- Low supply current, typical 9mA @ -10dBm output power
- Power Down and Clock modes makes power saving easy
- Reference Clock output pin for microcontroller

## APPLICATIONS

- Automatic Meter Reading
- Keyless entry
- Wireless data communication
- Alarm and security systems
- Home Automation
- Remote control
- Surveillance
- Automotive
- Telemetry
- Toys

## GENERAL DESCRIPTION

nRF904 is a single-chip transmitter for the 902-928 MHz band. It is compliant with the US Federal Communications Commission (FCC) standard CFR47 chapter 15. The transmitter consists of a fully integrated frequency synthesiser, a power amplifier, a crystal oscillator and a modulator. Due to the use of the crystal-oscillator stabilised frequency synthesiser, frequency drift is much lower than in comparable SAW-resonator based solutions. Output power and frequency deviation is easily programmable by use of external resistors. Current consumption is very low, only 9 mA at an output power of –10dBm. Built-in Clock and Power Down modes makes power saving easily realisable.

## QUICK REFERENCE DATA

| Parameter | Value | Unit |
|---|---|---|
| Supply voltage | 2.4 – 3.6 | V |
| Maximum output power @ 400Ω, 3 V | 1 | dBm |
| Maximum FSK data rate | 50 | kbit/s |
| Supply current FSK transmitter @ -10dBm output power | 9 | mA |
| Supply current in Clock mode | 200 | µA |
| Supply current in Power Down mode | <10 | nA |

Table 1. nRF904 quick reference data.

| Type Number | Description | Version |
|---|---|---|
| nRF904 - IC | 8 pin SOIC | |
| nRF904 - EVKIT | Evaluation kit with nRF904 IC on board | |

Table 2. nRF904 ordering information.

# BLOCK DIAGRAM

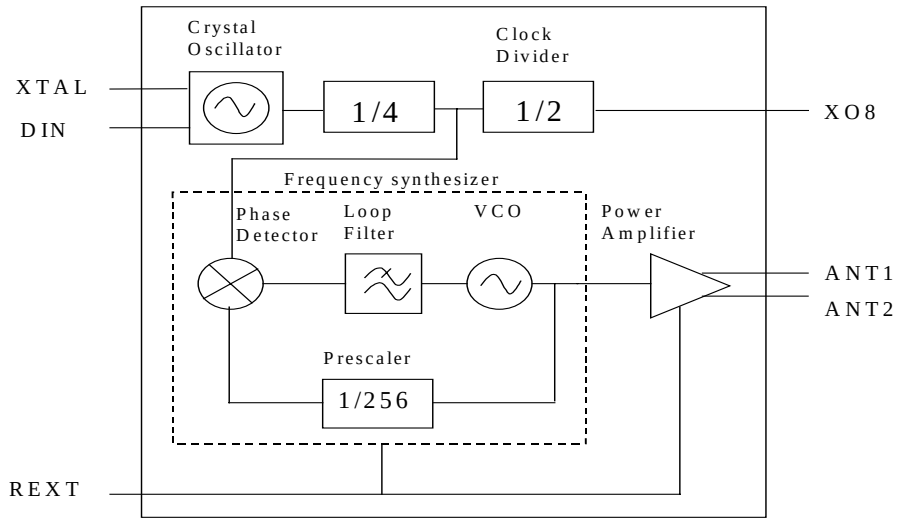



Figure 1. nRF904 block diagram.

# PIN FUNCTIONS

| Pin | Name | Pin function | Description |
|---|---|---|---|
| 1 | XTAL | Input | Crystal pin / Power Up |
| 2 | REXT | Input | Power adjust / Clock Mode / ASK modulation digital input |
| 3 | XO8 | Output | Reference Clock Output (Crystal Frequency / 8) |
| 4 | VDD | Power | Power Supply (+ 3 V DC) |
| 5 | DIN | Input | Digital Data Input |
| 6 | ANT2 | Output | Antenna terminal |
| 7 | ANT1 | Output | Antenna terminal |
| 8 | VSS | Power | Ground (0V) |

Table 3. nRF904 pin functions.

# PIN ASSIGNMENT

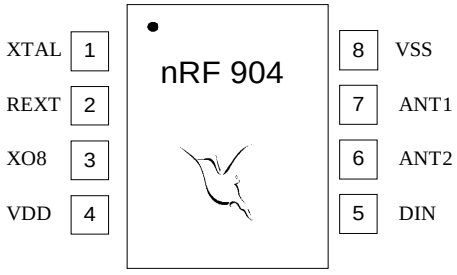



Figure 2. nRF904 pin assignment.

# ELECTRICAL SPECIFICATIONS

Conditions: VDD = +3V, VSS = 0V, $T_A$ = - 40ºC to + 85ºC

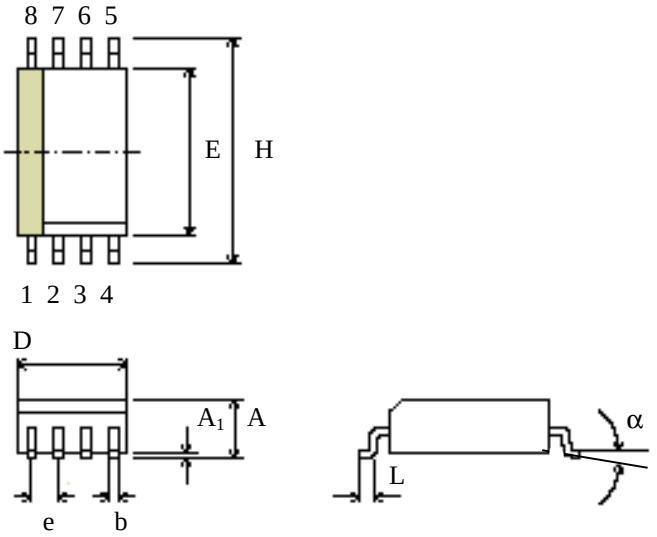
| Symbol | Parameter (condition) | Notes | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | **Operating conditions** | | | | | |
| $f_{TX}$ | Transmit frequency | 1) | 902 | | 928 | MHz |
| $f_{XTAL}$ | Crystal frequency | 1) | 14.094 | | 14.500 | MHz |
| $V_{DD}$ | Supply voltage | | 2.4 | | 3.6 | V |
| Tamb | Operating temperature range | | - 40 | | + 85 | °C |
| $P_{RF}$ | Maximum Output Power | 3) | | | 1 | dBm |
| $I_{DD}$ | Supply current CLOCK Mode | 2) | | 175 | 300 | µA |
| $I_{DD}$ | Supply current POWER DOWN Mode | | | 10 | 100 | nA |
| | **FSK modulation** | | | | | |
| Δf | Frequency deviation (peak) | 6) | 10 | 20 | 40 | kHz |
| $R_{FSK}$ | FSK data rate | | 0 | | 50 | kbit/s |
| $I_{DD}$ | Supply current @ 1dBm output power | 3) | | 18 | 27 | mA |
| $I_{DD}$ | Supply current @ -10dBm output power | 3) | | 9 | 17 | mA |
| | **ASK modulation** | | | | | |
| $R_{ASK}$ | ASK data rate | | 0 | | 10 | kbit/s |
| $P_{RF1}$ | Transmitted power at data = '1' | | | | 1 | dBm |
| $P_{RF0}$ | Transmitted power at data = '0' | | | | -50 | dBm |
| $I_{DD}$ | Supply current @ 1dBm output power | 3) | | 18 | 27 | mA |
| $I_{DD}$ | Supply current @ -50dBm output power | 3) | | 175 | 300 | uA |
| | **DIN input pin** | | | | | |
| $V_{IH}$ | HIGH level input voltage | 4) | $V_{DD}$ - 0.5 | | $V_{DD}$ | V |
| $V_{IL}$ | LOW level input voltage | 4) | Vss | | 0.3 | V |
| | **XO8 output pin** | | | | | |
| $V_{OH}$ | HIGH level output voltage | 5) | | $V_{DD}$ | $V_{DD}$ | V |
| $V_{OL}$ | LOW level output voltage | 5) | | $V_{DD}$ -1.0 | | V |

NOTES:
1) The crystal frequency may be altered to produce any desired frequency within the 902MHz to 928MHz band.
2) Measured with no load on XO8 output pin.
3) Antenna load impedance = 400 Ω.
4) The levels stated are supplied to a external series resistor in front of the DIN input pin
5) Output is an open collector.
6) Controllable with crystal parameters and external data filter.

Table 4. nRF904 electrical specifications.

# PACKAGE OUTLINE

nRF904, uses the SOIC 8 package. Dimensions are in mm.




| Package Type | | D | E | H | A | $A_1$ | e | b | L | Copl. | α |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SOIC 8 | **Min** | 4.80 | 3.81 | 5.84 | 1.55 | 0.127 | 1.27 | 0.35 | 0.41 | | 0° |
| | **Max** | 4.98 | 3.99 | 6.20 | 1.73 | 0.250 | | 0.49 | 0.89 | 0.25 | 8° |

Figure 3. nRF904 package outline.

## Absolute Maximum Ratings

**Supply voltages**

VDD..... - 0.3V to + 6V

VSS.....0V

**Input voltage**

$V_I$..... - 0.3V to VDD + 0.3V

**Output voltage**

$V_O$..... - 0.3V to VDD + 0.3V

**Total Power Dissipation**

$P_D$ ($T_A$=85°C).....220mW

**Temperatures**

Operating Temperature…. - 40°C to + 85°C

Storage Temperature….. - 40°C to + 125°C

*Note: Stress exceeding one or more of the limiting values may cause permanent damage to the device.*

**ATTENTION!**

Electrostatic Sensitive Device

Observe Precaution for handling.

# MODES OF OPERATION

### Overview of Operational Modes

Table 5 provides an overview of the different modes that the nRF904 may be set to. $V_{R1}$ to $V_{R4}$ are the control nodes for resistors 1 to 4 (R1 to R4 see Figure 4) and represent the voltage state needed to set a particular mode.

| Mode | $V_{R1}$ | $V_{R2}$ | $V_{R3}$ | $V_{R4}$ |
|---|---|---|---|---|
| Power Down | GND | - | - | - |
| Clock | VDD | GND | VDD | - |
| ASK | VDD | ASK DATA | VDD or GND | VDD |
| FSK | VDD | VDD | VDD or GND | FSK DATA |

Table 5 Overview of Operational Modes for nRF904.

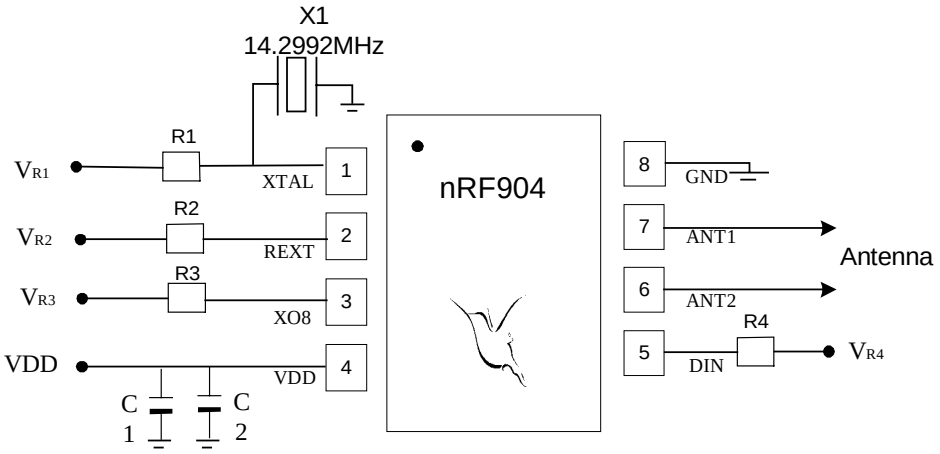



Figure 4. nRF904 with External Components.

### FSK Mode

FSK modulation is realised by feeding the modulating data to the digital DIN input pin (see Figure 4). This is the normal operating mode for nRF904.

In applications where high data rate and low spectrum bandwidth is required; a low pass filter should replace R4 as in Figure 5 to shape the input FSK bit stream. Figure 5 shows both a 1st order (a), and a 2nd order (b) low pass filter.

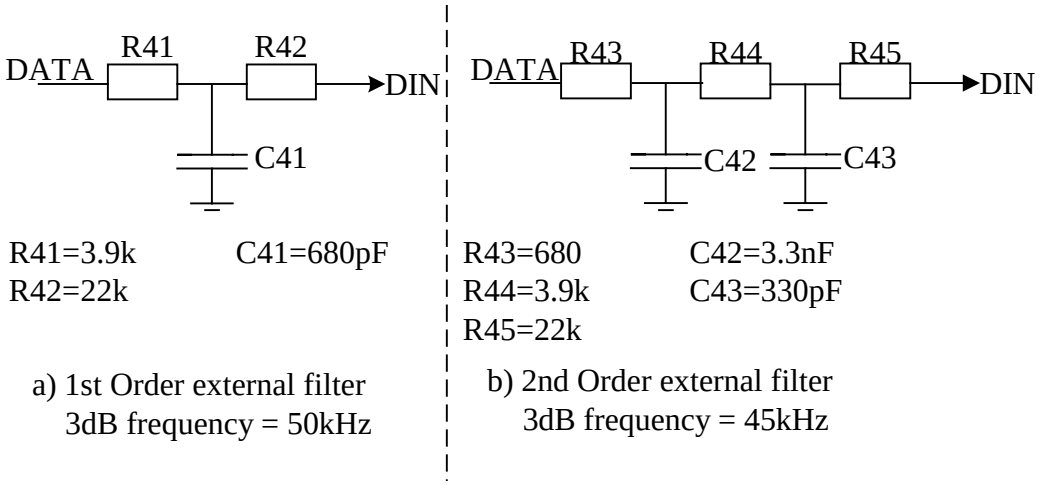



Figure 5. Alternative external DIN components for setting the spectral bandwidth.

**ASK modulation.**
ASK modulation can be realised by using the REXT pin (see Figure 4). When R2 is connected to VDD, the chip transmits a carrier. When R2 is connected to GND then the internal output power amplifier is turned off. These two situations represent logic '1' and logic '0' in an ASK system. When ASK modulation is used, the DIN pin must be connected to VDD.

**Clock mode**
Clock mode is available so that an external microprocessor may have a reference signal without the cost of a second crystal. In Clock mode, the crystal oscillator and reference clock output, XO8, are operating, while the rest of the transmitter is disabled.

Connecting the power-adjusting resistor R2 to ground sets clock mode. Current consumption in Clock mode is typically 175µA when no load is applied at the XO8 clock output pin. If a capacitive load is applied at the XO8 output, then current consumption in Clock mode will increase. Start-up time when switching between Clock mode and Transmit mode is extremely fast, less than 50µs.

The frequency of the clock signal is 1/8th of the crystal frequency i.e. a crystal frequency of 14.2992 MHz will result in an output clock frequency of 1.7874 MHz. The XO8 output is an open collector with an internal 30 kΩ resistor.

The internal XO8 series resistor has a typical value of 30 kΩ. For a given value of the external resistor R3 the output voltage $V_{XO8}$ (peak-to-peak) may be calculated as:

$$V_{XO8} = V_{DD} \cdot \left( \frac{R3}{R3 + 30k\Omega} \right) \qquad \text{[Vpp]}$$

The suggested value of R3 is 15 kΩ. Using the above equation this should provide a typical output voltage of 1.0Vpp. Note that if a significant capacitive load (more than a few picofarads) is present at the XO8 pin this will lead to a voltage loss due to lowpass filtering. Using a capacitive load of 10 pF the typical output voltage swing will drop from 1.0Vpp to 0.8Vpp.

The XO8 signal will be present in Transmit mode and Clock mode if R3 is connected to VDD. If the XO8 pin is not used, it should be connected directly to ground on the circuit board.

If a micro-controller is being used any internal pull up resistor within the micro-controller should also be factored into the above equation.

**Power Down mode**

Power Down mode is used to achieve very low current consumption. Effectively the chip is disabled with minimal leakage current consumption, typically less than 10nA. Operating in this mode when not transmitting data significantly increases battery lifetime.

The resistor R1 connected from the crystal pin towards VDD supplies the crystal oscillator with bias current (see Figure 4). When R1 is connected to ground, the chip enters Power Down mode. A typical value for R1 is 150 kΩ.

# IMPORTANT TIMING DATA

### Timing information

The timing information for the different operations is summarised in Table 6.
(TX is Transmit mode, Clk is Clock mode, Pwr_Dn is Power Down Mode.)

| Change of Mode | Max Delay |
|---|---|
| Pwr_Dn ➔ TX | 5ms |
| Clk ➔ TX | 50µs |

Table 6. Switching times for nRF904.

### Switching between Power Down Mode and Transmit-mode.

The minimum time from Power Down mode until the synthesised frequency is stable and data can be transmitted is seen in Figure 6. XTAL is controlled by $V_{R1}$, Figure 4.

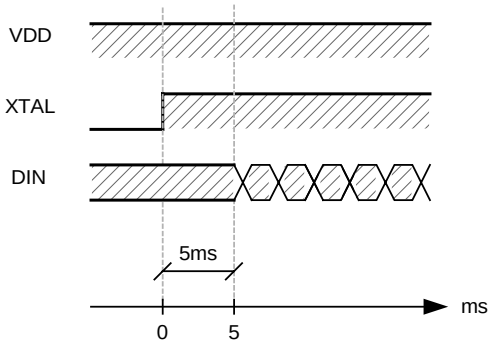



Figure 6. Timing diagram when going from Power Down mode to Transmit-mode.

### Switching between Clock Mode and Transmit-mode.

The minimum time from Clock mode until the synthesised frequency is stable and data can be transmitted is seen in Figure 7. REXT is controlled by $V_{R2}$, Figure 4.

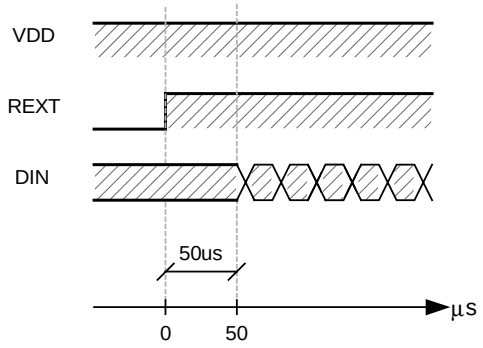



Figure 7. Timing diagram when going from Clock mode to Transmit-mode.

# PERIPHERAL RF INFORMATION

### Antenna output

The "ANT" output pins provide a balanced RF output to the antenna. The pins must have a DC path to VDD, either via a RF choke or via the centre point in a loop antenna. The load impedance seen between the ANT1/ANT2 outputs should be in the range 200-700 Ω. A load impedance of 400 Ω is recommended if maximum output power (10dBm) is needed. Lower load impedance (for instance 50 Ω) can be obtained by fitting a simple matching network or a RF transformer (balun). The 50 Ω load can also be connected directly between the ANT1/ANT2 pins, but this will result in higher current consumption for a given output power to the antenna.

A single ended antenna or 50Ω test instrument may be connected to nRF904 by using a differential to single ended matching network (BALUN) as shown in Figure 8.

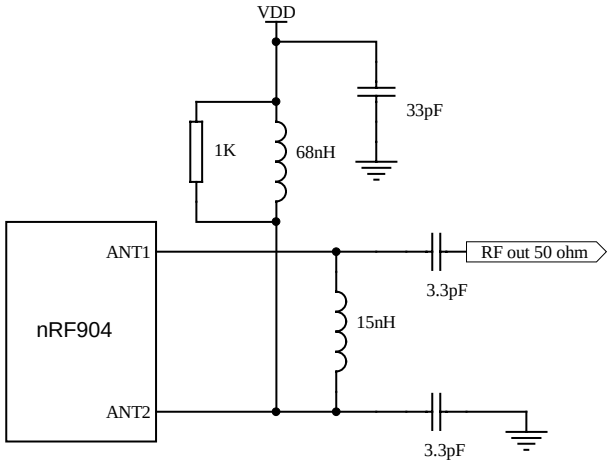



Figure 8. Connection of nRF904 to single ended antenna (50 Ω) by using a differential to single ended matching network.

The inductors in Figure 8 need to have a Self-Resonance Frequency (SRF) above the carrier frequency (902-928MHz). Suitable 68nH inductors are listed in Table 7.

| **Vendors** | **WWW address** | **Part. no., 68 nH inductors, 0603 size** |
|---|---|---|
| Pulse | http://www.pulseeng.com | PE-0603CD680JTT |
| Coilcraft | http://www.coilcraft.com | 0603CS-68NXJBC |
| muRata | http://www.murata.com | LQW1608A68NJ00 |
| Stetco | http://www.stetco.com | 0603G680JTE |
| KOA | http://www.koaspeer.com | KQ0603TE68NJ |

Table 7. Vendors and part no. for suitable 68nH inductors.

Suitable 15nH inductors are listed in Table 8.

| Vendors | WWW address | Part. no., 15 nH inductors, 0603 size |
|---|---|---|
| Pulse | http://www.pulseeng.com | PE-0603CD150GTT |
| Coilcraft | http://www.coilcraft.com | 0603CS-15NXGBC |
| muRata | http://www.murata.com | LQW1608A15NG00 |
| Stetco | http://www.stetco.com | 0603G150GTE |
| KOA | http://www.koaspeer.com | KQ0603TE15NG |

Table 8. Vendors and part no. for suitable 15nH inductors.

**Crystal Specification**

Modulation is achieved by pulling of the crystal capacitance. As such to achieve correct frequency deviation operation as specified in Table 4 the crystal must meet the following specification:

Parallel resonant frequency: fp = transmitter centre frequency divided by 64
Load capacitance: CL = 10 pF
Series resistance, ESR: Rs < 60 ohm
Crystal parallel capacitance: Co < 7 pF
Motional capacitance: Cs = 9 fF (Guideline specification)

**Frequency deviation setting**

The frequency modulation is achieved by pulling the crystal load by the use of an internal varactor. As the external resistor R4 is varied, the varactor voltage swing will vary linearly. R4 is equal to the sum of resistor values if an input filter is used as shown in Figure 5. Changing the value of R4 enables easy variation of the frequency deviation, see Figure 9.

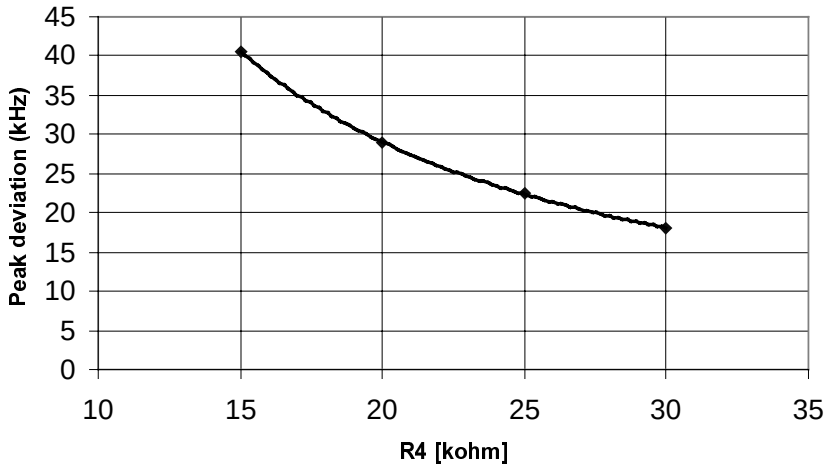



Figure 9. Typical RF Frequency Deviation for varing values of R4.

### Output Power adjustment

A bias resistor R2 (see Figure 4) should be connected from the REXT pin to the positive power supply VDD. The value of this resistor sets the output power level. See table 9 for choice of R2 value.

| Power setting resistor R2 | RF output power | DC current consumption |
|---|---|---|
| 47kΩ | 1dBm | 18mA |
| 120kΩ | -10dBm | 9mA |

Conditions: VDD = 3.0V, VSS = 0V, $T_A$ = 27ºC, Load impedance = 400 Ω.

Table 9. RF output power setting for the nRF904.

### PCB layout and decoupling guidelines

A well-designed PCB is necessary to achieve good RF performance. A PCB with a minimum of two layers including a ground plane is recommended for optimum performance.

The nRF904 DC supply voltage should be decoupled as close as possible to the VDD pins with high performance RF capacitors, see Table 10. It is preferable to mount a large surface mount capacitor (e.g. 4.7 µF tantalum) in parallel with the smaller value capacitors. The nRF904 supply voltage should be filtered and routed separately from the supply voltages of any digital circuitry.

Long power supply lines on the PCB should be avoided. All device grounds, VDD connections and VDD bypass capacitors must be connected as close as possible to the nRF904 IC. For a PCB with a topside RF ground plane, the VSS pins should be connected directly to the ground plane. For a PCB with a bottom ground plane, the best technique is to have via holes in or close to the VSS pads.

Full swing digital data or control signals should not be routed close to the crystal and the XTAL pin.

### PCB layout example

Figure 11 shows a PCB layout example for the application schematic in Figure 10. A double-sided FR-4 board of 1.6mm thickness is used. This PCB has a continuous ground plane on the bottom layer. Additionally, there are ground areas on the component side of the board to ensure sufficient grounding of critical components. A large number of via holes connect the top layer ground areas to the bottom layer ground plane. There is no ground plane beneath the antenna.

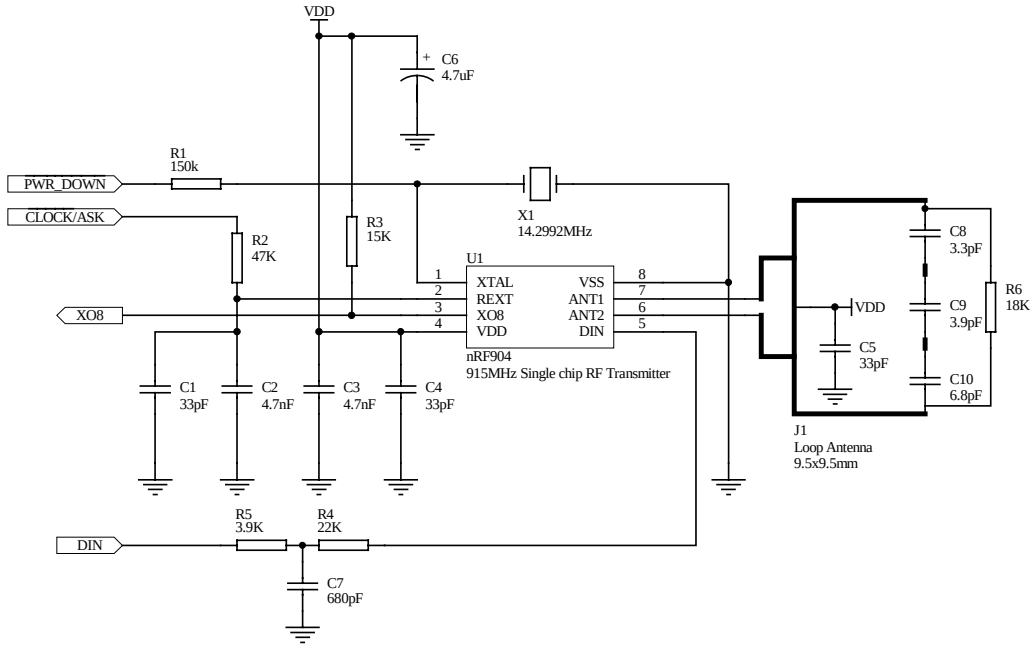
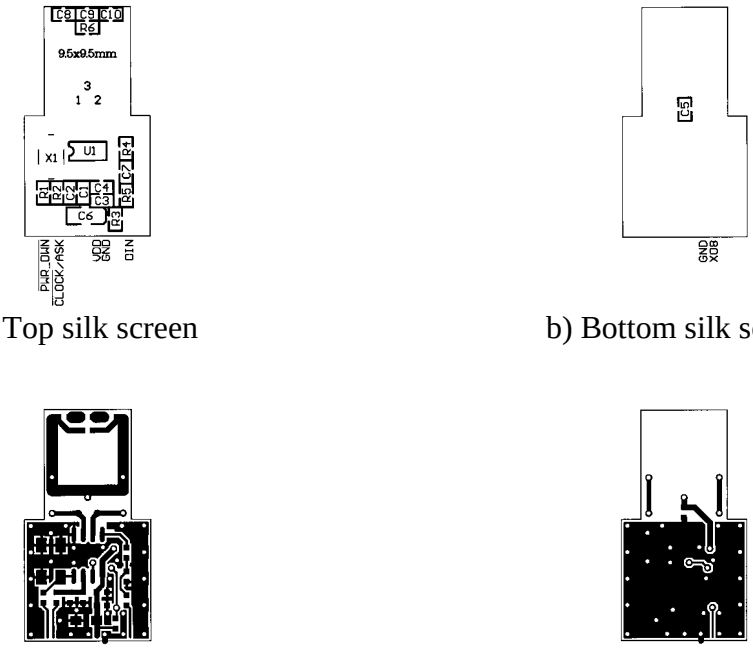



Figure 10. nRF904 application schematic.

| Component | Description | Size | Value | Tolerance | Units |
|---|---|---|---|---|---|
| C1 | NP0 ceramic chip capacitor, (REXT pin decoupling) | 0603 | 33 | | pF |
| C2 | X7R ceramic chip capacitor, (REXT pin decoupling) | 0603 | 4.7 | | nF |
| C3 | X7R ceramic chip capacitor, (Supply decoupling) | 0603 | 4.7 | | nF |
| C4 | NP0 ceramic chip capacitor, (Supply decoupling) | 0603 | 33 | | pF |
| C5 | NP0 ceramic chip capacitor, (Supply decoupling) | 0603 | 33 | | pF |
| C6 | Tantalum chip capacitor, (Supply decoupling) | 3216 | 4.7 | | µF |
| C7 | X7R ceramic chip capacitor, (Data bit stream filter) | 0603 | 680 | | pF |
| C8 | NP0 ceramic chip capacitor, (Antenna tuning) | 0603 | 3.3 | ±0.1 | pF |
| C9 | NP0 ceramic chip capacitor, (Antenna tuning) | 0603 | 3.9 | ±0.1 | pF |
| C10 | NP0 ceramic chip capacitor, (Antenna tuning) | 0603 | 6.8 | ±0.1 | pF |
| R1 | 0.1W chip resistor, (Crystal oscillator bias) | 0603 | 150 | | kΩ |
| R2 | 0.1W chip resistor, (Transmitter power setting) | 0603 | 47 | | kΩ |
| R3 | 0.1W chip resistor, (XO8 output level setting) | 0603 | 15 | | kΩ |
| R4 | 0.1W chip resistor, (Data bit stream filter/Frequency deviation setting) | 0603 | 22 | | kΩ |
| R5 | 0.1W chip resistor, (Data bit stream filter/Frequency deviation setting) | 0603 | 3.9 | | kΩ |
| R6 | 0.1W chip resistor, (Antenna Q reduction) | 0603 | 18 | | kΩ |
| X1 | Crystal | - | 14.094-14.500 | | MHz |

Table 10. Recommended external components.




a) Top silk screen

b) Bottom silk screen

c) Top view

d) Bottom view

Figure 11. PCB layout (example) for nRF904 with loop antenna.

# DEFINITIONS

| **Data sheet status** | |
|---|---|
| Objective product specification | This datasheet contains target specifications for product development. |
| Preliminary product specification | This datasheet contains preliminary data; supplementary data may be published from Nordic VLSI ASA later. |
| Product specification | This datasheet contains final product specifications. Nordic VLSI ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| **Limiting values** | |
| Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Specifications sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |

Table 11. Definitions**.**

Nordic VLSI ASA reserves the right to make changes without further notice to the product to improve reliability, function or design. Nordic VLSI does not assume any liability arising out of the application or use of any product or circuits described herein.

# LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Nordic VLSI ASA customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Nordic VLSI ASA for any damages resulting from such improper use or sale.

Product specification: Revision Date: 30.10.2001.

Datasheet order code: 301001-nRF904.

# YOUR NOTES

# Nordic VLSI ASA – World Wide Distributors

## For Your nearest dealer, please see http://www.nvlsi.no

**Main Office:**
Vestre Rosten 81, N-7075 Tiller, Norway
Phone: +47 72 89 89 00, Fax: +47 72 89 89 89
**E-mail: nRF@nvlsi.no**
**Visit the Nordic VLSI ASA website at http://www.nvlsi.no**