DATA SHEET

NE527
Voltage comparator

Product data
Supersedes data of 1994 Aug 31
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Philips
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Voltage comparator NE527

DESCRIPTION

The NE527 is a high-speed analog voltage comparator which, for the first time, mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed TTL gates with a precision linear amplifier on a single monolithic chip. The NE527 is similar in design to the Philips Semiconductors NE529 voltage comparator except that it incorporates an “Emitter-Follower” input stage for extremely low input currents. This opens the door to a whole new range of applications for analog voltage comparators.

FEATURES

- 15 ns propagation delay
- Complementary output gates
- TTL or ECL compatible outputs
- Wide common-mode and differential voltage range
- Typical gain of 5000

PIN CONFIGURATIONS

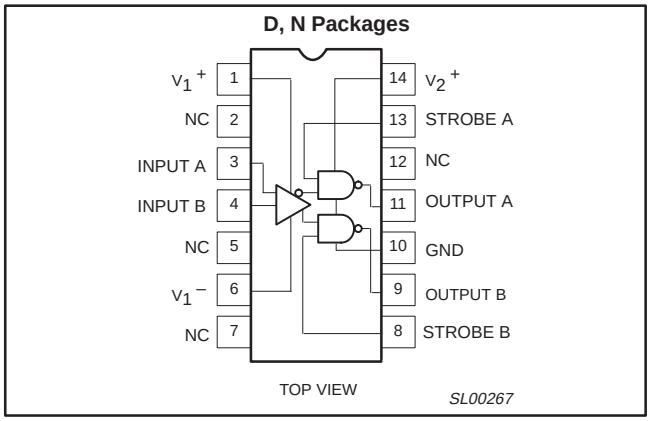


Figure 1. Pin Configuration

APPLICATIONS

- A/D conversion
- ECL-to-TTL interface
- TTL-to-ECL interface
- Memory sensing
- Optical data coupling

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Dual In-Line Package (DIP)	0 °C to +70 °C	NE527N	SOT27-1
14-Pin Small Outline (SO) Package	0 °C to +70 °C	NE527D	SOT108-1

EQUIVALENT SCHEMATIC

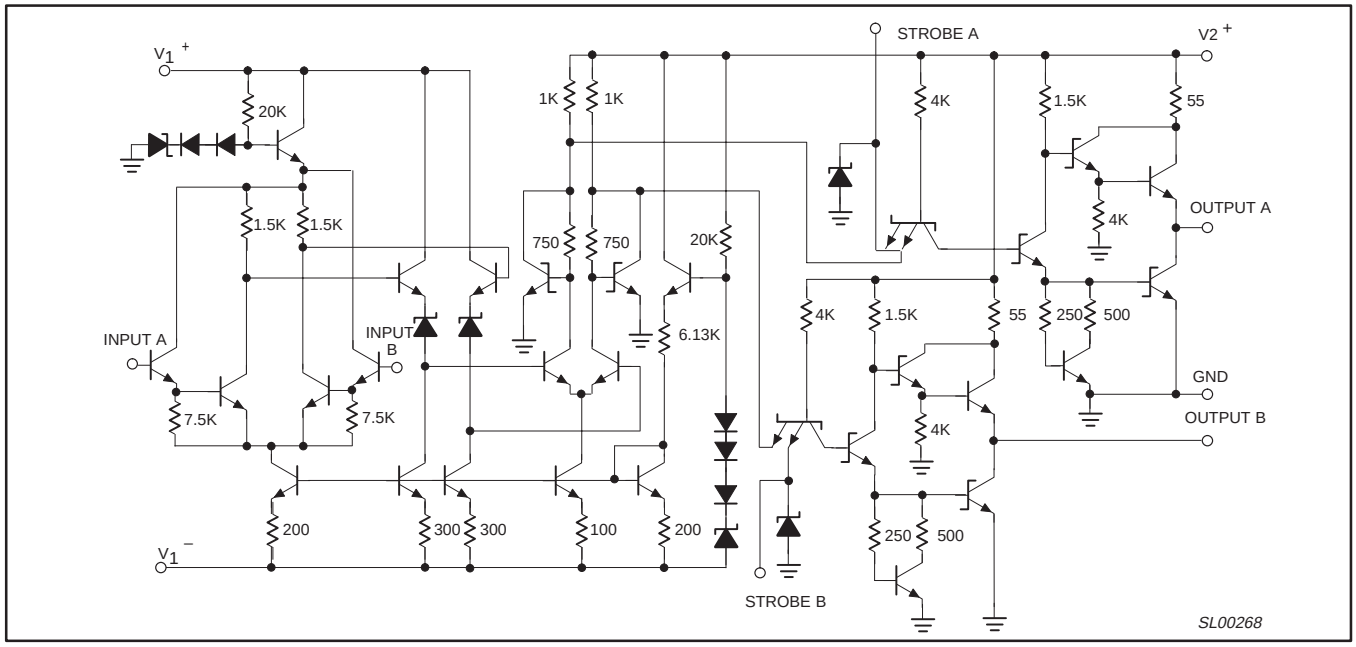


Figure 2. Equivalent Schematic

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_1+	Positive supply voltage	+15	V
V_1-	Negative supply voltage	–15	V
V_2+	Gate supply voltage	+7	V
V_{OUT}	Output voltage	+7	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Input common mode voltage	±6	V
P_D	Max power dissipation[1] 25 °C ambient (still air) N package D package	 1420 1040	 mW mW
T_{amb}	Operating temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C
T_{sld}	Lead soldering temperature (10sec max)	+230	°C

NOTES:
1. Derate above 25 °C, at the following rates:
   N package 11.4 mW/°C
   D package 8.3 mW/°C

BLOCK DIAGRAM

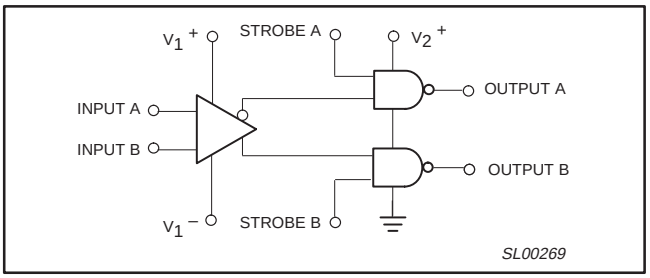


Figure 3. Block Diagram

DC ELECTRICAL CHARACTERISTICS

V_1+ = 10V; V_1- = –10 V; V_2+ = +5.0 V; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	NE527			UNIT
			Min	Typ	Max	
Input characteristics						
V_{OS}	Input offset voltage @ 25 °C				6	mV
	over temperature range				10	
I_{BIAS}	Input bias current @ 25 °C				2	µA
	over temperature range				4	
I_{OS}	Input offset current @ 25 °C				0.75	µA
	over temperature range	V_{IN} = 0 V			1	µA
V_{CM}	Common-mode voltage range		–5		+5	V
Gate characteristics						
V_{OUT}	Output Voltage					
	"1" State	V_2+ = 4.75 V; I_{SOURCE} = –1 mA	2.7	3.3		V
	"0" State	V_2+ = 4.75 V; I_{SINK} = 10 mA			0.5	V
	Strobe inputs					
	"0" Input current[1]	V_2+ = 5.25 V; V_{STROBE} = 0.5 V			–2	mA
	"1" Input current @ 25 °C[1]	V_2+ = 5.25 V; V_{STROBE} = 2.7 V			100	µA
	Over temperature range	V_2+ = 5.25 V; V_{STROBE} = 2.7 V			200	µA
	"0" Input voltage	V_2+ = 4.75 V			0.8	V
	"1" Input voltage	V_2+ = 4.75 V	2.0			V
I_{SC}	Short-circuit output current	V_2+ = 5.25 V;V_{OUT} = 0 V	–18		–70	mA
Power supply requirements						
	Supply voltage					
V_1+			5		10	V
V_1-			–6		–10	V
V_2+			4.75	5	5.25	V
	Supply current	V_1+ = 10 V; V_1- = –10 V				
		V_2+ = 5.25 V				
I_1+		Over temp.			5	mA
I_1-		Over temp.			10	mA
I_2+		Over temp.			20	mA

NOTE:
1. See Logic Function Table.

AC ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C, unless otherwise specified. (See AC test circuit)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Transient response propagation delay time					
t_{PLH}	Low-to-High	V_{IN} = ±100 mV step		16	26	ns
t_{PHL}	High-to-Low			14	24	ns
	Delay between output A and B			2	5	ns
	Strobe delay time					
t_{ON}	Turn-on time			6		ns
t_{OFF}	Turn-off time			6		ns

TYPICAL PERFORMANCE CHARACTERISTICS

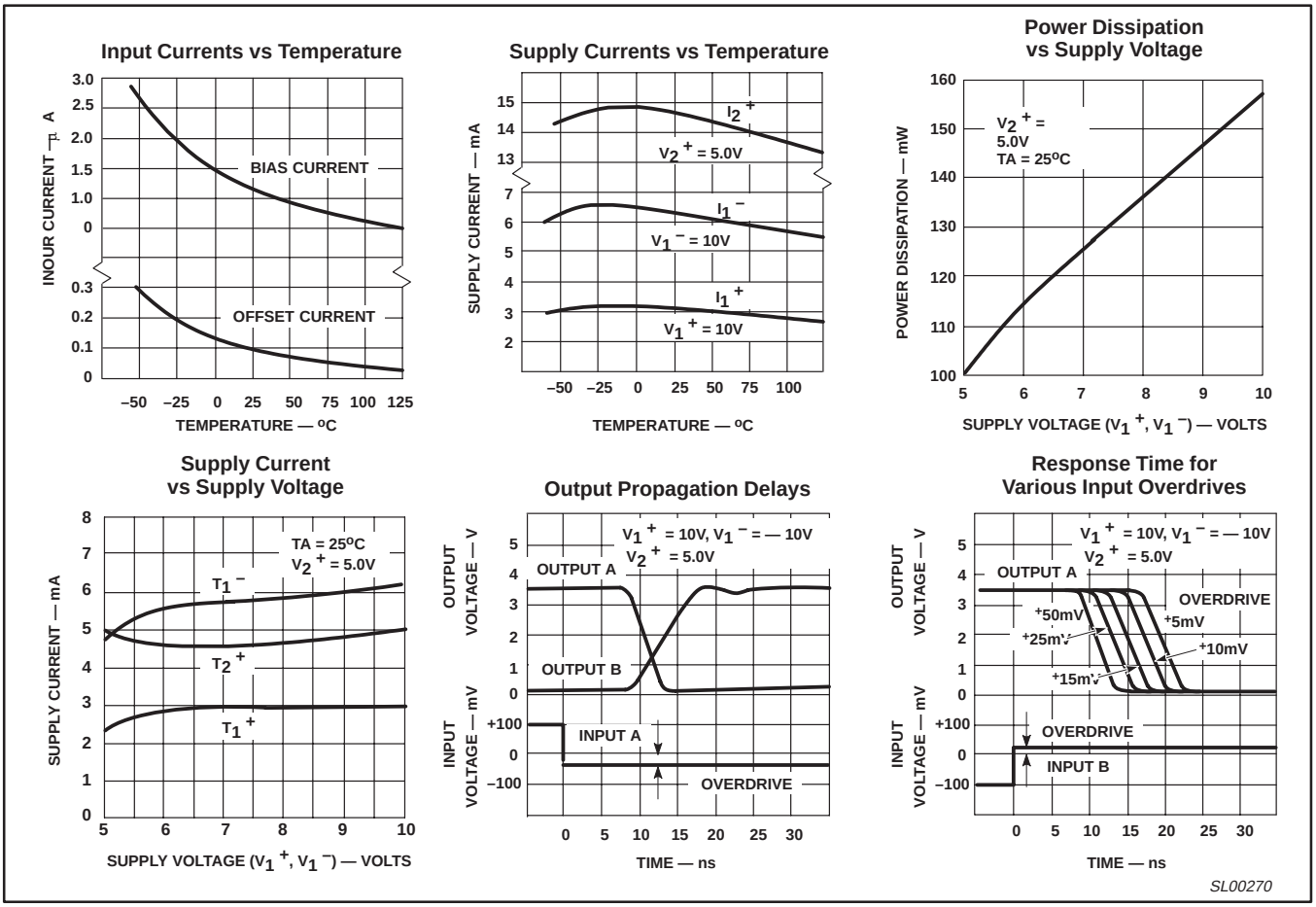


Figure 4. Typical Performance Characteristics

RESPONSE TIME TEST CIRCUIT

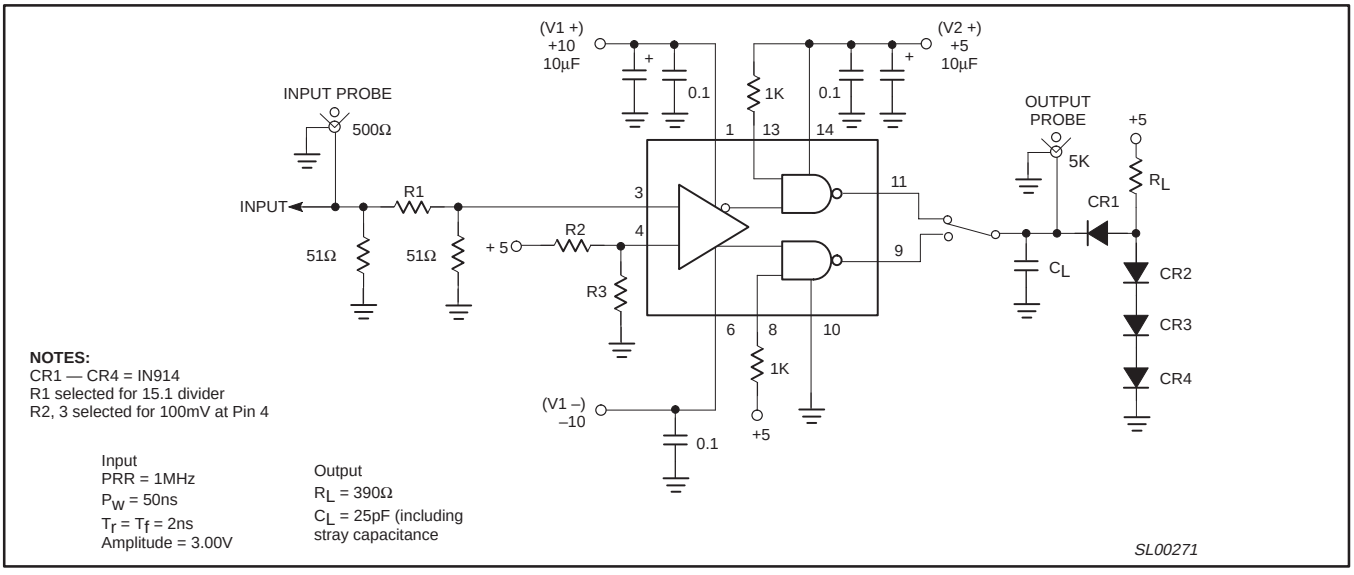


Figure 5. Response Time Test Circuit

APPLICATIONS

One of the main features of the device is that supply voltages (V_1+, V_1–) need not be balanced, as in the following diagrams. For proper operation, however, negative supply (V_1–) should always be at least 6 V more than the ground terminal (Pin 6). Input common-mode range should be limited to values of 2 V less than the supply voltages (V_1+ and V_1–) up to a maximum of ±5 V as supply voltages are increased. It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

LOGIC FUNCTION

V_{ID} (A^+, B^-)	STROBE A	STROBE B	OUTPUT A	OUTPUT B	COMMENT
$V_{ID} \leq -V_{OS}$	H	X	L	H	Read I_{IHA}, I_{ILB}
$-V_{OS} < V_{ID} < V_{OS}$	H	H	Undefined	Undefined	
$V_{ID} \geq V_{OS}$	X	H	H	L	Read I_{ILA}, I_{IHB}
X	L	L	H	H	

TYPICAL APPLICATIONS

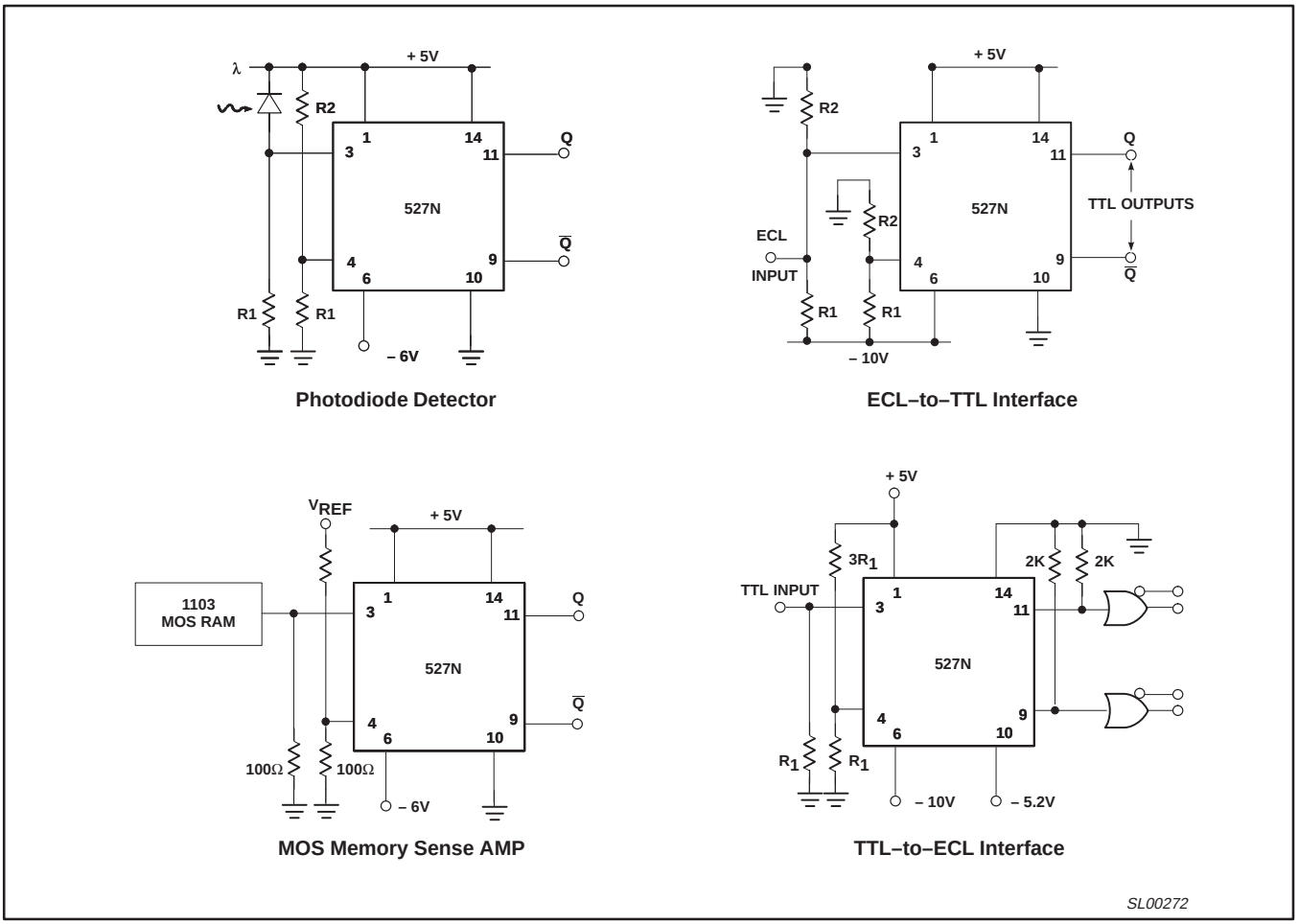
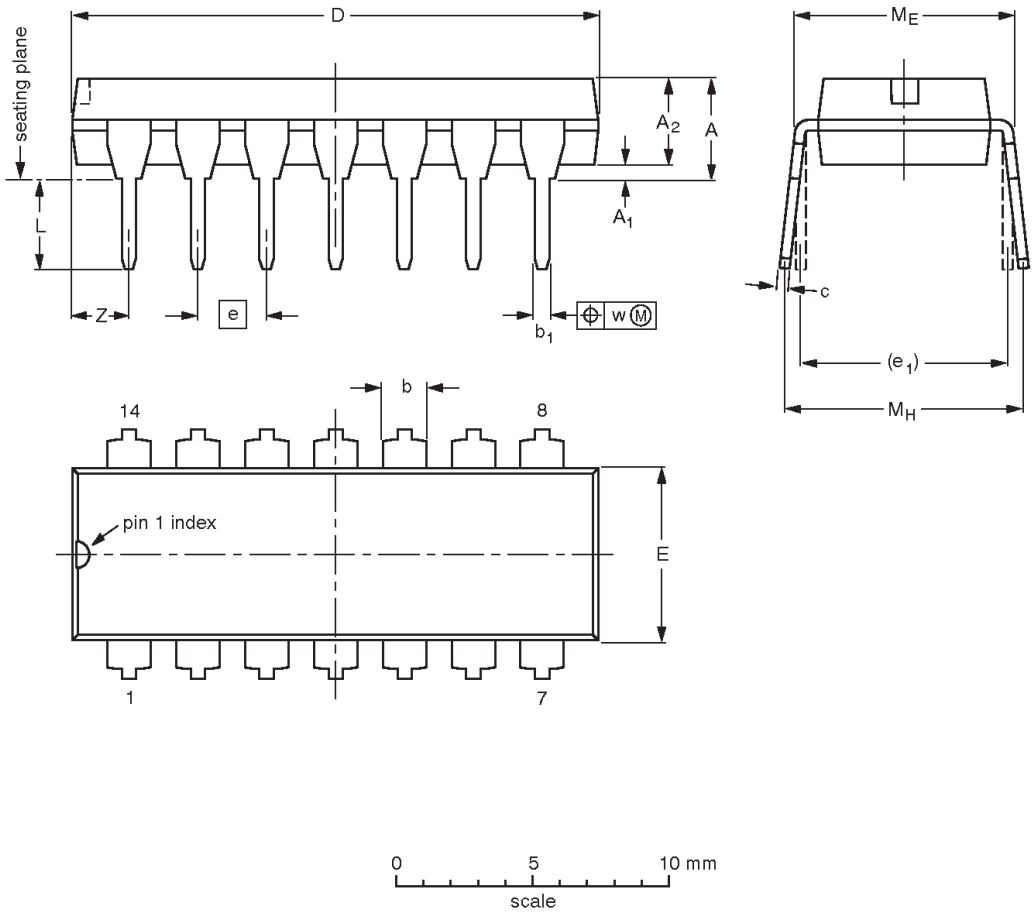


Figure 6. Typical Applications

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

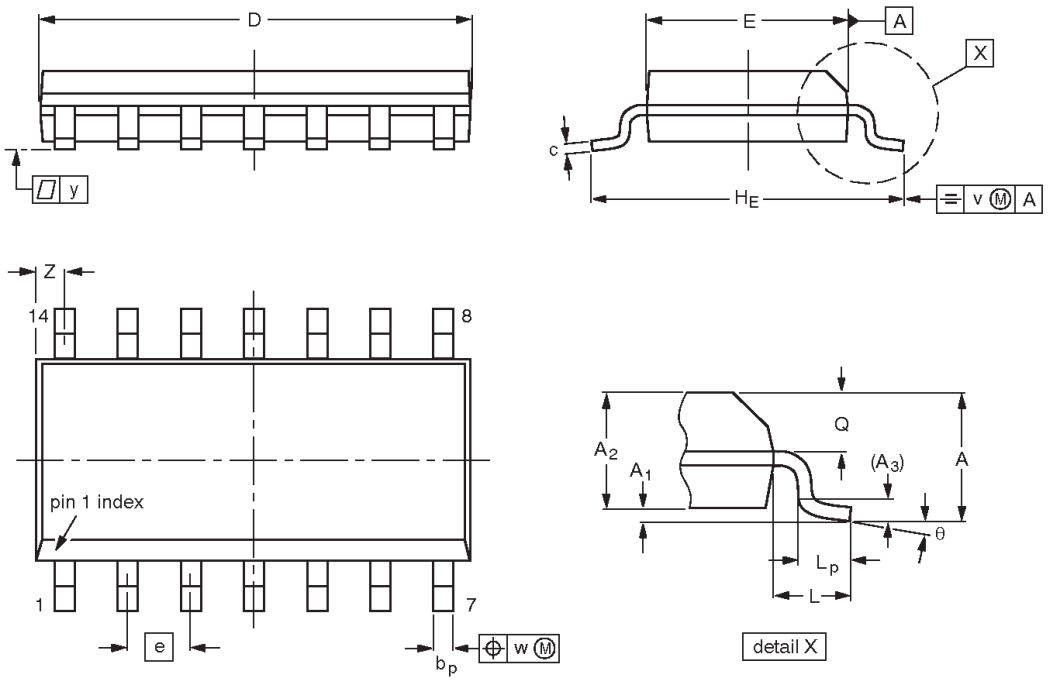
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

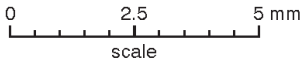
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001	SC-501-14			~~95-03-11~~ 99-12-27

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06	MS-012				~~97-05-22~~ 99-12-27

NOTES

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