Integrated Circuit Systems, Inc.

Product Brief

M906-02

VCSO Based Clock Generator

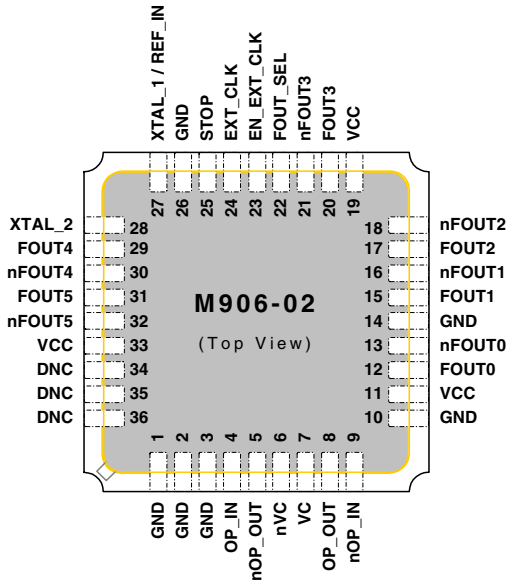
General Description

The M906-02 is a PLL (Phase Locked Loop) based clock generator that uses an internal VCSO (Voltage Controlled SAW Oscillator) to produce a very low jitter output clock. An output clock frequency of 155.52MHz or 77.76MHz is provided from six LVPECL clock output pairs. The accuracy of the output frequency is assured by the internal PLL that phase-locks the internal VCSO to the 19.44MHz frequency reference input. The input reference can either be an external crystal, utilizing the internal crystal oscillator, or a stable external clock source such as a canned crystal oscillator.

Features

- 155.52MHz or 77.76MHz output clock frequency (For other output frequencies, consult factory)
- Six identical LVPECL output pairs
- Low jitter 0.7ps rms (over 12kHz-20MHz)
- Ideal for OC-48/STM-16 clock reference
- Output-to-output skew < 250ps
- 19.44MHz XTAL or LVCMOS reference input
- Selectable external feed-through clock input
- STOP clock input (Logic 1 stops output clocks)
- Integrated SAW (surface acoustic wave) delay line
- Single 3.3V power supply
- Small 9 x 9 mm SMT (surface mount) package

Pin Assignment (9 x 9 mm SMT)



Example Output Frequency Configurations

Ref Clock Frequency (MHz)	VCSO Frequency (MHz)	P Divider Value	Output Frequency (MHz)
19.44	155.52	1	155.52
		2	77.76

Block Diagram