



GENERAL DESCRIPTION



The ICS87972I-147 is a low skew, LVC MOS/LVTTL Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS87972I-147 has three selectable inputs and provides 14 LVC MOS/LVTTL outputs.

The ICS87972I-147 is a highly flexible device. Using the crystal oscillator input, it can be used to generate clocks for a system. All of these clocks can be the same frequency or the device can be configured to generate up to three different frequencies among the three output banks. Using one of the single ended inputs, the ICS87972I-147 can be used as a zero delay buffer/multiplier/divider in clock distribution applications.

The three output banks and feedback output each have their own output dividers which allows the device to generate a multitude of different bank frequency ratios and output-to-input frequency ratios. In addition, 2 outputs in Bank C (QC2, QC3) can be selected to be inverting or non-inverting. The output frequency range is 10MHz to 150MHz. Input frequency range is 6MHz to 150MHz.

The ICS87972I-147 also has a QSYNC output which can be used or system synchronization purposes. It monitors Bank A and Bank C outputs and goes low one period of the faster clock prior to coincident rising edges of Bank A and Bank C clocks. QSYNC then goes high again when the coincident rising edges of Bank A and Bank C occur. This feature is used primarily in applications where Bank A and Bank C are running at different frequencies, and is particularly useful when they are running at non-integer multiples of one another.

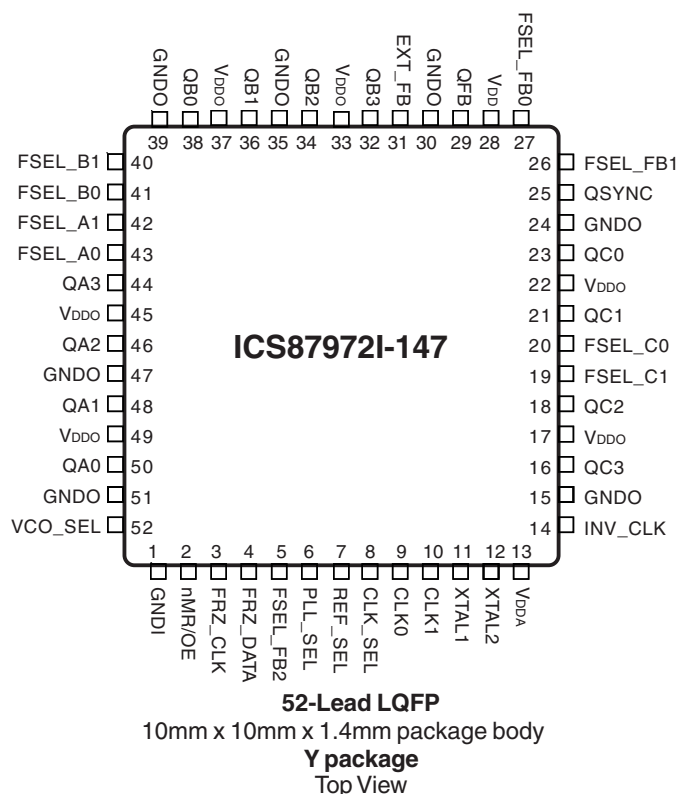
Example Applications:

1. *System Clock generator:* Use a 16.66 MHz Crystal to generate eight 33.33MHz copies for PCI and four 100MHz copies for the CPU or PCI-X.
2. *Line Card Multiplier:* Multiply 19.44MHz from a back plane to 77.76MHz for the line Card ASICs and Serdes.
3. *Zero Delay buffer for Synchronous memory:* Fan out up to twelve 100MHz copies from a memory controller reference clock to the memory chips on a memory module with zero delay.

FEATURES

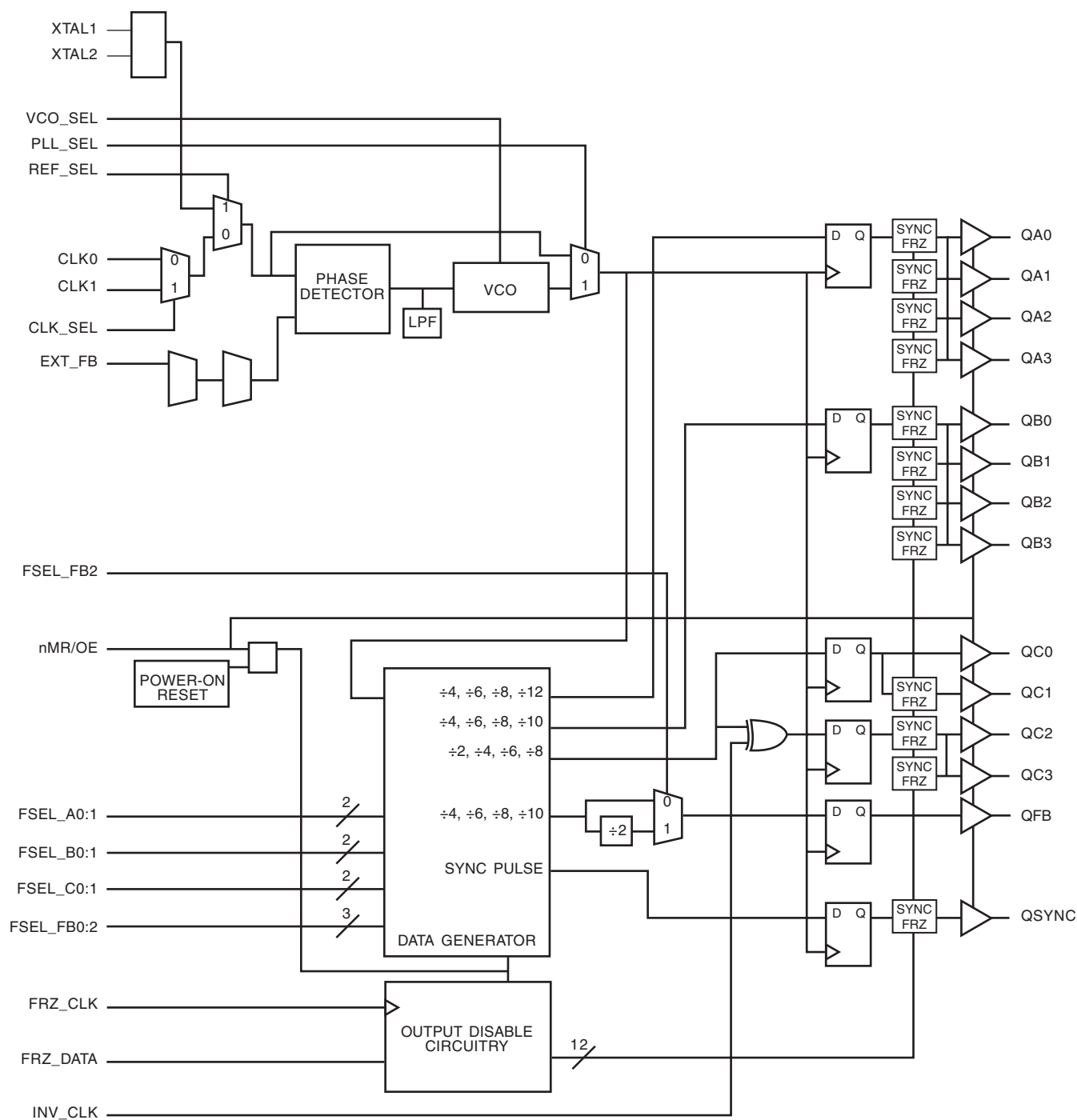
- Fully integrated PLL
- 14 LVC MOS/LVTTL outputs; (12)clocks, (1)feedback, (1)sync
- Selectable crystal oscillator interface or LVC MOS/LVTTL reference clock inputs
- CLK0, CLK1 can accept the following input levels: LVC MOS or LVTTL
- Output frequency range: 10MHz to 150MHz
- VCO range: 240MHz to 500MHz
- Output skew: 200ps (maximum)
- Cycle-to-cycle jitter, (all banks ÷4): 55ps (maximum)
- Full 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Pin compatible with MPC972
- Compatible with PowerPC™ and Pentium™ Microprocessors

PIN ASSIGNMENT





BLOCK DIAGRAM





SIMPLIFIED BLOCK DIAGRAM

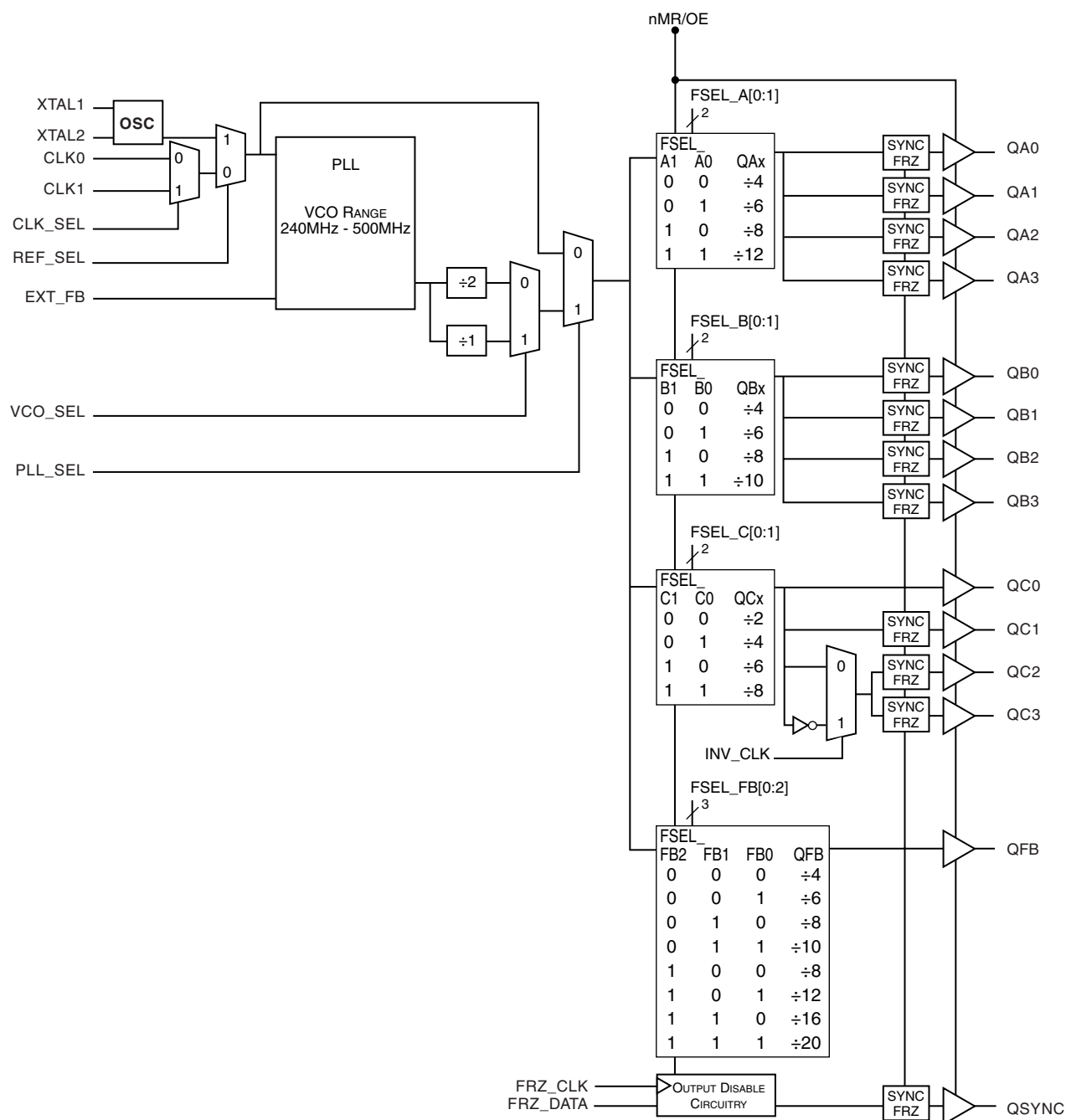




TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	GNDI	Power		Power supply ground.
2	nMR/OE	Input	Pullup	Master reset and output enable. When HIGH, enables the outputs. When LOW, resets the outputs to tristate and resets output divide circuitry. Enables and disables all outputs. LVC MOS / LVTTL interface levels.
3	FRZ_CLK	Input	Pullup	Clock input for freeze circuitry. LVC MOS / LVTTL interface levels.
4	FRZ_DATA	Input	Pullup	Configuration data input for freeze circuitry. LVC MOS / LVTTL interface levels.
5, 26, 27	FSEL_FB2, FSEL_FB1, FSEL_FB0	Input	Pullup	Select pins control Feedback Divide value. LVC MOS / LVTTL interface levels.
6	PLL_SEL	Input	Pullup	Selects between the PLL and reference clocks as the input to the output dividers. When HIGH, selects PLL. When LOW, bypasses the PLL and reference clocks. LVC MOS / LVTTL interface levels.
7	REF_SEL	Input	Pullup	Selects between crystal and reference clock. When LOW, selects CLK0 or CLK1. When HIGH, selects crystal inputs. LVC MOS / LVTTL interface levels.
8	CLK_SEL	Input	Pullup	Clock select input. When LOW, selects CLK0. When HIGH, selects CLK1. LVC MOS / LVTTL interface levels.
9, 10	CLK0, CLK1	Input	Pullup	Reference clock inputs. LVC MOS / LVTTL interface levels.
11, 12	XTAL1, XTAL2	Input		Crystal oscillator interface. XTAL1 is the input. XTAL2 is the output.
13	V _{DDA}	Power		Analog supply pin.
14	INV_CLK	Input	Pullup	Inverted clock select for QC2 and QC3 outputs. LVC MOS / LVTTL interface levels.
15, 24, 30, 35, 39, 47, 51	GNDO	Power		Power supply ground.
16, 18, 21, 23	QC3, QC2, QC1, QC0	Output		Bank C clock outputs. 7Ω typical output impedance. LVC MOS / LVTTL interface levels.
17, 22, 33 37, 45, 49	V _{DDO}	Power		Output supply pins.
19, 20	FSEL_C1, FSEL_C0	Input	Pullup	Select pins for Bank C outputs. LVC MOS / LVTTL interface levels.
25	QSYNC	Output		Synchronization output for Bank A and Bank C. Refer to Figure 1, Timing Diagrams. LVC MOS / LVTTL interface levels.
28	V _{DD}	Power		Core supply pins.
29	QFB	Output		Feedback clock output. LVC MOS / LVTTL interface levels.
31	EXT_FB	Input	Pullup	External feedback. LVC MOS / LVTTL interface levels.
32, 34, 36, 38	QB3, QB2, QB1, QB0	Output		Bank B clock outputs. 7Ω typical output impedance. LVC MOS / LVTTL interface levels.
40, 41	FSEL_B1, FSEL_B0	Input	Pullup	Select pins for Bank B outputs. LVC MOS / LVTTL interface levels.
42, 43	FSEL_A1, FSEL_A0	Input	Pullup	Select pins for Bank A outputs. LVC MOS / LVTTL interface levels.
44, 46, 48, 50	QA3, QA2, QA1, QA0	Output		Bank A clock outputs. 7Ω typical output impedance. LVC MOS / LVTTL interface levels.
52	VCO_SEL	Input	Pullup	Selects VCO. When HIGH, selects VCO ÷ 1. When LOW, selects VCO ÷ 2. LVC MOS / LVTTL interface levels.

NOTE: *Pullup* refers to internal input resistors. See table 2, Pin Characteristics, for typical values.



TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		K Ω
C_{PD}	Power Dissipation Capacitance (per output)	$V_{DDA}, V_{DD}, V_{DDO} = 3.465V$			18	pF
R_{OUT}	Output Impedance		5	7	12	Ω

TABLE 3A. OUTPUT BANK CONFIGURATION SELECT FUNCTION TABLE

Inputs		Outputs	Inputs		Outputs	Inputs		Outputs
FSEL_A1	FSEL_A0	QA	FSEL_B1	FSEL_B0	QB	FSEL_C1	FSEL_C0	QC
0	0	$\div 4$	0	0	$\div 4$	0	0	$\div 2$
0	1	$\div 6$	0	1	$\div 6$	0	1	$\div 4$
1	0	$\div 8$	1	0	$\div 8$	1	0	$\div 6$
1	1	$\div 12$	1	1	$\div 10$	1	1	$\div 8$

TABLE 3B. FEEDBACK CONFIGURATION SELECT FUNCTION TABLE

Inputs			Outputs
FSEL_FB2	FSEL_FB1	FSEL_FB0	QFB
0	0	0	$\div 4$
0	0	1	$\div 6$
0	1	0	$\div 8$
0	1	1	$\div 10$
1	0	0	$\div 8$
1	0	1	$\div 12$
1	1	0	$\div 16$
1	1	1	$\div 20$

TABLE 3C. CONTROL INPUT SELECT FUNCTION TABLE

Control Pin	Logic 0	Logic 1
VCO_SEL	VCO/2	VCO
REF_SEL	CLK0 or CLK1	XTAL
CLK_SEL	CLK0	CLK1
PLL_SEL	BYPASS PLL	Enable PLL
nMR/OE	Master Reset/Output Hi Z	Enable Outputs
INV_CLK	Non-Inverted QC2, QC3	Inverted QC2, QC3

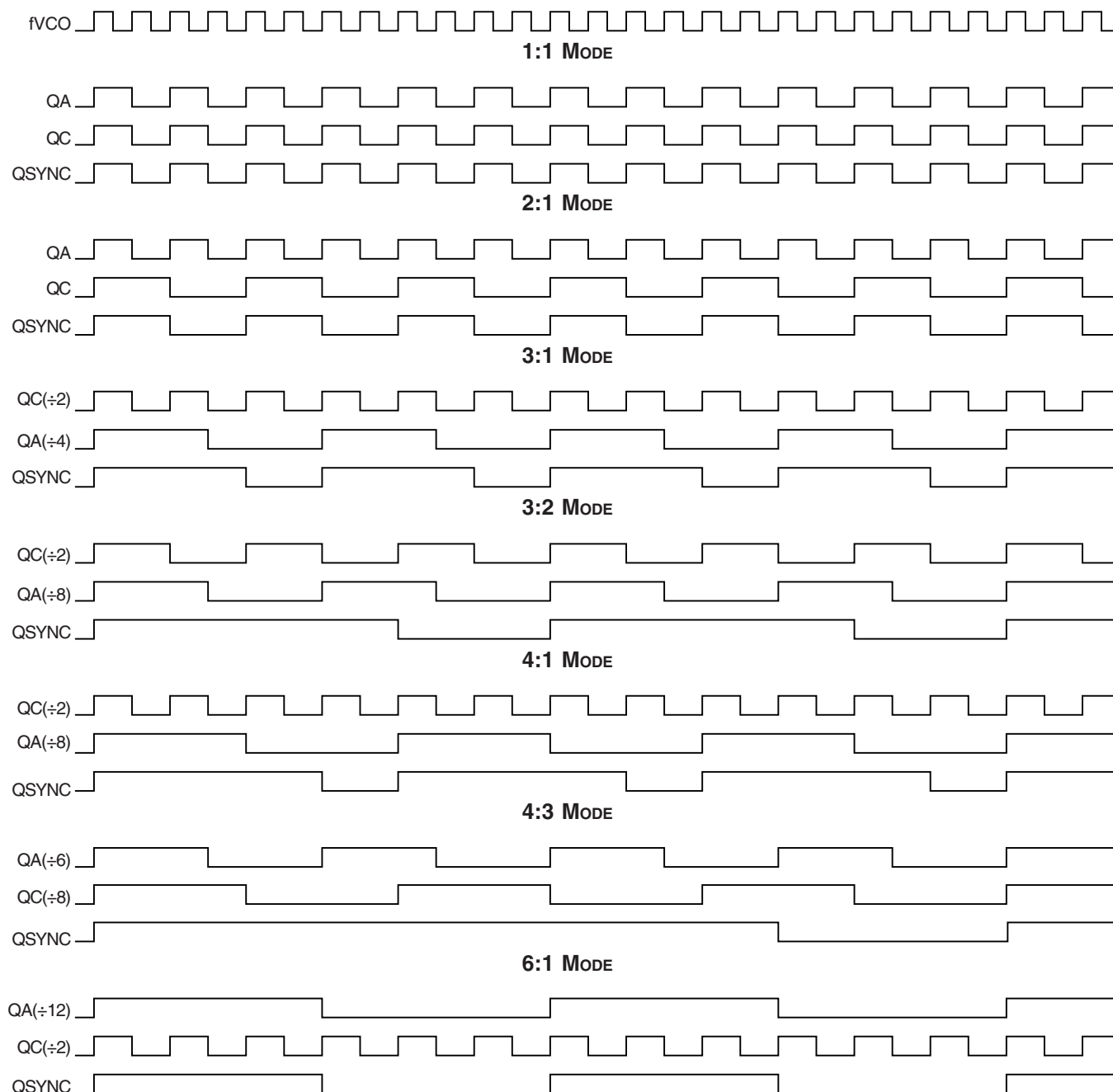


FIGURE 1. TIMING DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to $V_{DD} + 0.5V$
Outputs, V_O	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, θ_{JA}	42.3°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				250	mA
I_{DDA}	Analog Supply Current				20	mA

NOTE: Special thermal handling may be required in some configurations.

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		$V_{DD} + -0.3$	V
V_{IL}	Input Low Voltage	VCO_SEL, PLL_SEL, REF_SEL, CLK_SEL, EXT_FB, FSEL_FB2, nMR/OE, FSEL_X0:1, FSEL_FB0:2, FRZ_DATA	-0.3		0.8	V
		CLK0, CLK1, FRZ_CLK, INV_CLK	-0.3		1.3	V
I_{IN}	Input Current				± 120	μA
V_{OH}	Output High Voltage	$I_{OH} = -20\text{mA}$	2.4			V
V_{OL}	Output Low Voltage	$I_{OL} = 20\text{mA}$			0.5	V

TABLE 5. INPUT FREQUENCY CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	CLK0, CLK1; NOTE 1			150	MHz
		XTAL1, XTAL2	12		40	MHz
		FRZ_CLK			20	MHz

NOTE 1: Input frequency depends on the feedback divide ratio to ensure "clock * feedback divide" is in the VCO range of 240MHz to 500MHz.



TABLE 6. CRYSTAL CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^{\circ}C$ TO $85^{\circ}C$

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		12		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

TABLE 7. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^{\circ}C$ TO $85^{\circ}C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	$\div 2$			150	MHz
		$\div 4$			125	MHz
		$\div 6$			83.33	MHz
		$\div 8$			62.5	MHz
$t(\emptyset)$	Static Phase Offset; NOTE 1	CLK0	QFB $\div 8$		-10	ps
		CLK1	In Frequency = 50MHz		-65	ps
$tsk(o)$	Output Skew; NOTE 2, 4				200	ps
$tjit(cc)$	Cycle-to-Cycle Jitter; NOTE 4	All Banks $\div 4$			55	ps
f_{VCO}	PLL VCO Lock Range		240		500	MHz
t_{LOCK}	PLL Lock Time; NOTE 3				10	ms
t_R / t_F	Output Rise/Fall Time	0.8V to 2V	0.15		0.7	ns
odc	Output Duty Cycle		45		55	%
t_{PZL}, t_{PZH}	Output Enable Time; NOTE 3				10	ns
t_{PLZ}, t_{PHZ}	Output Disable Time; NOTE 3				8	ns

NOTE 1: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.

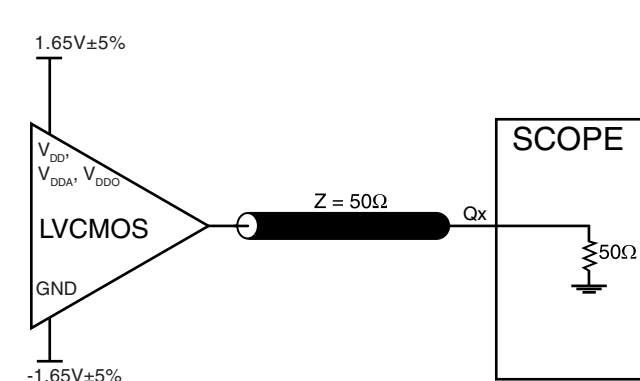
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.

NOTE 3: These parameters are guaranteed by characterization. Not tested in production.

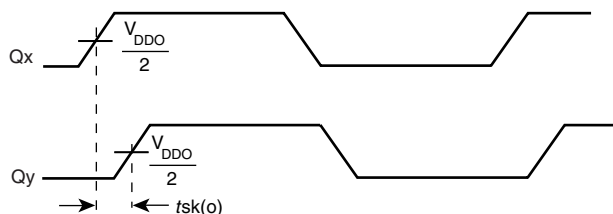
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.



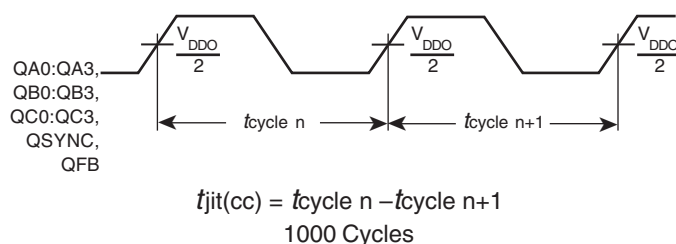
PARAMETER MEASUREMENT INFORMATION



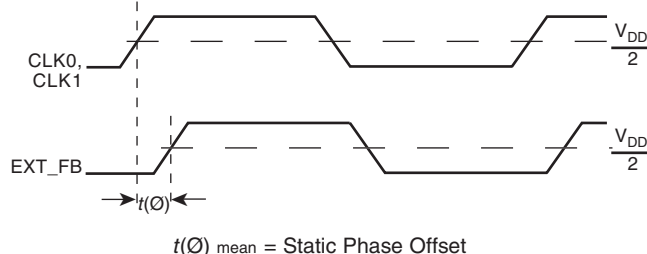
3.3V OUTPUT LOAD AC TEST CIRCUIT



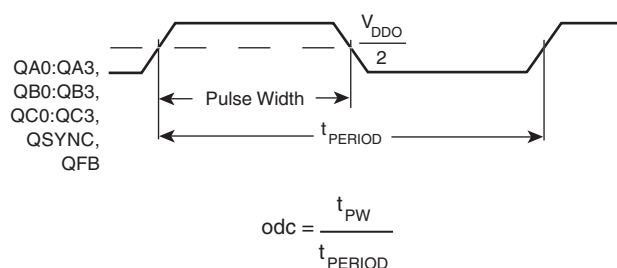
OUTPUT SKEW



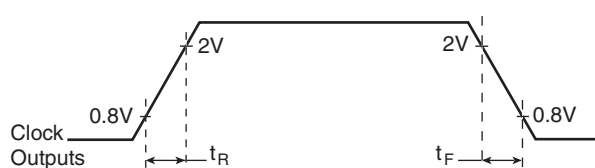
CYCLE-TO-CYCLE JITTER



STATIC PHASE OFFSET



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME



APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS87972I-147 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} , V_{DDA} , and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 2* illustrates how a 10Ω resistor along with a $10\mu\text{F}$ and a $.01\mu\text{F}$ bypass capacitor should be connected to each V_{DDA} pin.

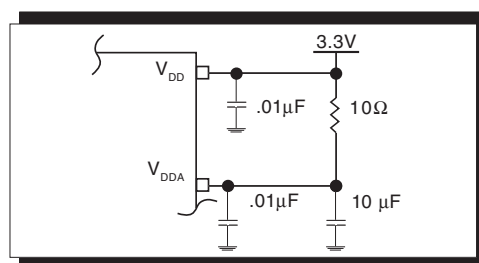


FIGURE 2. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS87972I-147 has been characterized with 18 pF parallel resonant crystals. External capacitors are not required for this crystal interface. While layout the PC board, it is recommended to have spare footprints capacitor C1 and C2. If re-

quired, the spare C1 and C2 footprints can be used for fine tuned further for more accurate frequency. The possible C1 and C2 value are ranged from 2pF – 25pF. The suggest footprint size is 0402 or 0603.

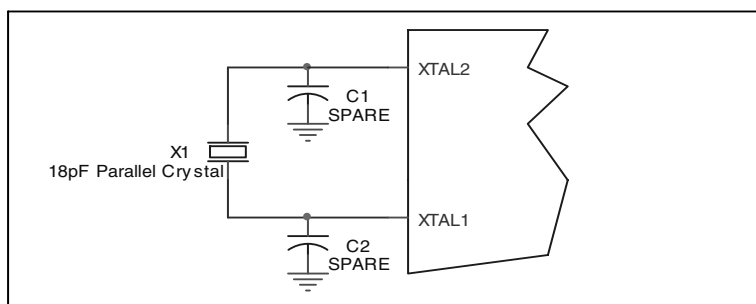


Figure 3. CRYSTAL INPUT INTERFACE



USING THE OUTPUT FREEZE CIRCUITRY

OVERVIEW

To enable low power states within a system, each output of ICS87972I-147 (Except QC0 and QFB) can be individually frozen (stopped in the logic "0" state) using a simple serial interface to a 12 bit shift register. A serial interface was chosen to eliminate the need for each output to have its own Output Enable pin, which would dramatically increase pin count and package cost. Common sources in a system that can be used to drive the ICS87972I-147 serial interface are FPGA's and ASICs.

PROTOCOL

The Serial interface consists of two pins, FRZ_Data (Freeze Data) and FRZ_CLK (Freeze Clock). Each of the outputs which can be frozen has its own freeze enable bit in the 12 bit shift register. The sequence is started by supplying a logic "0" start bit followed by 12NRZ freeze enable bits. The period of each FRZ_DATA bit equals the period of the FRZ_CLK signal. The FRZ_DATA serial transmission should be timed so the ICS87972I-147 can sample each FRZ_DATA bit with the rising edge of the FRZ_CLK signal.

To place an output in the freeze state, a logic "0" must be written to the respective freeze enable bit in the shift register. To unfreeze an output, a logic "1" must be written to the respective freeze enable bit. Outputs will not become enabled/disabled until all 12 data bits are shifted into the shift register. When all 12 data bits are shifted in the register, the next rising edge of FRZ_CLK will enable or disable the outputs. If the bit that is following the 12th bit in the register is a logic "0", it is used for the start bit of the next cycle; otherwise, the device will wait and won't start the next cycle until it sees a logic "0" bit. Freezing and unfreezing of the output clock is synchronous (see the timing diagram below). When going into a frozen state, the output clock will go LOW at the time it would normally go LOW, and the freeze logic will keep the output low until unfrozen. Likewise, when coming out of the frozen state, the output will go HIGH only when it would normally go HIGH. This logic, therefore, prevents runt pulses when going into and out of the frozen state.

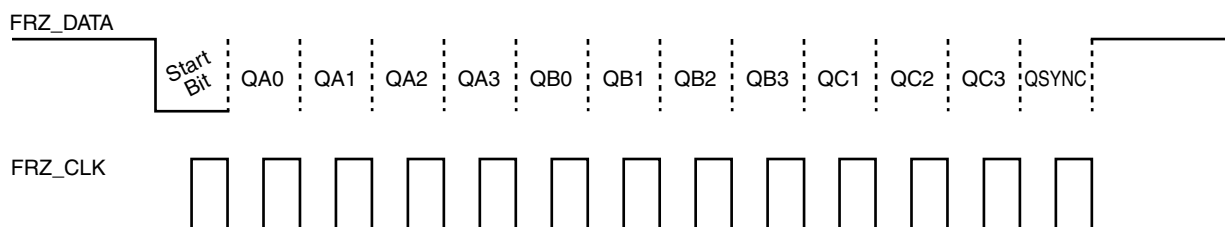


FIGURE 4A. FREEZE DATA INPUT PROTOCOL

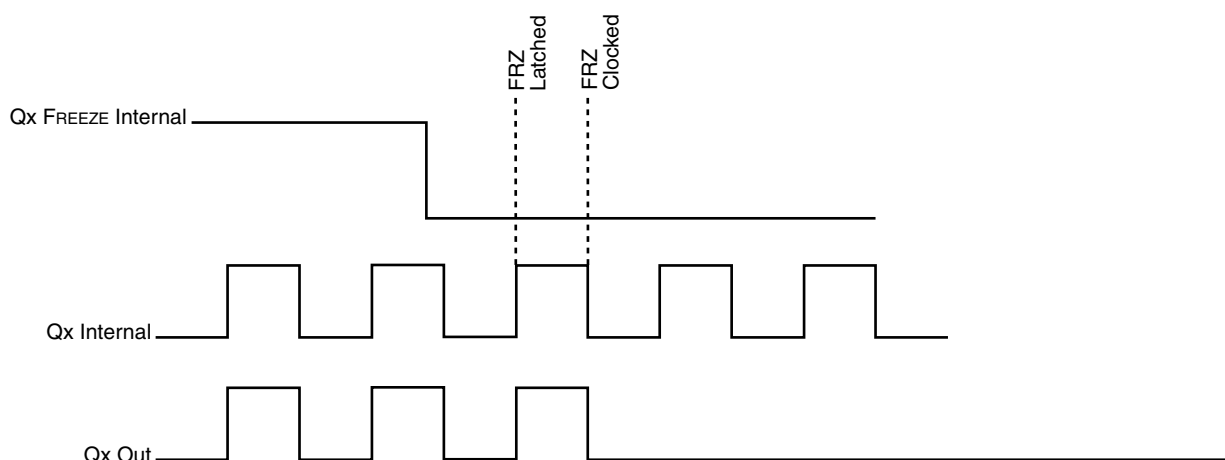


FIGURE 4B. OUTPUT DISABLE TIMING



RELIABILITY INFORMATION

TABLE 8. θ_{JA} vs. AIR FLOW TABLE FOR 52 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	58.0°C/W	47.1°C/W	42.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	42.3°C/W	36.4°C/W	34.0°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

TRANSISTOR COUNT

The transistor count for ICS87972I-147 is: 8364



Integrated
Circuit
Systems, Inc.

ICS87972I-147

LOW SKEW, 1-TO-12

LVC MOS/LVTTL CLOCK MULTIPLIER/ZERO DELAY BUFFER

PACKAGE OUTLINE - Y SUFFIX FOR 52 LEAD LQFP

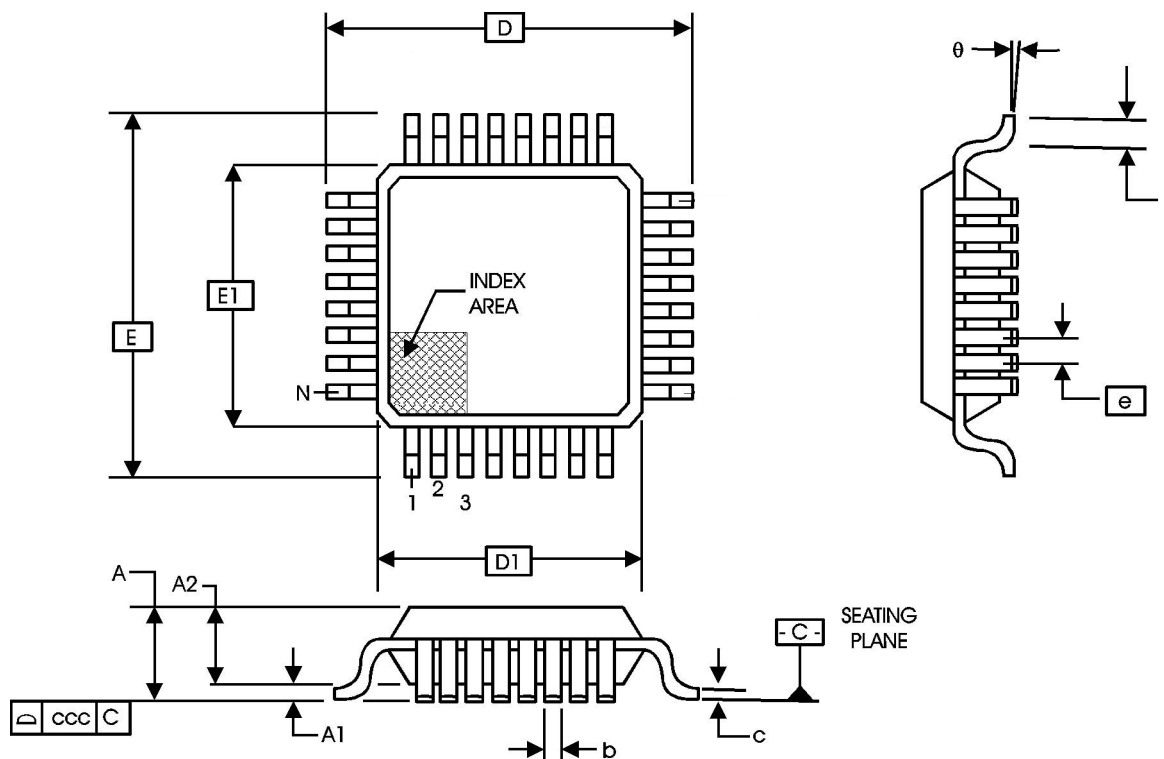


TABLE 9. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BCC		
	MINIMUM	NOMINAL	MAXIMUM
N	52		
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.22	0.32	0.38
b1	0.22	0.30	0.33
D	12.00 BASIC		
D1	10.00 BASIC		
E	12.00 BASIC		
E1	10.00 BASIC		
e	0.65 BASIC		
ccc	0.45	--	0.10
ddd	--	--	0.13

Reference Document: JEDEC Publication 95, MS-026



Integrated
Circuit
Systems, Inc.

ICS87972I-147

LOW SKEW, 1-TO-12
LVCMOS/LVTTL CLOCK MULTIPLIER/ZERO DELAY BUFFER

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS87972DYI-147	ICS87972DYI147	52 Lead LQFP	160 per tray	-40°C to 85°C
ICS87972DYI-147T	ICS87972DYI147	52 Lead LQFP on Tape and Reel	500	-40°C to 85°C

While the information presented herein has been checked for both accuracy and reliability, Integrated Circuit Systems, Incorporated (ICS) assumes no responsibility for either its use or for infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial and industrial applications. Any other applications such as those requiring high reliability, or other extraordinary environmental requirements are not recommended without additional processing by ICS. ICS reserves the right to change any circuitry or specifications without notice. ICS does not authorize or warrant any ICS product for use in life support devices or critical medical instruments.