Integrated Circuit Systems, Inc.

ICS83948I

LOW SKEW, 1-TO-12 DIFFERENTIAL-TO-LVCMOS FANOUT BUFFER

GENERAL DESCRIPTION

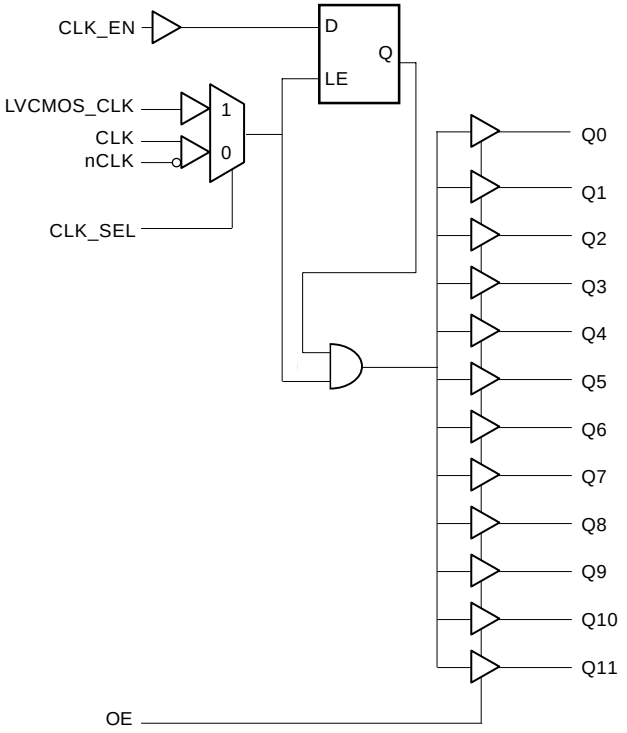
The ICS83948I is a low skew, 1-to-12 Differential-to-LVCMOS Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS83948I has two selectable clock inputs. The CLK, nCLK pair can accept most standard differential input levels. The LVCMOS_CLK can accept LVCMOS or LVTTL input levels. The low impedance LVCMOS outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 12 to 24 by utilizing the ability of the outputs to drive two series terminated lines.

The ICS83948I is characterized at 3.3V core/3.3V output. Guaranteed output and part-to-part skew characteristics make the ICS83948I ideal for those clock distribution applications demanding well defined performance and repeatability.

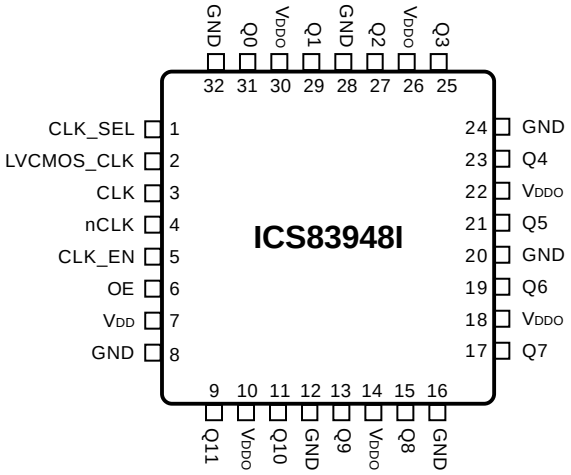
FEATURES

- 12 LVCMOS outputs
- Selectable LVCMOS clock or differential CLK, nCLK inputs
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- LVCMOS_CLK accepts the following input levels: LVCMOS or LVTTL
- Maximum output frequency: 250MHz
- Output skew: 350ps (maximum)
- Part to part skew: 1.5ns (maximum)
- 3.3V core, 3.3V output
- -40°C to 85°C ambient operating temperature
- Pin compatible with the MPC948/948L

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	CLK_SEL	Input	Pullup	Clock select input. Selects LVCMOS clock input when HIGH. Selects CLK, nCLK inputs when LOW. LVCMOS / LVTTL interface levels.
2	LVCMOS_CLK	Input	Pullup	Clock input. LVCMOS / LVTTL interface levels.
3	CLK	Input	Pullup	Non-inverting differential clock input.
4	nCLK	Input	Pulldown	Inverting differential clock input.
5	CLK_EN	Input	Pullup	Clock enable. LVCMOS / LVTTL interface levels.
6	OE	Input	Pullup	Output enable. LVCMOS / LVTTL interface levels.
7	V_{DD}	Power		Core supply pin.
8, 12, 16, 20, 24, 28, 32	GND	Power		Power supply ground.
9, 11, 13, 15, 17, 19, 21, 23 25, 27, 29, 31	Q11, Q10, Q9, Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	Output		Clock outputs. LVCMOS / LVTTL interface levels.
10, 14, 18, 22, 26, 30	V_{DDO}	Power		Output supply pins.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
C_{PD}	Power Dissipation Capacitance (per output)			25		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
R_{OUT}	Output Impedance			7		Ω

TABLE 3A. CLOCK SELECT FUNCTION TABLE

Control Input	Clock	
CLK_SEL	CLK, nCLK	LVCMOS_CLK
0	Selected	De-selected
1	De-selected	Selected

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs				Outputs	Input to Output Mode	Polarity
CLK_SEL	LVCMOS_CLK	CLK	nCLK	Q0:Q12		
0	—	0	1	LOW	Differential to Single Ended	Non Inverting
0	—	1	0	HIGH	Differential to Single Ended	Non Inverting
0	—	0	Biased; NOTE 1	LOW	Single Ended to Single Ended	Non Inverting
0	—	1	Biased; NOTE 1	HIGH	Single Ended to Single Ended	Non Inverting
0	—	Biased; NOTE 1	0	HIGH	Single Ended to Single Ended	Inverting
0	—	Biased; NOTE 1	1	LOW	Single Ended to Single Ended	Inverting
1	0	—	—	LOW	Single Ended to Single Ended	Non Inverting
1	1	—	—	HIGH	Single Ended to Single Ended	Non Inverting

NOTE 1: Please refer to the Application Information section, "Wiring the Differential Input to Accept Single Ended Levels".

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±0.3V, T_A = -40° TO 85°

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.0	3.3	3.6	V
V_{DDO}	Output Supply Voltage		3.0	3.3	3.6	V
I_{DD}	Power Supply Current				55	mA

TABLE 4B. DC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±0.3V, T_A = -40° TO 85°

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{PP}	Peak-to-Peak Input Voltage		0.15		1.3	V
V_{CMR}	Input Common Mode Voltage; NOTE 1, 2		GND + 0.5		V_{DD} - 0.85	V
I_{IN}	Input Current				±100	µA
V_{OH}	Output High Voltage	I_{OH} = -20mA	2.5			V
V_{OL}	Output Low Voltage	I_{OL} = 20mA			0.4	V

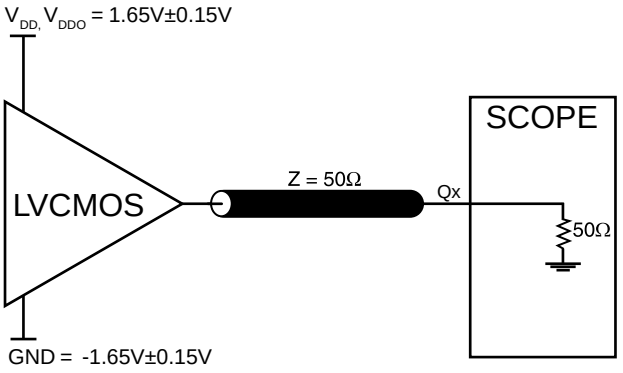
NOTE 1: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 5. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 0.3V$, $T_A = -40°$ TO $85°$

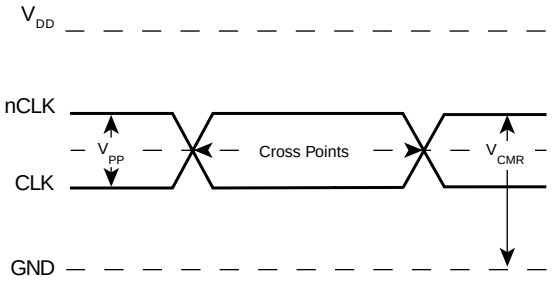
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					250	MHz
t_{PD}	Propagation Delay	CLK, nCLK; NOTE 1A	f ≤ 150MHz	2.25		3.75	ns
		LVCMOS_CLK; NOTE 1B	f ≤ 150MHz	2		4	ns
*t*sk(o)	Output Skew; NOTE 2, 6		Measured on rising edge @V_{DDO}/2			350	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 6	CLK, nCLK	Measured on rising edge @V_{DDO}/2			1.5	ns
		LVCMOS_CLK				2	ns
t_R	Output Rise Time		0.8V to 2V	0.2		1.0	ns
t_F	Output Fall Time		0.8V to 2V	0.2		1.0	ns
t_{PW}	Output Pulse Width		f < 150MHz	tCycle/2 - 800		tCycle/2 + 800	ps
t_{PZL}, t_{PZH}	Output Disable Time; NOTE 4					11	ns
t_{PLZ}, t_{PHZ}	Output Enable Time; NOTE 4					11	ns
t_S	Clock Enable Setup Time; NOTE 5	CLK_EN to CLK, nCLK		1			ns
		CLK_EN to LVCMOS_CLK		0			ns
t_H	Clock Enable Hold Time; NOTE 5	CLK, nCLK to CLK_EN		1			ns
		LVCMOS_CLK to CLK_EN		1			ns

NOTE 1A: Measured from the differential input crossing point to V_{DDO}/2 of the output.
NOTE 1B: Measured from the V_{DD}/2 or crosspoint of the input to V_{DDO}/2 of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: Setup and Hold times are relative to the rising edge of the input clock.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

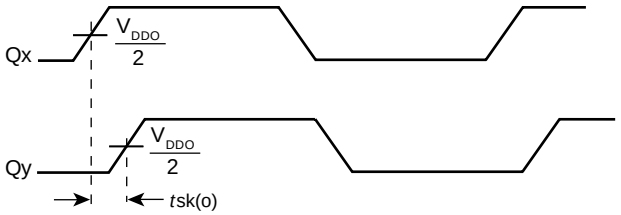
PARAMETER MEASUREMENT INFORMATION



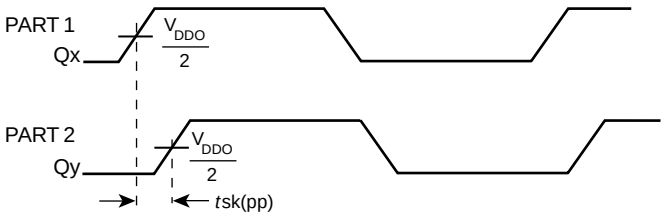
3.3V OUTPUT LOAD AC TEST CIRCUIT



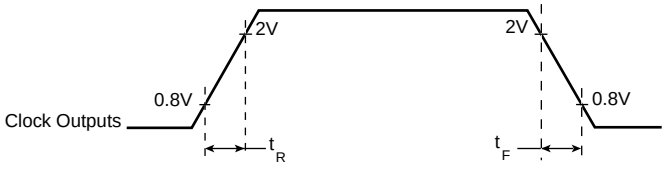
DIFFERENTIAL INPUT LEVEL



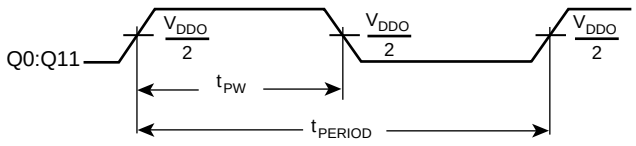
OUTPUT SKEW



PART-TO-PART SKEW

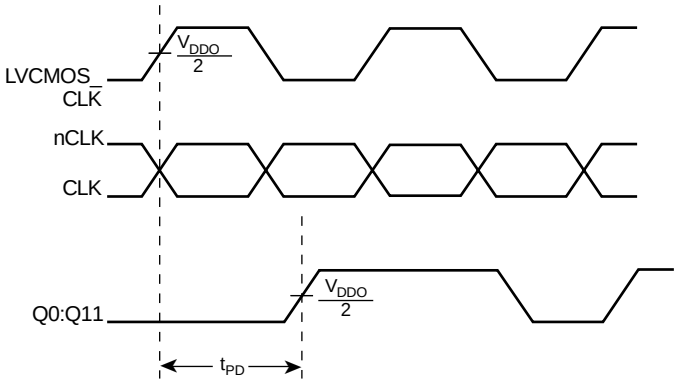


OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

t_{PW} & t_{PERIOD}



PROPAGATION DELAY

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

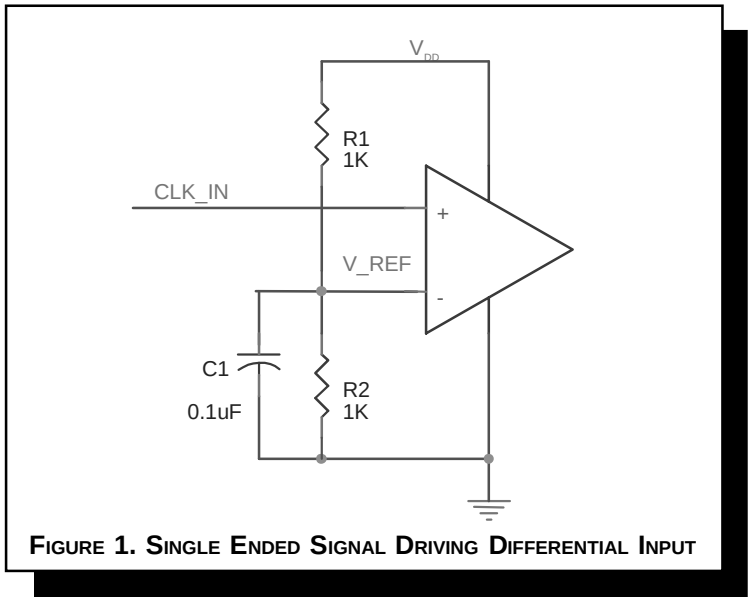


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS83948I is: 1040

PACKAGE OUTLINE - Y SUFFIX

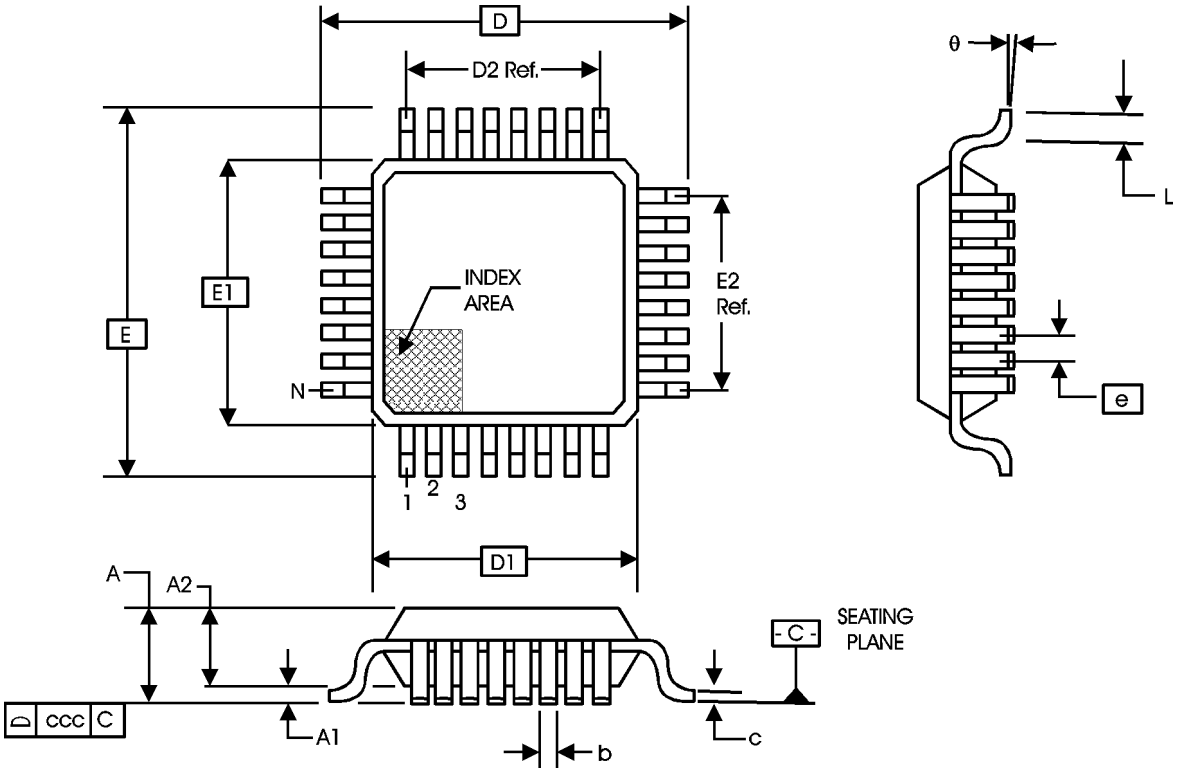


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

REFERENCE DOCUMENT: JEDEC PUBLICATION 95, MS-026

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS83948AYI	ICS83948AYI	32 Lead LQFP	250 per tray	-40°C to 85°C
ICS83948AYIT	ICS83948AYI	32 Lead LQFP on Tape and Reel	1000	-40°C to 85°C

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	T5	4	AC Characteristics table - t_{LZ}, t_{HZ} row changed symbol to read t_{PLZ}, t_{PHZ} and changed Parameter to read Output Enable Time. Added rows: t_S "Clock Enable Setup Time" and t_H "Clock Enable Hold Time".	05/20/02
B	T5	4	AC Characteristics table, t_S and t_H rows - replaced SYNC_OE with CLK_EN. Added an extra note to Propagation Delay row.	6/26/02
B	T5	4	AC Characteristics table, f_{MAX} row corrected typo error of 150MHz to 250MHz.	8/8/02
B	T5	4	AC Characteristics table - tPW row, added f< 150MHz for tPW Test Conditions.	11/11/02