HI5813

CMOS 3.3V, 25 Microsecond, 12-Bit, Sampling A/D Converter with Internal Track and Hold

August 1997

Features

- **Conversion Time 25μs**
- **Throughput Rate . . . . . .40 KSPS**
- **Built-In Track and Hold**
- **Single Supply Voltage . . . . . +3.3V**
- **Maximum Power Consumption at 25°C. 3.3mW**

Applications

- **Remote Low Power Data Acquisition Systems**
- **Battery Operated Systems**
- **Pen Based PC Handheld Scanners**
- **DSP Modems**
- **General Purpose DSP Front End**
- **μP Controlled Measurement Systems**
- **PCMCIA Type II Compliant**
- **PC Based Industrial Controls/DAQ Systems**

Description

The HI5813 is a 3.3V, very low power, 12-bit, successive approximation analog-to-digital converter. It can operate from a single 3V to 6V supply and typically draws a maximum of 1.0mA (at 25°C) when operating at 3.3V. The HI5813 features a built-in track and hold. The conversion time is as low as 25μs with a 3.3V supply.

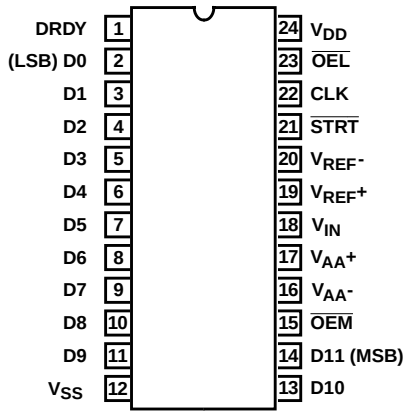
The twelve data outputs feature full high speed CMOS three-state bus driver capability, and are latched and held through a full conversion cycle. The output is user selectable: (i.e.) 12-bit , 8-bit (MSBs), and/or 4-bit (LSBs). A data ready flag and conversion start input complete the digital interface.

Ordering Information

PART NUMBER	INL (LSB) (MAX OVER TEMP.)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI5813JIP	±4.0	-40 to 85	24 Ld PDIP	E24.3
HI5813KIP	±2.5	-40 to 85	24 Ld PDIP	E24.3
HI5813JIB	±4.0	-40 to 85	24 Ld SOIC	M24.3
HI5813KIB	±2.5	-40 to 85	24 Ld SOIC	M24.3
HI5813JIJ	±4.0	-40 to 85	24 Ld CERDIP	F24.3
HI5813KIJ	±2.5	-40 to 85	24 Ld CERDIP	F24.3

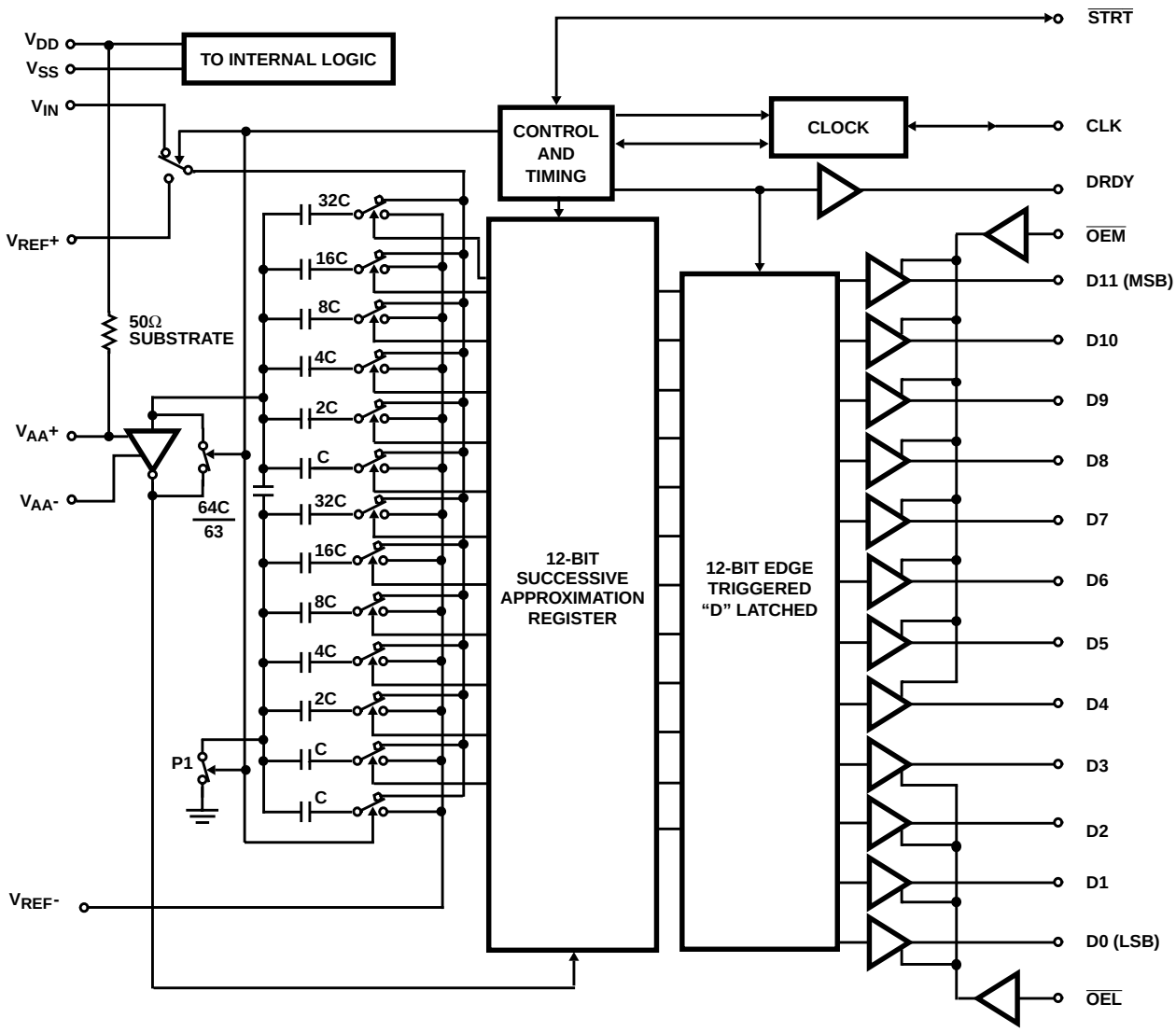
Pinout

HI5813 (PDIP, CERDIP, SOIC)
TOP VIEW



File Number **3634.1**

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage
- V_{DD} to V_{SS} . . . . . (V_{SS} -0.5V) < V_{DD} < +6.5V
- V_{AA}+ to V_{AA}- . . . . . (V_{SS} -0.5V) to (V_{SS} +6.5V)
- V_{AA}+ to V_{DD} . . . . . ±0.3V

Analog and Reference Inputs
- V_{IN}, V_{REF}+, V_{REF}- . . . . . (V_{SS} -0.3V) < V_{INA} < (V_{DD} +0.3V)

Digital I/O Pins . . . . . (V_{SS} -0.3V) < VI/O < (V_{DD} +0.3V)

Operating Conditions

Temperature Range
- PDIP, SOIC, and CERDIP Packages . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	80	N/A
SOIC Package	75	N/A
CERDIP Package	60	12

Maximum Junction Temperature
- PDIP and SOIC Packages . . . . . 150°C
- CERDIP Package . . . . . 175°C

Maximum Storage Temperature Range . . . . . -65°C to 150°C

Maximum Lead Temperature (Soldering, 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{DD} = V_{AA}+ = V_{REF}+ = 3.3V, V_{SS} = V_{AA}- = V_{REF}- = GND, CLK = 600kHz (J suffix), CLK = 500kHz (K suffix), Unless Otherwise Specified

PARAMETER		TEST CONDITIONS	25°C			-40°C TO 85°C		UNITS
			MIN	TYP	MAX	MIN	MAX	
ACCURACY								
Resolution			12	-	-	12	-	Bits
Integral Linearity Error, INL (End Point)	J		-	-	±4.0	-	±4.0	LSB
	K		-	-	±2.5	-	±2.5	LSB
Differential Linearity Error, DNL	J		-	-	±4.0	-	±4.0	LSB
	K		-	-	±2.0	-	±2.0	LSB
Gain Error, FSE (Adjustable to Zero)	J		-	-	±2.0	-	±2.0	LSB
	K		-	-	±2.0	-	±2.0	LSB
Offset Error, V_{OS} (Adjustable to Zero)	J		-	-	±3.0	-	±3.0	LSB
	K		-	-	±2.5	-	±2.5	LSB
DYNAMIC CHARACTERISTICS								
Signal to Noise Ratio, SINAD $\frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	J	f_S = 600kHz, f_{IN} = 1kHz	-	61.5	-	-	-	dB
	K	f_S = 500kHz, f_{IN} = 1kHz	-	63.9	-	-	-	dB
Signal to Noise Ratio, SNR $\frac{\text{RMS Signal}}{\text{RMS Noise}}$	J	f_S = 600kHz, f_{IN} = 1kHz	-	63.2	-	-	-	dB
	K	f_S = 500kHz, f_{IN} = 1kHz	-	65.1	-	-	-	dB
Total Harmonic Distortion, THD	J	f_S = 750kHz, f_{IN} = 1kHz	-	-68.4	-	-	-	dBc
	K	f_S = 750kHz, f_{IN} = 1kHz	-	-70.8	-	-	-	dBc
Spurious Free Dynamic Range, SFDR	J	f_S = 600kHz, f_{IN} = 1kHz	-	69.0	-	-	-	dB
	K	f_S = 500kHz, f_{IN} = 1kHz	-	71.8	-	-	-	dB
ANALOG INPUT								
Input Current, Dynamic		At V_{IN} = V_{REF}+, 0V	-	±50	±100	-	±100	µA
Input Current, Static		Conversion Stopped	-	±0.4	±10	-	±10	µA

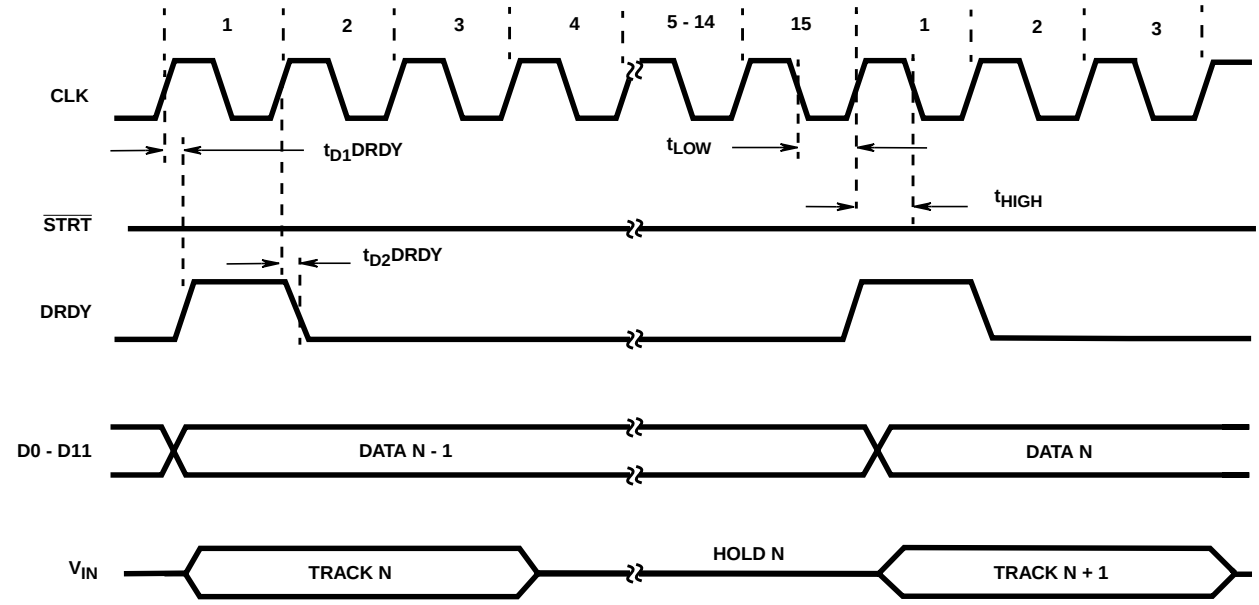
Electrical Specifications $V_{DD} = V_{AA}+ = V_{REF}+ = 3.3V$, $V_{SS} = V_{AA}- = V_{REF}- = GND$, CLK = 600kHz (J suffix), CLK = 500kHz (K suffix), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	25°C			-40°C TO 85°C		UNITS
		MIN	TYP	MAX	MIN	MAX	
Input Bandwidth -3dB		-	1		-	-	MHz
Reference Input Current		-	160	-	-	-	µA
Input Series Resistance, R_S	In Series with Input C_{SAMPLE}	-	420	-	-	-	Ω
Input Capacitance, C_{SAMPLE}	During Sample State	-	380	-	-	-	pF
Input Capacitance, C_{HOLD}	During Hold State	-	20	-	-	-	pF
DIGITAL INPUTS $\overline{OEL}$, $\overline{OEM}$, $\overline{STRT}$							
High-Level Input Voltage, V_{IH}		2.4	-	-	2.4	-	V
Low-Level Input Voltage, V_{IL}		-	-	0.8	-	0.8	V
Input Leakage Current, I_{IL}	Except CLK, V_{IN} = 0V, 5V	-	-	±10	-	±10	µA
Input Capacitance, C_{IN}		-	10		-	-	pF
DIGITAL OUTPUTS							
High-Level Output Voltage, V_{OH}	I_{SOURCE} = -400µA	2.6	-	-	2.6	-	V
Low-Level Output Voltage, V_{OL}	I_{SINK} = 1.6mA	-	-	0.4	-	0.4	V
Three-State Leakage, I_{OZ}	Except DRDY, V_{OUT} = 0V, 3.3V	-	-	±10	-	±10	µA
Output Capacitance, C_{OUT}	Except DRDY	-	20	-	-	-	pF
TIMING							
Conversion Time ($t_{CONV} + t_{ACQ}$) (Includes Acquisition Time) J		25	-	-	25	-	µs
K		30	-	-	30	-	µs
Clock Frequency	(Note 2)	0.05	-	0.75	0.05	0.75	MHz
Clock Pulse Width, t_{LOW}, t_{HIGH}	(Note 2)	100	-	-	100	-	ns
Aperture Delay, t_DAPR	(Note 2)	-	35	50	-	70	ns
Clock to Data Ready Delay, t_{D1}DRDY	(Note 2)	-	180	210	-	240	ns
Clock to Data Ready Delay, t_{D2}DRDY	(Note 2)	-	180	220	-	250	ns
Start Removal Time, $t_R\overline{STRT}$	(Note 2)	75	30	-	75	-	ns
Start Setup Time, $t_{SU}\overline{STRT}$	(Note 2)	85	60	-	30	-	ns
Start Pulse Width, $t_W\overline{STRT}$	(Note 2)	-	15	25	-	25	ns
Start to Data Ready Delay, t_{D3} DRDY	(Note 2)	-	110	130	-	160	ns
Output Enable Delay, t_{EN}	(Note 2)	-	65	75	-	80	ns
Output Disabled Delay, t_{DIS}	(Note 2)	-	95	110	-	130	ns
POWER SUPPLY CHARACTERISTICS							
Supply Current, $I_{DD} + I_{AA}$		-	0.5	1	-	2.5	mA

NOTE:

2. Parameter guaranteed by design or characterization, not production tested.

Timing Diagrams



$\overline{OEL}$ = $\overline{OEM}$ = V_{SS}

FIGURE 1. CONTINUOUS CONVERSION MODE

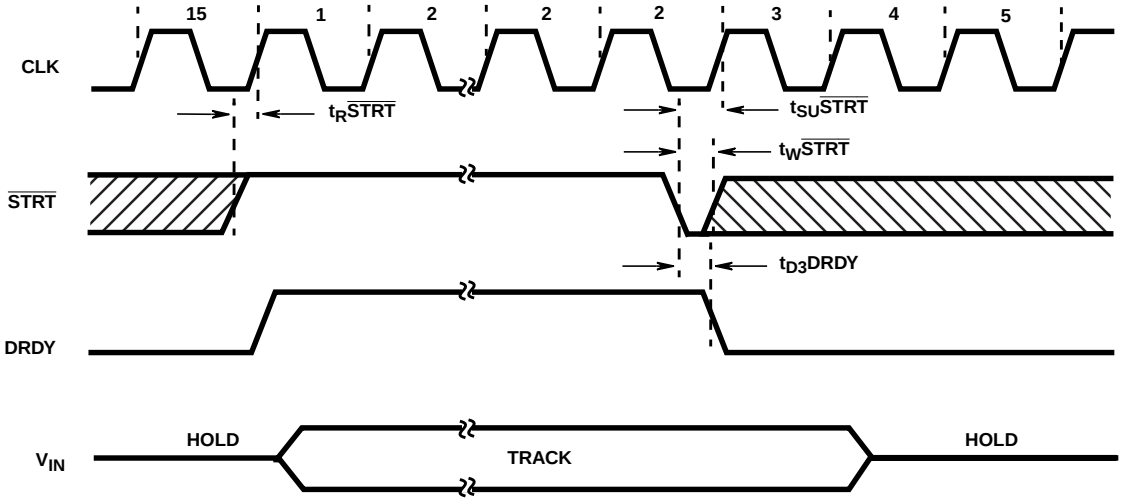


FIGURE 2. SINGLE SHOT MODE

Timing Diagrams (Continued)

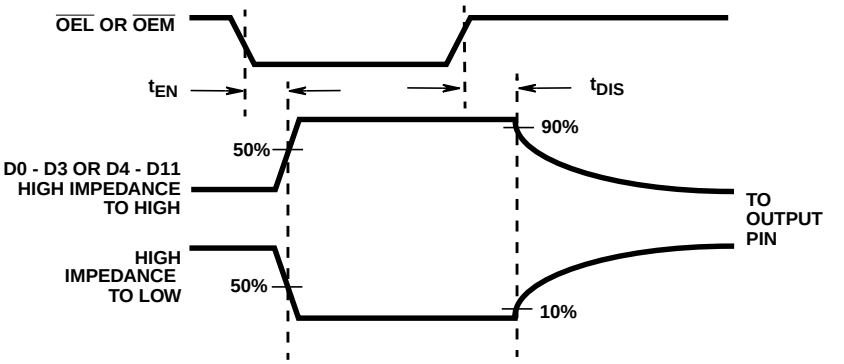


FIGURE 3A.

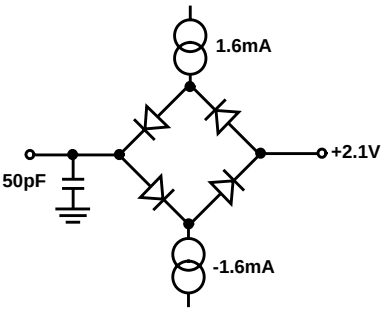


FIGURE 3B.

FIGURE 3. OUTPUT ENABLE/DISABLE TIMING DIAGRAM

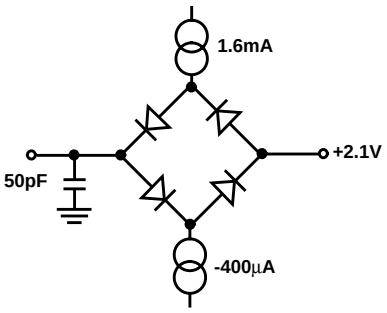


FIGURE 4. GENERAL TIMING LOAD CIRCUIT

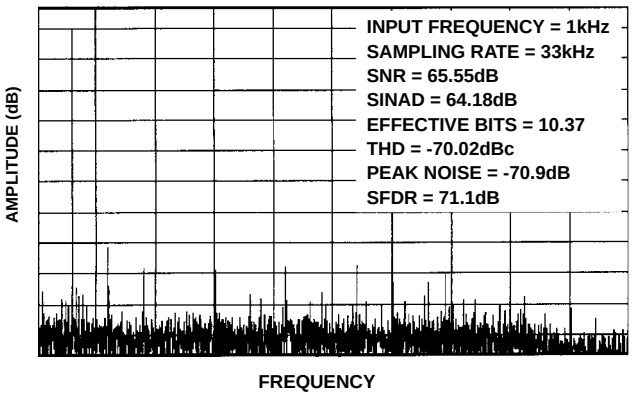


FIGURE 5. FFT SPECTRUM

Typical Performance Curves

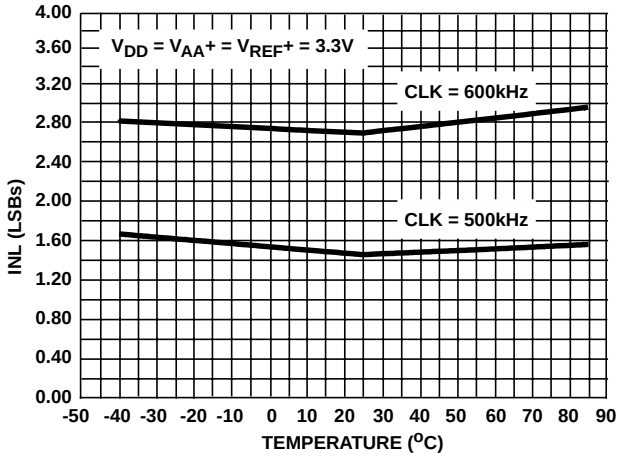


FIGURE 6. INL vs TEMPERATURE

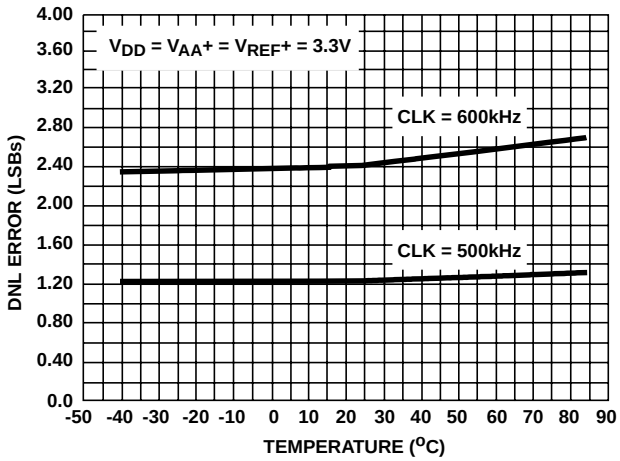


FIGURE 7. DNL vs TEMPERATURE

Typical Performance Curves

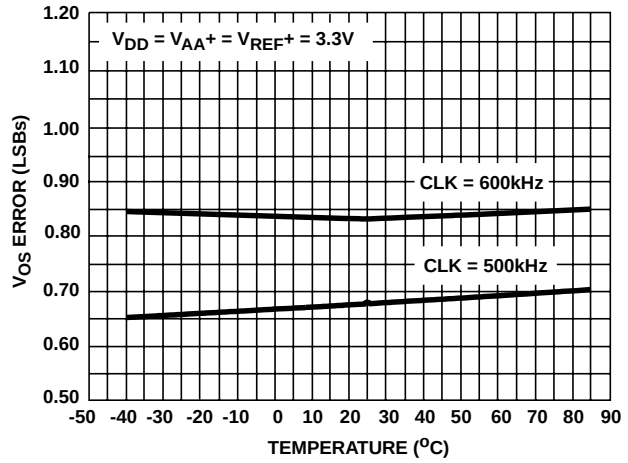


FIGURE 8. OFFSET ERROR vs TEMPERATURE

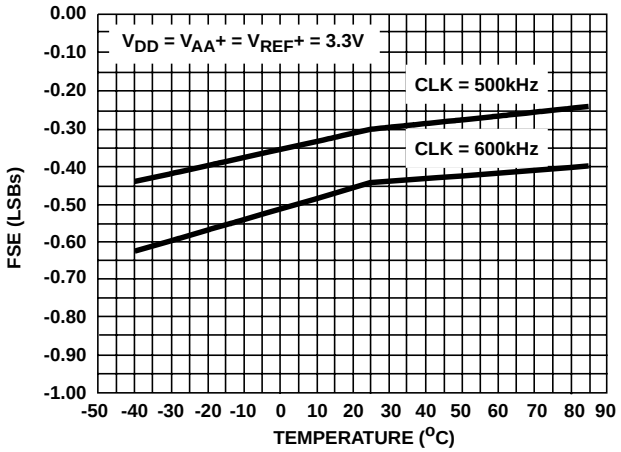


FIGURE 9. FULL SCALE ERROR vs TEMPERATURE

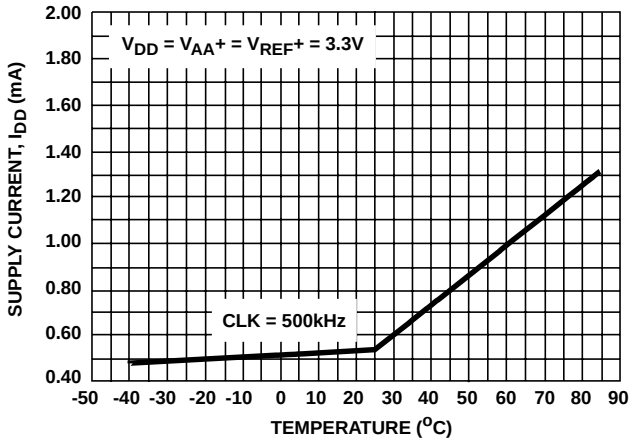


FIGURE 10. SUPPLY CURRENT vs TEMPERATURE

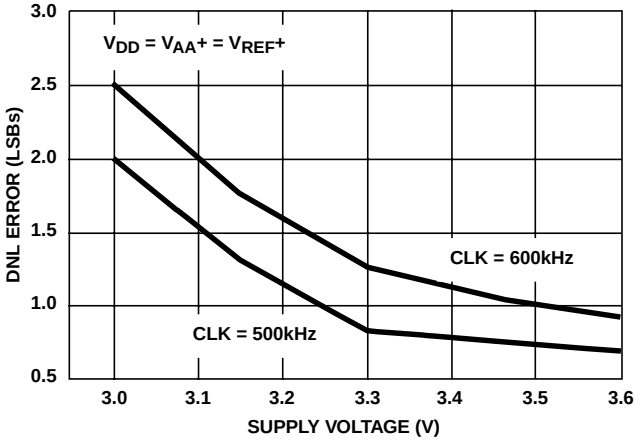


FIGURE 11. DNL vs SUPPLY VOLTAGE

Pin Descriptions

PIN #	NAME	DESCRIPTION
1	DRDY	Output flag signifying new data is available. Goes high at end of clock period 15. Goes low when new conversion is started.
2	D0	Bit 0 (Least Significant Bit, LSB).
3	D1	Bit 1.
4	D2	Bit 2.
5	D3	Bit 3.
6	D4	Bit 4.
7	D5	Bit 5.
8	D6	Bit 6.
9	D7	Bit 7.
10	D8	Bit 8.
11	D9	Bit 9.
12	V_{SS}	Digital Ground, (0V).
13	D10	Bit 10.

PIN #	NAME	DESCRIPTION
14	D11	Bit 11 (Most significant bit, MSB)
15	$\overline{OEM}$	Three-State enable for D4-D11. Active Low Input.
16	V_{AA}-	Analog Ground, (0V).
17	V_{AA}+	Analog Positive Supply. (+3.3V) (See text.)
18	V_{IN}	Analog Input.
19	V_{REF}+	Reference Voltage Positive Input, sets 4095 code end of input range.
20	V_{REF}-	Reference Voltage Negative Input, sets 0 code end of input range.
21	$\overline{STRT}$	Start Conversion Input active low, recognized after end of clock period 15.
22	CLK	CLK Input. Conversion functions are synchronized to positive going edge. (See text)
23	$\overline{OEL}$	Three-State Enable for D0 - D3. Active low input.
24	V_{DD}	Digital Positive Supply (+3.3V).

Theory of Operation

HI5813 is a CMOS 12-Bit, Analog-to-Digital Converter that uses capacitor charge balancing to successively approximate the analog input. A binary weighted capacitor network forms the A/D heart of the device. See the block diagram for the HI5813.

The capacitor network has a common node which is connected to a comparator. The second terminal of each capacitor is individually switchable to the input, $V_{REF}+$ or $V_{REF}-$.

During the first three clock periods of a conversion cycle, the switchable end of every capacitor is connected to the input and the comparator is being auto balanced at the capacitor common node.

During the fourth period, all capacitors are disconnected from the input; the one representing the MSB (D11) is connected to the $V_{REF}+$ terminal; and the remaining capacitors to $V_{REF}-$. The capacitor common node, after the charges balance out, will indicate whether the input was above $^1/_2$ of ($V_{REF}+ - V_{REF}-$). At the end of the fourth period, the comparator output is stored and the MSB capacitor is either left connected to $V_{REF}+$ (if the comparator was high) or returned to $V_{REF}-$. This allows the next comparison to be at either $^3/_4$ or $^1/_4$ of ($V_{REF}+ - V_{REF}-$).

At the end of periods 5 through 14, capacitors representing D10 through D1 are tested, the result stored, and each capacitor either left at $V_{REF}+$ or at $V_{REF}-$.

At the end of the 15th period, when the LSB (D0) capacitor is tested, (D0) and all the previous results are shifted to the output registers and drivers. The capacitors are reconnected to the input, the comparator returns to the balance state, and the data ready output goes active. The conversion cycle is now complete.

Analog Input

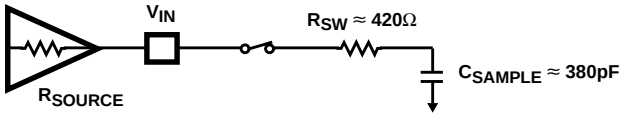
The analog input pin is a predominately capacitive load that changes between the track and hold periods of the conversion cycle. During hold, clock period 4 through 15, the input loading is leakage and stray capacitance, typically less than 5µA and 20pF.

At the start of input tracking, clock period 1, some charge is dumped back to the input pin. The input source must have low enough impedance to dissipate the current spike by the end of the tracking period. The amount of charge is dependent on supply and input voltages. The average current is also proportional to clock frequency.

As long as these current spikes settle completely by end of the signal acquisition period, converter accuracy will be preserved. The analog input is tracked for 3 clock cycles. With a clock of 500kHz the track period is 6µs.

A simplified analog input model is presented in Figure 12. During tracking, the A/D input (V_{IN}) typically appears as a 380pF capacitor being charged through a 420Ω internal switch resistance. The time constant is 160ns. To charge this capacitor from an external "zero Ω" source to 0.5 LSB (1/8192), the charging time must be at least 9 time constants or 1.4µs. The maximum source impedance (R_{SOURCE} Max) for a 6µs acquisition time settling to within 0.5 LSB is 1.3kΩ.

If the clock frequency was slower, or the converter was not restarted immediately (causing a longer sample time), a higher source impedance could be tolerated.



$$R_{SOURCE\ (MAX)} = \frac{-t_{ACQ}}{C_{SAMPLE} \ln [2^{-(N+1)}]} - R_{SW}$$

FIGURE 12. ANALOG INPUT MODEL IN TRACK MODE

Reference Input

The reference input $V_{REF}+$ should be driven from a low impedance source and be well decoupled.

Current spikes are generated on the reference pin during each bit test of the successive approximation part of the conversion cycle as the charge balancing capacitors are switched between $V_{REF}-$ and $V_{REF}+$ (clock periods 5 - 14). These current spikes must settle completely during each bit test of the conversion to not degrade the accuracy of the converter. Therefore $V_{REF}+$ and $V_{REF}-$ should be well bypassed. Reference input $V_{REF}-$ is normally connected directly to the analog ground plane. If $V_{REF}-$ is biased for nulling the converters offset it must be stable during the conversion cycle.

Full Scale and Offset Adjustment

In many applications the accuracy of the HI5813 would be sufficient without any adjustments. In applications where accuracy is of utmost importance full scale and offset errors may be adjusted to zero.

The $V_{REF}+$ and $V_{REF}-$ pins reference the two ends of the analog input range and may be used for offset and full scale adjustments. In a typical system the $V_{REF}-$ might be returned to a clean ground, and the offset adjustment done on an input amplifier. $V_{REF}+$ would then be adjusted to null out the full scale error. When this is not possible, the $V_{REF}-$ input can be adjusted to null the offset error, however, $V_{REF}-$ must be well decoupled.

Full scale and offset error can also be adjusted to zero in the signal conditioning amplifier driving the analog input (V_{IN}).

Control Signal

The HI5813 may be synchronized from an external source by using the $\overline{STRT}$ (Start Conversion) input to initiate conversion, or if $\overline{STRT}$ is tied low, may be allowed to free run. Each conversion cycle takes 15 clock periods.

The input is tracked from clock period 1 through period 3, then disconnected as the successive approximation takes place. After the start of the next period 1 (specified by t_D data), the output is updated.

The DRDY (Data Ready) status output goes high (specified by t_{D1}DRDY) after the start of clock period 1, and returns low (specified by t_{D2}DRDY) after the start of clock period 2.

The 12 data bits are available in parallel on three-state bus driver outputs. When low, the $\overline{OEM}$ input enables the most significant byte (D4 through D11) while the $\overline{OEL}$ input enables the four least significant bits (D0 - D3). t_{EN} and t_{DIS} specify the output enable and disable times.

If the output data is to be latched externally, either the trailing edge of data ready or the next falling edge of the clock after data ready goes high can be used.

Figure 2 shows operation of the HI5813 when the $\overline{STRT}$ pin is used to initate a conversion. If $\overline{STRT}$ is taken high at least $t_R\overline{STRT}$ before clock period 1 and is not reapplied during that period, the converter will stay in the track mode and the DRDY output will remain high. A low signal applied to $\overline{STRT}$ will bring the DRDY flag low and the conversion will continue with clock period 3 on the first positive going clock edge that meets the $t_{SU}\overline{STRT}$ setup time.

Clock

The clock used to drive the HI5813 can range in frequency from 50kHz up to 750kHz. All converter functions are synchronized with the rising edge of the clock signal. The clock can be shut off only during the sample (track) portion of the conversion cycle. At other times it must be above the minimum frequency shown in the specifications. In the above two cases, a further restriction applies in that the clock should not be shut off during the third sample period for more than 1ms. This might cause an internal charge pump voltage to decay.

If the clock is shut off during the conversion time (clock cycles 4 through 15) of the A/D, the output might be invalid due to balancing capacitor droop.

The clock must also meet the minimum t_{LOW} and t_{HIGH} times shown in the specifications. A violation may cause an internal miscount and invalidate the results.

Power Supplies and Grounding

V_{DD} and V_{SS} are the digital supply pins: they power all internal logic and the output drivers. Because the output drivers can cause fast current spikes in the V_{DD} and V_{SS} lines, V_{SS} should have a low impedance path to digital ground and V_{DD} should be well bypassed.

Except for V_{AA}+, which is a substrate connection to V_{DD}, all pins have protection diodes connected to V_{DD} and V_{SS}. Input transients above V_{DD} or below V_{SS} will get steered to the digital supplies.

The V_{AA}+ and V_{AA}- terminals supply the charge balancing comparator only. Because the comparator is autobalanced between conversions, it has good low frequency supply rejection. It does not reject well at high frequencies however; V_{AA}- should be returned to a clean analog ground and V_{AA}+ should be RC decoupled from the digital supply as shown in Figure 13.

There is approximately 50Ω of substrate impedance between V_{DD} and V_{AA}+. This can be used, for example, as part of a low pass RC filter to attenuate switching supply noise. A 10µF capacitor from V_{AA}+ to ground would attenuate 30kHz noise by approximately 40dB. Note that back to back diodes should be placed from V_{DD} to V_{AA}+ to handle supply to capacitor turn-on or turn-off current spikes.

Dynamic Performance

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the A/D. A low distortion sine wave is applied to the input of the A/D converter. The input is sampled by the A/D and its output stored in RAM. The data is than transformed into the frequency domain with a 4096 point FFT and analyzed to evaluate the converters dynamic performance such as SNR and THD. See typical performance characteristics.

Signal-To-Noise Ratio

The signal to noise ratio (SNR) is the measured RMS signal to RMS sum of noise at a specified input and sampling frequency. The noise is the RMS sum of all except the fundamental and the first five harmonic signals. The SNR is dependent on the number of quantization levels used in the converter. The theoretical SNR for an N-bit converter with no differential or integral linearity error is: SNR = (6.02N + 1.76)dB. For an ideal 12-bit converter the SNR is 74dB. Differential and integral linearity errors will degrade SNR:

$$SNR = 10 \text{ Log } \frac{\text{Sinewave Signal Power}}{\text{Total Noise Power}}$$

Signal-To-Noise + Distortion Ratio

SINAD is the measured RMS signal to RMS sum of noise plus harmonic power and is expressed by the following:

$$SINAD = 10 \text{ Log } \frac{\text{Sinewave Signal Power}}{\text{Noise + Harmonic Power (2nd - 6th)}}$$

Effective Number of Bits

The effective number of bits (ENOB) is derived from the SINAD data:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Total Harmonic Distortion

The total harmonic distortion (THD) is the ratio of the RMS sum of the second through sixth harmonic components to the fundamental RMS signal for a specified input and sampling frequency.

$$THD = 10 \text{ Log} \frac{\text{Total Harmonic Power (2nd - 6th Harmonic)}}{\text{Sinewave Signal Power}}$$

Spurious-Free Dynamic Range

The spurious-free dynamic range (SFDR) is the ratio of the fundamental RMS amplitude to the rms amplitude of the next largest spur or spectral component. If the harmonics are buried in the noise floor it is the largest peak.

$$SFDR = 10 \text{ Log } \frac{\text{Sinewave Signal Power}}{\text{Highest Spurious Signal Power}}$$

TABLE 2. CODE TABLE

CODE DESCRIPTION	INPUT VOLTAGE† $V_{REF}+ = 3.3V$ $V_{REF}- = 0.0V$ (V)	DECIMAL COUNT	BINARY OUTPUT CODE MSB											LSB
			D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Full Scale (FS)	3.2992	4095	1	1	1	1	1	1	1	1	1	1	1	1
FS - 1 LSB	3.2984	4094	1	1	1	1	1	1	1	1	1	1	1	0
$^3/_4$ FS	2.4750	3072	1	1	0	0	0	0	0	0	0	0	0	0
$^1/_2$ FS	1.6500	2048	1	0	0	0	0	0	0	0	0	0	0	0
$^1/_4$ FS	0.8250	1024	0	1	0	0	0	0	0	0	0	0	0	0
1 LSB	0.00080566	1	0	0	0	0	0	0	0	0	0	0	0	1
Zero	0	0	0	0	0	0	0	0	0	0	0	0	0	0

†The voltages listed above represent the ideal lower transition of each output code shown as a function of the reference voltage.

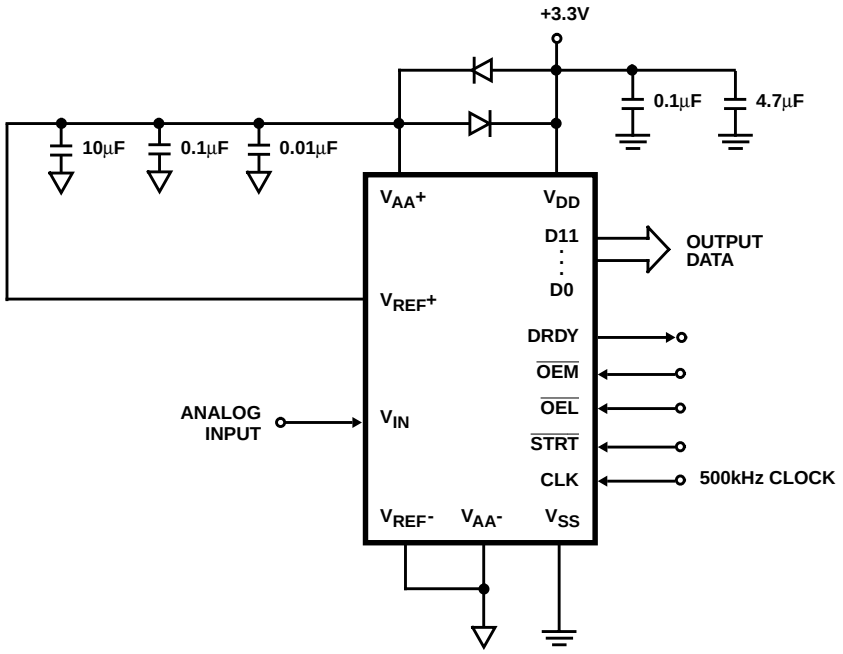


FIGURE 13. GROUND AND SUPPLY DECOUPLING

Die Characteristics

DIE DIMENSIONS:

3200µm x 3940µm

METALLIZATION:

Type: AlSi
Thickness: 11kÅ ±1kÅ

PASSIVATION:

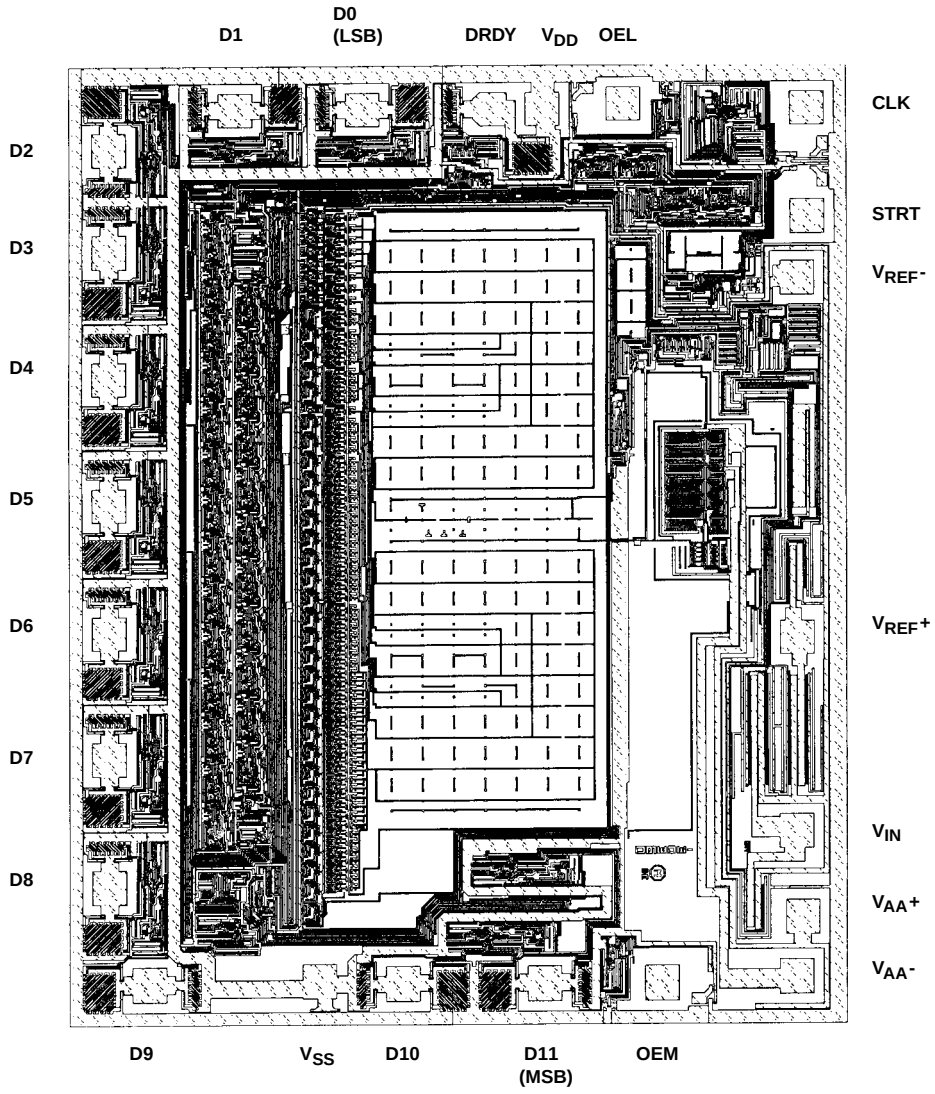
Type: PSG
Thickness: 13kÅ ±2.5kÅ

WORST CASE CURRENT DENSITY:

1.84×10^5 A/cm^2

Metallization Mask Layout

HI5813



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.