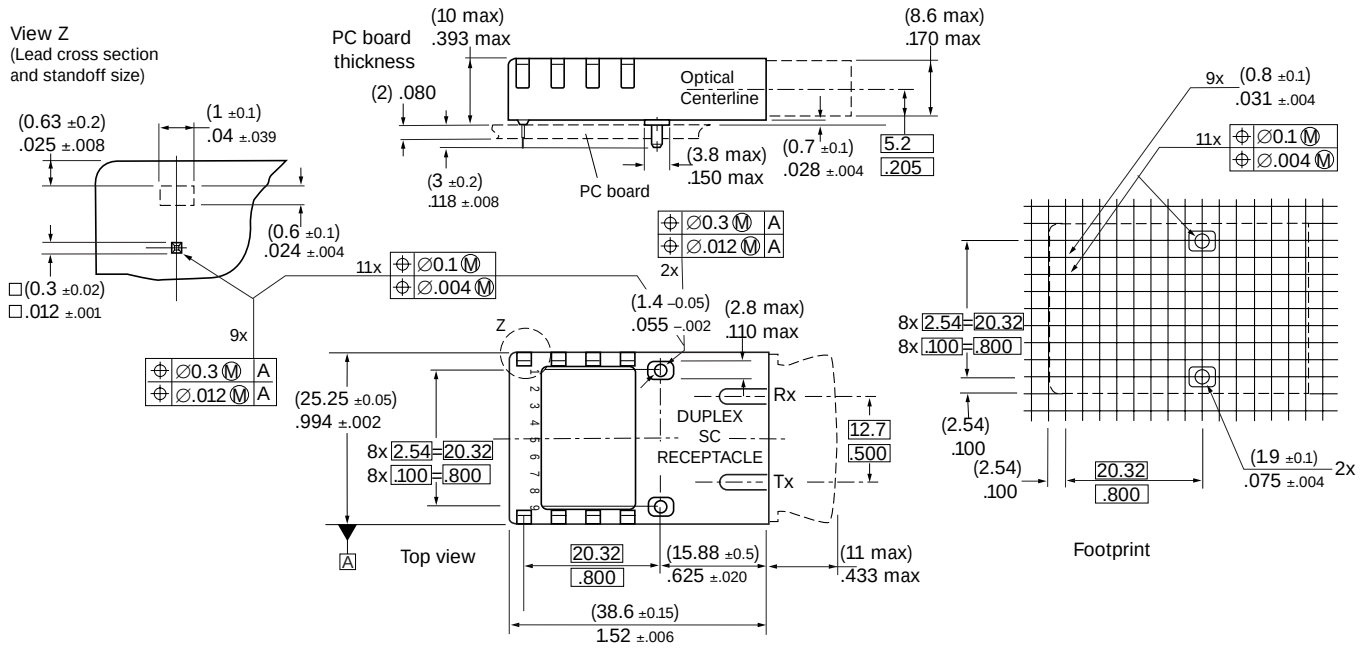
SIEMENS

V23809-F7-C10

Multimode 1300 nm LED Fibre Channel 266 MBd Transceiver*

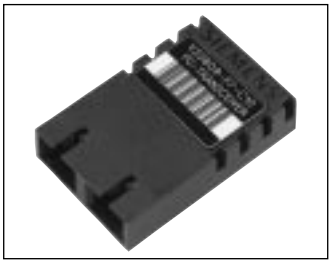
Dimensions in (mm) inches



FEATURES

- **Fully compliant with all major standards**
- **Compact integrated transceiver unit with duplex SC receptacle**
- **Single power supply with 3.0 V to 5.5 V range**
- **Extremely low power consumption < 0.7 W at 3.3 V**
- **PECL differential inputs and outputs**
- **System is optimized for 62.5/50 µm graded index fiber**
- **Industry standard multisource footprint**
- **Very low profile for high slot density**
- **Process plug included**
- **Wave solderable and washable with process plug inserted**
- **Testboard available**
- **UL-94 V-0 certified**

* Available also as FC 133 MBd V23809-B7-C10 on request



APPLICATIONS

- **FC fabric point-to-point links**
- **HIPPI, SCSI, IPI**
- **High speed computer links**
- **Local area networks up to 320 MBd**
- **High definition digital television**
- **Switching systems**

Absolute Maximum Ratings

Exceeding any one of these values may destroy the device immediately.

Supply Voltage (V_{CC}–V_{EE})	–0.5 to 7 V
Data Input Levels (PECL) (V_{IN})	V_{EE} to V_{CC}
Differential Data Input Voltage (ΔV_{IN})	3.0 V
Operating Ambient Temperature (T_{AMB})	0°C to 85°C
Storage Ambient Temperature (T_{STG})	–40°C to 85°C
Humidity/Temperature Test Condition (R_H)	85%/85°C
Soldering Conditions, Temp/Time (T_{SOLD}/t_{SOLD}) (MIL-STD 883C, Method 2003)	270°C/10 s
ESD Resistance (all pins to V_{EE}, human body)	1.5 kV
Output Current (I_O)	50 mA

DESCRIPTION

This data sheet describes the Siemens Fibre Channel transceiver, which belongs to the Siemens Multistandard Transceiver Family. It is fully compliant with the Fibre Channel FC-133 MBaud and FC-266 MBaud draft standard.

Fibre Channel provides a general transport for upper layer protocols such as Intelligent Peripheral Interface (IPI), High Performance Parallel Interface (HIPPI) and Small Computer System Interface (SCSI) command sets. Defined transmission rates are 266 MBaud and 133 MBaud in point-to-point or fabric topology.

The Siemens low cost multistandard transceiver is a single unit comprised of a transmitter, a receiver, and an SC receptacle. This design frees the customer from many alignment and PC board layout concerns. The modules are designed for low cost applications.

The inputs/outputs are PECL compatible, and the unit operates from a 3.0 V to 5.5 V power supply. As an option, the data output stages can be switched to static levels during absence of light as indicated by the Signal Detect function. It can be directly interfaced with available chipsets.

Regulatory Compliance

Feature	Standard	Comments
Electromagnetic Interference (EMI)	FCC Class B EN 55022 Class B CISPR 22	Noise frequency range:30 MHz to 1 GHz
Immunity: Electrostatic Discharge	EN 61000-4-2 IEC 1000-4-2	Discharges of ± 15kV with an air discharge probe on the receptacle cause no damage.
Immunity: Radio Frequency Electromagnetic Field	EN 61000-4-3 IEC 1000-4-3	With a field strength of 10 V/m rms, noise frequency ranges from 10 MHz to 1 GHz
Eye Safety	IEC 825-1	Class 1

TECHNICAL DATA

The electro-optical characteristics described in the following tables are valid only for use under the recommended operating conditions.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Ambient Temperature	T_{AMB}	0		70	°C
Power Supply Voltage	$V_{CC}–V_{EE}$	3		5.5	V
Supply Current 3.3 V	I_{CC}			230	mA
Supply Current 5 V(1)				260	
Transmitter					
Data Input High Voltage	$V_{IH}–V_{CC}$	–1165		–880	mV
Data Input Low Voltage	$V_{IL}–V_{CC}$	–1810		–1475	
Threshold Voltage	$V_{BB}–V_{CC}$	–1380		–1260	
Input Data Rise/Fall Time, 20%–80%	t_R, t_F	0.4		1.3	ns
Data High Time(2)	t_{ON}			1000	
Receiver					
Output Current	I_O			25	mA
Input Duty Cycle Distortion	t_{DCD}			1	ns
Input Data Dependent Jitter	t_{DDJ}			1	
Input Random Jitter	t_{RJ}			0.76	
Input Center Wavelength	λ_C	1260		1380	nm
Electrical Output Load(3)	R_L		50		Ω

Notes

1. For $V_{CC}–V_{EE}$ (min., max.). 50% duty cycle. The supply current ($I_{CC2}+I_{CC3}$) does not include the load drive current (I_{CC1}). Add max. 45 mA for the three outputs. Load is 50 Ω to $V_{CC}–2$ V.
2. To maintain good LED reliability, the device should not be held in the ON state for more than the specified time. Normal operation should be done with 50% duty cycle.
3. To achieve proper PECL output levels the 50 Ω termination should be done to $V_{CC}–2$ V. For proper termination see the application notes.

Transmitter Electro-Optical Characteristics

(Values in brackets are for 320 MBd)

Transmitter	Symbol	Min.	Typ.	Max.	Units
Data Rate	DR	0		266 (320)	mBaud
Launched Power (Average)(1, 2) into 62.5 μm Fiber	P_O	–20 (–21)	–16 (–17)	–14	dBm
Center Wavelength(2, 3)	λ_C	1280		1380	nm
Spectral Width (FWHM)(2, 4)	Δ_λ			200	
Output Rise Time, 10%–90%(5)	t_R	0.6		2.0 (2.5)	ns
Output Rise Time, 10%–90%(5)	t_F			2.2 (2.5)	
Temperature Coefficient of Optical Output Power	TCp			.03	dB/°C
Extinction Ratio (Dynamic)(2, 6)	ER			12	%
Deterministic Jitter(7, 8)	t_{DJ}			16	
Random Jitter(7, 9)	t_{RJ}			9	

Notes

1. Measured at the end of 5 meters of 62.5/125/0.275 graded index fiber using calibrated power meter and a precision test ferrule. Cladding modes are removed. Values valid for EOL.
2. The input data pattern is a 12.5 MHz square wave pattern.
3. Center wavelength is defined as the midpoint between the two 50% levels of the optical spectrum of the LED.
4. Spectral width (full width, half max.) is defined as the difference between 50% levels of the optical spectrum of the LED.
5. 10% to 90% levels. Measured using a 12.5 MHz square wave pattern with an optoelectronic measurement system (detector and oscilloscope) with 3 dB bandwidth ranging from less than 0.1 MHz to more than 750 MHz.
6. Extinction ratio is defined as PL/PH x 100%. Measurement system as in Note 5.
7. Test method and consideration as in FC-PH Appendix A.
8. Measured with the K28.5 pattern from Chapter II of the FC-PH at 266MBd.
9. Measured with the K28.7 pattern from Chapter II of the FC-PH which equals a 133 MHz square wave.

Receiver Electro-Optical Characteristics

(Values in brackets are for 320 MBd)

Receiver	Symbol	Min.	Typ.	Max.	Units
Data Rate	DR	5		266 (320)	mBaud
Sensitivity (Average Power)(1)	P_{IN}		–30	–26	dBm
Saturation (Average Power)(2)	P_{SAT}	–14	–11		
Deterministic Jitter(3, 4)	t_{DJ}			19	%
Random Jitter(3, 5)	t_{RJ}			9	
Signal Detect Assert Level(6)	P_{SDA}	–43.5		–29	dBm
Signal Detect Deassert Level(7)	P_{SDD}	–45		–30.5	
Signal Detect Hysteresis	P_{SDA}–P_{SDD}	1.5			dB
Output Low Voltage(8)	V_{OL}–V_{CC}	–1810		–1620	mV
Output High Voltage(8)	V_{OH}–V_{CC}	–1025		–880	
Output Data Rise/Fall Time, 20%–80%	t_R, t_F			1.3	ns
Output SD Rise/Fall Time, 20%–80%				40	

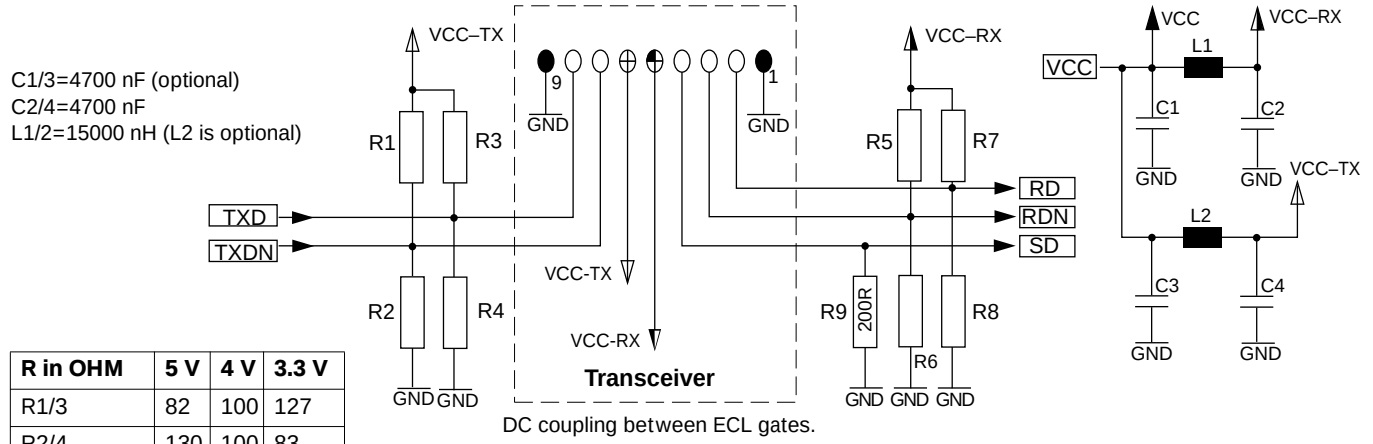
Notes

1. For a bit error rate (BER) of less than 1x10E-12 over a receiver eye opening of least 1.0ns. Measured with a 2^7–1 PRBS.
2. For a BER of less than 1x10E-12. Measured in the center of the eye opening with a 2^7–1 PRBS.
3. Test method and considerations as in FH-PC Appendix A.
4. Measured with the K28.5 pattern from Chapter II of the FC-PH at 266 MBd.
5. Measured with the K28.7 pattern from Chapter II of the FC-PH which equals a 133 MHz square wave.
6. An increase in optical power through the specified level will cause the Signal Detect output to switch from a Low state to a High state.
7. A decrease in optical power through the specified level will cause the Signal Detect output to switch from a High state to a Low state.
8. PECL compatible. Load is 50 Ω into V_{CC}–2 V. Measured under DC conditions. For dynamic measurements a tolerance of 50 mV should be added for V_{CC}=5 V.

Pin Description for 1x9 Pin Row

Pin Name		Level	Pin #	Description
RxV_{EE}	Rx Ground	Power Supply	1	Negative power supply, normally ground
RxD	Rx Output Data	PECL Output	2	Receiver output data
RxDn	Rx Output Data	PECL Output	3	Inverted receiver output data
Rx SD	RX Signal Detect	PECL Output active high	4	A high level on this output shows that an optical signal is applied to the optical input
RxV_{CC}	Rx +3.3...5 V	Power Supply	5	Positive power supply, +3.3...5 V
TxV_{CC}	Tx +3.3...5 V	Power Supply	6	Positive power supply, +3.3...5 V
TxDn	Tx Input Data	PECL Input	7	Inverted transmitter input data
TxD	Tx Input Data	PECL Input	8	Transmitter input data
TxV_{EE}	Tx Ground	Power Supply	9	Negative power supply, normally ground
Case	Support	Not Connected	S1/S2	Support stud, not connected

APPLICATION NOTE FOR 1X9 PIN ROW TRANSCEIVER



R in OHM	5 V	4 V	3.3 V
R1/3	82	100	127
R2/4	130	100	83
R5/7	82	100	127
R6/8	130	100	83

R9=200 Ohm

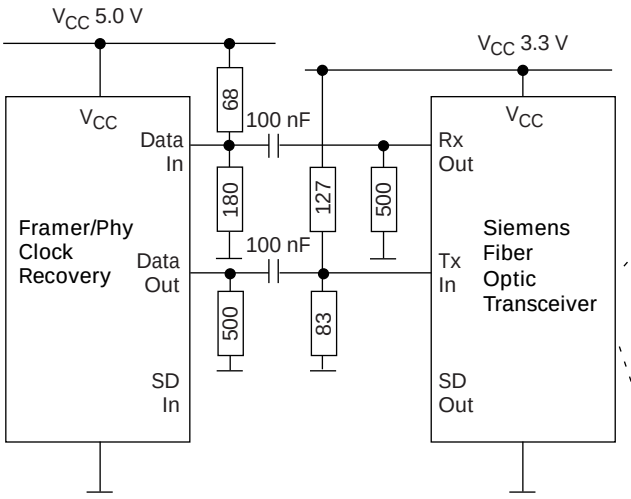
The power supply filtering is required for good EMI performance. Use short tracks from the inductor L1/L2 to the module V_{CC}–RX/V_{CC}–TX.

A GND plane under the module is recommended for good EMI and sensitivity performance.

APPLICATION NOTE FOR MULTIMODE 1300 NM LED TRANSCEIVER

Solutions for connecting a Siemens 3.3 V Fiber Optic Transceiver to a 5.0 V Framer-/Phy-Device.

Figure 1. Common GND



Inputs and outputs are differential and should be doubled. Signal Detect (SD) is single ended (if used).

Figure 1a. Circuitry for SD (Differential) and Common GND

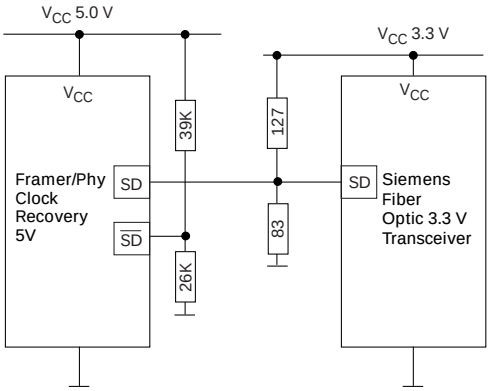


Figure 1b. Circuitry for SD (Single Ended) and Common GND

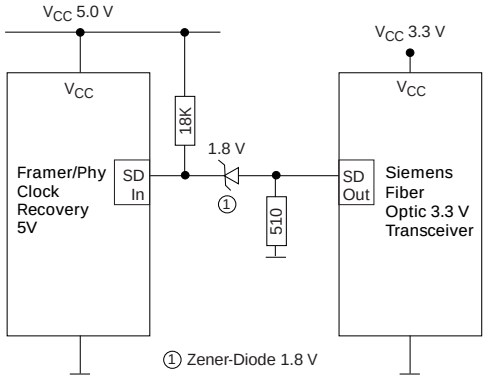


Figure 2. Common V_{CC}

Inputs and outputs are differential and should be doubled. Signal Detect (SD) is single ended.