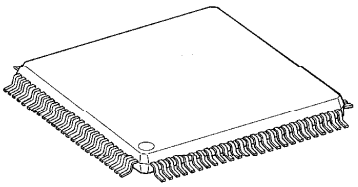
TENTATIVE TOSHIBA CCD AREA IMAGE SENSOR CCD(Charge Coupled Device)

TC6335AF

TCD5460AC, TCD5470AC, TCD5580C DRIVING PULSE GENERATOR IC

The CMOS LSI of TC6335AF was developed to drive the TCD5460AC, TCD5470AC, TCD5580C, TCD5700D, TCD5710D can be combined with a vertical clock driver to constitute the CCD area image sensor driving circuit.



LQFP100-P-1414-0.50B

Weight : 0.35g (Typ.)

FEATURES

- Generation of all timing pulses required to drive TCD5460AC, TCD5470AC, TCD5580C, TCD5700D, TCD5710D.
- Correspondence with electronic shutter from 1 / 25, to 1 / 10000 s.
- Generation of sampling pulses for CDS signal processing.
- High resolution function
- Adjustment of phase of reset pulse and sampling pulses

MAXIMUM RATINGS (V_{SS} = 0V)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	−0.3~7.0	V
Input Voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Input Current	I_{IN}	± 10	mA
Storage Temperature	T_{stg}	−40~125	°C

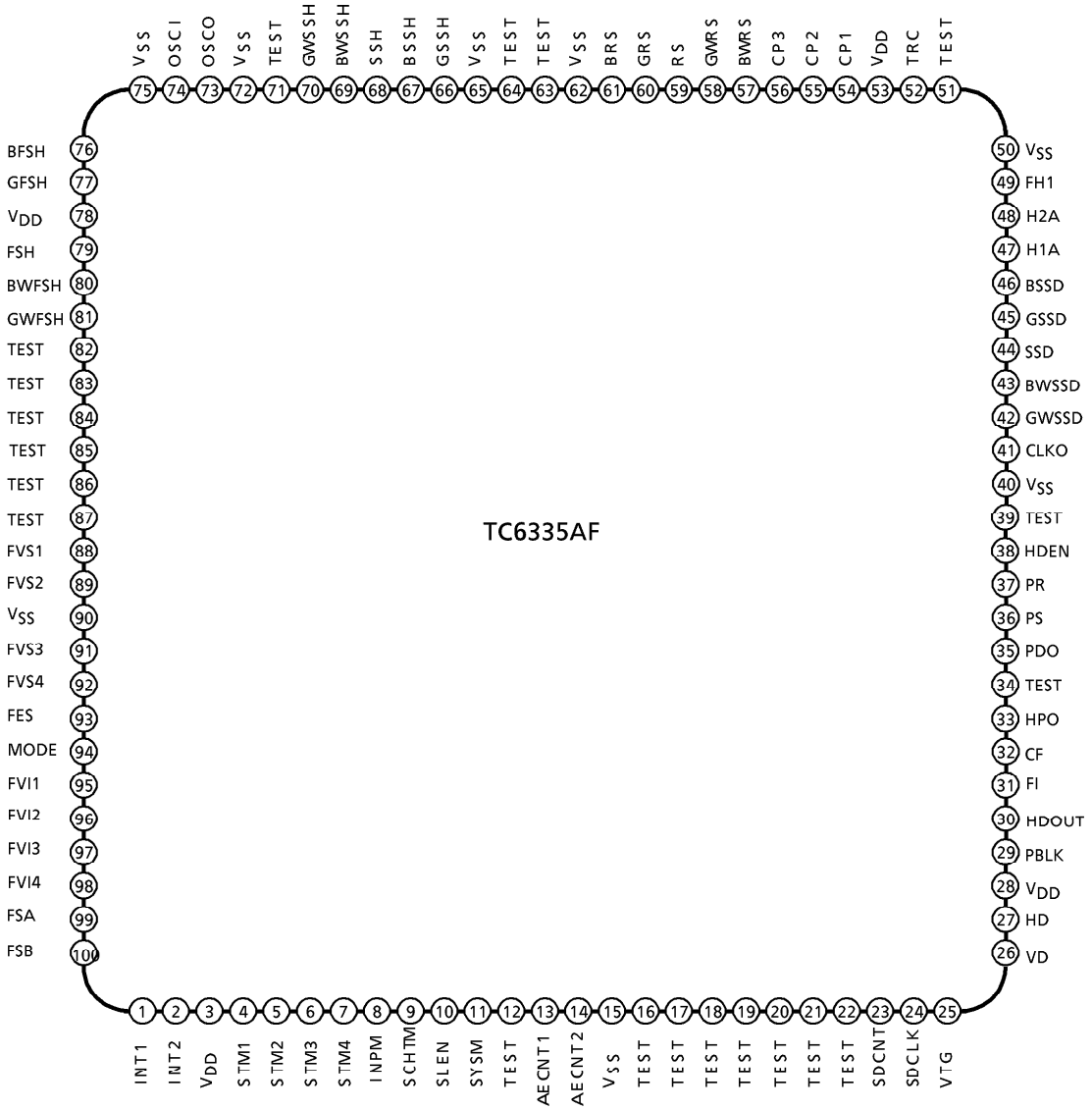
RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	4.75~5.25	V
Operating Temperature	T_{opr}	−20~70	°C

ELECTRICAL CHARACTERISTICS (V_{SS} = 0V, V_{DD} = 4.75~5.25V, Ta = 0~70°C)

CHARACTERISTIC		SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Voltage	"H" Level	V_{IH}		3.5	—	—	V
	"L" Level	V_{IL}		—	—	1.5	
Input Current	"H" Level	I_{IH}	$V_{IN} = V_{DD}$	– 10	—	10	μA
			$V_{IN} = V_{DD}$, (included PULL-DOWN)	10	—	200	
	"L" Level	I_{IL}	$V_{IN} = V_{SS}$	– 10	—	10	
			$V_{IN} = V_{SS}$, (included PULL-UP)	– 200	—	– 10	
Output Voltage	"H" Level	V_{OH}	I_{OH} = – 16mA, H1A, H2A, RS	2.4	—	—	V
			I_{OH} = – 4mA except H1A, H2A				
	"L" Level	V_{OL}	I_{OL} = 16mA, H1A, H2A, RS	—	—	0.4	
			I_{OL} = 4mA except H1A, H2A				
Static Consumption Current		I_{DD}	C_L = 0pF, V_{DD} = 5V, Ta = 25°C	—	—	200	μA

PIN CONNECTION



PIN FUNCTION

<table>
<tr><th>PIN No.</th><th>SYMBOL</th><th>I / O</th><th>POLARITY</th><th>FUNCTION</th></tr>
<tr><td>1
2</td><td>INT1
INT2</td><td>I</td><td>PULL DOWN</td><td>Input terminal for switching storage mode.
<table>
<tr><th>INT1</th><th>INT2</th><th>FIT Mode</th><th>IT Mode</th></tr>
<tr><td>L</td><td>L</td><td colspan="2">Field storage mode</td></tr>
<tr><td>H</td><td>L</td><td>High resolution</td><td>—</td></tr>
<tr><td>L</td><td>H</td><td>—</td><td>—</td></tr>
<tr><td>H</td><td>H</td><td colspan="2">Frame storage mode</td></tr>
</table></td></tr>
<tr><td>3</td><td>V_{DD}</td><td>—</td><td></td><td>Connected to power supply 5.0V ± 0.25V</td></tr>
<tr><td>4
5
6
7</td><td>STM1
STM2
STM3
STM4</td><td>I</td><td>PULL DOWN</td><td>Shutter period setting terminal.
(See the attached table for the shutter period)</td></tr>
<tr><td>8</td><td>INPM</td><td>I</td><td>PULL DOWN</td><td>Input terminal for switching shutter speed setting mode.
- parallel input mode in "L" level
- serial input mode in "H" level</td></tr>
<tr><td>9</td><td>SCHTM</td><td>I</td><td>PULL DOWN</td><td>Input terminal for switching electronic shutter sweep mode.
- FIT sweep mode in "L" level
- substrate sweep mode in "H" level
* IT mode only for substrate sweep</td></tr>
<tr><td>10</td><td>SLEN</td><td>I</td><td>PULL DOWN</td><td>Input terminal for low speed electronic shutter mode.
- Desable in "L" level
- Enable in "H" level * IT mode disabled.</td></tr>
<tr><td>11</td><td>SYSM</td><td>I</td><td>PULL DOWN</td><td>Input terminal for switching TV system.
- NTSC mode in "L" level
- PAL mode in "H" level</td></tr>
<tr><td>12</td><td>TEST</td><td>—</td><td>PULL DOWN</td><td>Test terminal (open for normal use)</td></tr>
<tr><td>13
14</td><td>AECNT1
AECNT2</td><td>I</td><td>PULL DOWN</td><td>Input terminal for controlling AECNT mode and electronic shutter speed. * IT mode disabled.</td></tr>
<tr><td>15</td><td>V_{SS}</td><td>—</td><td></td><td>GND</td></tr>
<tr><td>16
17
18
19
20</td><td>TEST</td><td>O</td><td></td><td>Test terminal (open for normal use)</td></tr>
<tr><td>21
22</td><td>TEST</td><td>I</td><td>PULL DOWN</td><td>Test terminal (open for normal use)</td></tr>
</table>

PIN No.	SYMBOL	I / O	POLARITY	FUNCTION
23	SDCNT	I	PULL DOWN	Serial data control input connected to VD of synchronization generator IC.
24	SDCLK	I	PULL DOWN	Serial data clock input.
25	VTG	O		Output terminal for standard pulse of AECONT mode is opened for normal use.
26	VD	I	PULL DOWN	Input terminal for VD of synchronization generator IC.
27	HD	I	PULL DOWN	Input terminal for HD of synchronization generator IC.
28	V_{DD}	—		Connected to power supply 5.0 ± 0.25V
29	PBLK	O		Pre-blanking pulse output. "H" level indicates the erase period.
30	HDOUT	O		Horizontal drive pulse is output when 1H divider works (HDEN : "H" level).
31	FI	O		Field index output (H:0dd field / L:Even field)
32	CF	O		Color field pulse output for field
33	HPO	O		Horizontal transfer control pulse. This pulse is output within horizontal flyback time to indicate that horizontal CCD transfer period stops.
34	TEST	I	PULL DOWN	Test terminal (open for normal use)
35	PDO	O		Output terminal for phase comparator.
36	PS	I	PULL DOWN	Input terminal for phase comparator.
37	PR	I	PULL DOWN	Input terminal for phase comparator.
38	HDEN	I	PULL DOWN	Input terminal for controlling 1H divider. - stop working in "L" level - working in "H" level
39	TEST	—	PULL DOWN	Test terminal (open for normal use)
40	V_{SS}	—		GND
41	CLKO	O		Master clock output for synchronization generator IC.
42	GWSSD	I		Input and output terminal for adjusting SSD width. The BWSSD output is delayed with a capacitor and resistor connected to the GWSSD.
43	BWSSD	O		
44	SSD	O		Signal sampling delay pulse output.
45	GSSD	I		Input and output terminal for adjusting SSD phase. The BSSD output is delayed with a capacitor and resistor connected to the GSSD.
46	BSSD	O		
47	H1A	O		Horizontal CCD drive pulse to be connected to the H1A and H2A gate of the CCD image sensor.
48	H2A	O		
49	FH1	O		Horizontal CCD drive pulse to be connected to the H1B gate of the CCD image sensor.

PIN No.	SYMBOL	I / O	POLARITY	FUNCTION
50	V_{SS}	—		GND
51	TEST	I	PULL DOWN	Test terminal (open for normal use)
52	TRC	I	PULL DOWN	IT mode drive transfer - Sweep disabled in "H" level - Sweep enabled in "L" level
53	V_{DD}	—		Connected to power supply 5.0V ± 0.25V
54	CP1	O		Clamp pulse output for signal processing. (CP1 is for OB portion of CCD signal output)
55	CP2	O		
56	CP3	O		
57	BWRS	O		Input and output terminal for adjusting RS width. The BWRS output is delayed with a capacitor and resistor connected to the GWRS.
58	GWRS	I		
59	RS	O		Reset gate pulse to be connected to the RS gate of the CCD image sensor.
60	GRS	I		Input and output terminal for adjusting RS phase. The BRS output is delayed with a capacitor and resistor connected to the GRS.
61	BRS	O		
62	V_{SS}	—		GND
63	TEST	—		Test terminal (open for normal use)
64	TEST	—		Test terminal (open for normal use)
65	V_{SS}	—		GND
66	GSSH	I		Input and output terminal for adjusting SSH phase. The BSSH output is delayed with a capacitor and resistor connected to the GSSH.
67	BSSH	O		
68	SSH	O		Signal sampling pulse output.
69	BWSSH	O		Input and output terminal for adjusting SSH width. The BWSSH output is delayed with a capacitor and resistor connected to the GWSSH.
70	GWSSH	I		
71	TEST	I	PULL DOWN	Test terminal (open for normal use)
72	V_{SS}	—		GND
73	OSCO	O		Master clock output (2fck = 45MHz)
74	OSCI	I		Master clock input (2fck = 45MHz)
75	V_{SS}	—		Connected to power supply 5.0V ± 0.25V
76	BFSH	O		Input and output terminal for adjusting FSH phase. The BFSH output is delayed with a capacitor and resistor connected to the GFSH.
77	GFSH	I		
78	V_{DD}	—		Connected to power supply 5.0 ± 0.25V
79	FSH	O		Feed through sampling pulse output

PIN No.	SYMBOL	I / O	POLARITY	FUNCTION
80	BWFSH	O		Input and output terminal for adjusting FSH width. The BWFSH output is delayed with a capacitor and resistor connected to the GWFSH.
81	GWFSH	I		
82	TEST	I	PULL DOWN	Test terminal (open for normal use)
83	TEST	I	PULL DOWN	Test terminal (open for normal use)
84	TEST	I		Test terminal (open for normal use)
85	TEST	I		Test terminal (open for normal use)
86	TEST	I		Test terminal (open for normal use)
87	TEST	I		Test terminal (open for normal use)
88	FVS1	O		Vertical CCD drive pulse ϕS1 and ϕS2 connected to the inversion type vertical clock driver.
89	FVS2	O		
90	V_{SS}	—		GND
91	FVS3	O		Vertical CCD drive pulse ϕS3 and ϕS4 connected to the inversion type vertical clock deiver.
92	FVS4	O		
93	FES	O		Electronic shutter pulse connected to the inversion type driver.
94	MODE	I	PULL DOWN	Input terminal for drive mode - Frame Interline Transfer in "L" level - Interline Transfer in "H" level
95	FVI1	O		Vertical CCD drive pulse ϕI1, ϕI2, ϕI3 and ϕI4 connected to the inversion type vertical clock driver.
96	FVI2	O		
97	FVI3	O		
98	FVI4	O		
99	FSA	O		Field shift drive pulse ϕI1 and ϕI3 connected to the inversion type vertical clock driver.
100	FSB	O		

SETTING FOR ELECTRONIC SHUTTER SPEED

INPM	Electronic shutter						Storage mode			
					Shutter speed		FIT Drive			IT Drive
	STM1	STM2	STM3	STM4	NTSC	PAL	substrate sweep	FIT sweep	high resolution	substrate sweep
L (Parallel-- input)	L	L	L	L	1/60*	1/50*	—	—	—	—
	H	L	L	L	1/100	1/60	○	○	○	○
	L	H	L	L	1/120		○	○	○	○
	H	H	L	L	1/250		○	○	○	○
	L	L	H	L	1/500		○	○	○	○
	H	L	H	L	1/1000		○	○	○	○
	L	H	H	L	1/2000		○	○	×	○
	H	H	H	L	1/4000		○	×	×	○
	L	L	L	H	1/8000		○	×	×	○
	H	L	L	H	1/10000		○	×	×	○
	L	H	L	H	1/62**	1/52**	○	○	○	○
	H	H	H	H	AECNT mode Timing pulse on AECNT1 and AECNT2 controls shutter speed. (AECNT1 only during IT drive.)					
H serial output	Serial binary data on SDCLK and STM4 can set the shutter speed in 1H (partially in 1.5H).						○	○	○	○

○ available
× disable

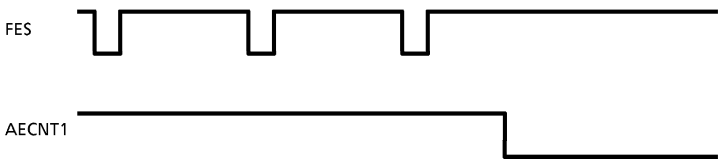
* Normal mode when electronic shutter mode is disable. On frame storage mode storage speed is fixed to 1/30 s in NTSC mode (1/25 s in PAL mode).
** Normal mode when electronic shutter mode is available.

AECNT MODE

In this mode timing pulse on AECNT1 and AECNT2 can control the shutter speed.

- AECNT1: Input on AECNT1 controls FES pulse. The available range of setting the substrate shutter is until 1/10000 s.

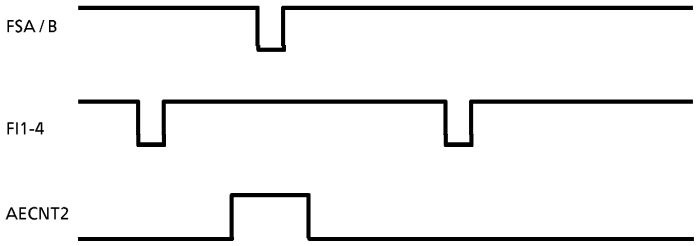
AECNT1	FES
H	Generating
L	Stoping



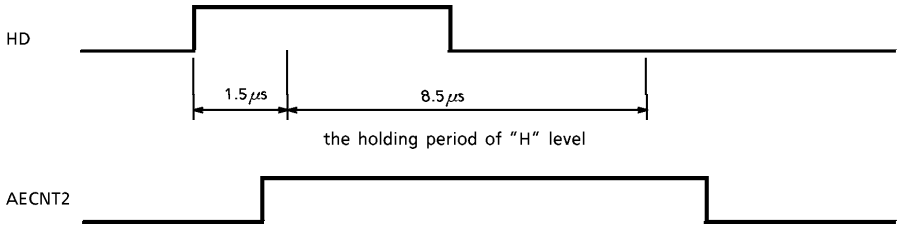
AECNT1 is not allowed to change while FES pulse is "L" level. Because AECNT1 gates FES pulse.

- AECNT2: Input on AECNT2 controls FSA and FSB pulses (FIT shutter).

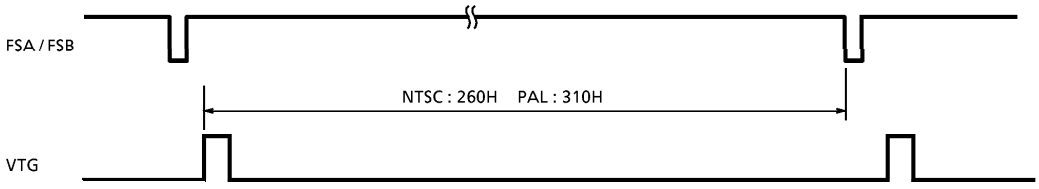
AECNT2	FSA / FSB, FI1~4
H	Field shift
L	Line shift



The period of "H" level on AECNT2 should be longer than the holding period of "H" level as follows. AECNT2 is not allowed to change 9H before FSA / B and 10H after FSA / B.

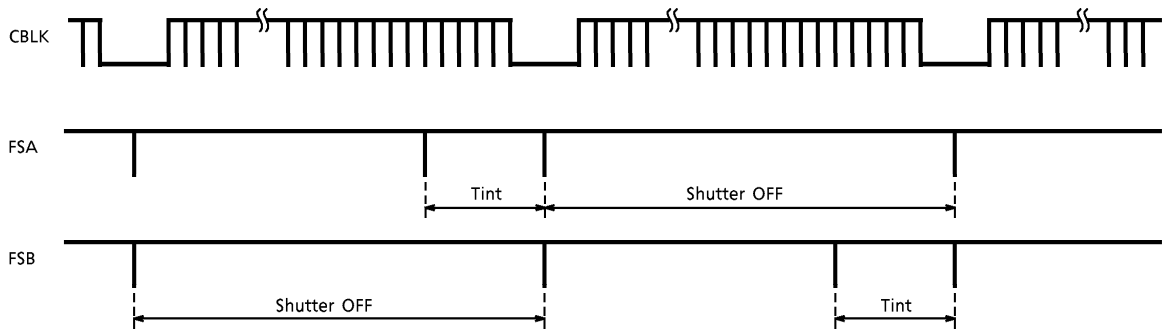


On AECNT mode, generation of trigger pulse needs external counter circuits. And VTG pulse is used for the standard pulse resetting the external counter circuits. The time difference of VTG and field shift (shutter OFF) in the next field are set as follows;



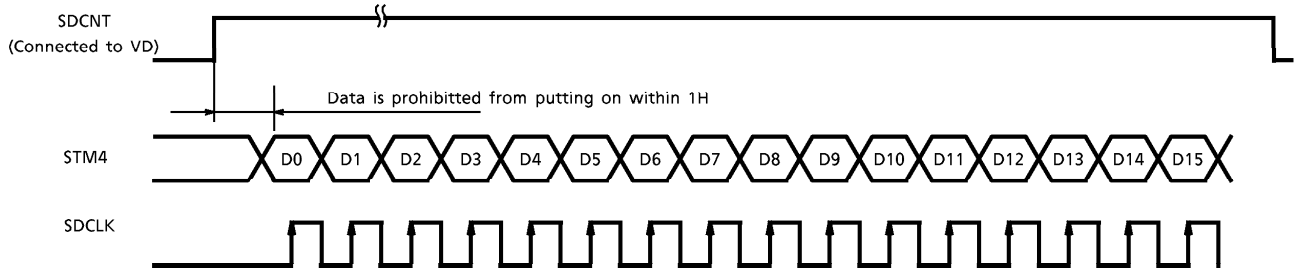
- **HIGH RESOLUTION MODE** (Only during FIT drive)

  The high resolution mode uses the FIT shutter to add read the accumulation time that differs from the accumulation time of the two add read pixels. This improves the perpendicular resolution from the normal add read. This mode maintains the accumulation time of one pixel (shutter OFF accumulation) and accumulates the set shutter time and add reads this for the other pixel.



SERIAL SETTING MODE

INPM : "H" level
STM4 : Serial data must be put in when VD is "H" level.
SDCLK : Clock for serial data
SDCNT : Serial data control connected to VD of synchronization generator IC.



SDCNT is connected to VD of synchronization generator IC.
Data is prohibitted from putting on within 1H after VD pulse raises. The data set on STM4 is fed into shutter speed controller when SDCLK pulse raises. The data is organizad 16 bits.

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
0	SS0	S0	S1	S2	S3	S4	S5	S6	S7	S8	S9	×			
Put "0" on D0	9 bits binary data put on S0 – 8 can set the shutter speed in 1H. And the data on SS0 can set the shutter speed in 0.5H below 10H on NTSC mode or 14H on PAL mode.											Not concerned			

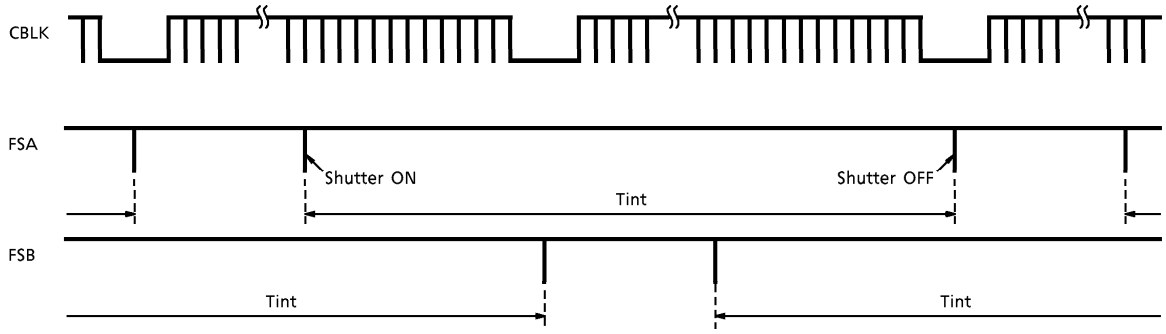
TC6317AF has shift resistor (clock : SDCLK). When data above 16 bits puts on, last 16 bits is available. Input on SDCNT always connect to VD.

Allowance range of input shows as follows.

System	Storage Mode			
	FIT Mode			IT Mode
	Substrate shutter	FIT shutter	High resolution	Substrate shutter
NTSC	1H~256H	11H~256H	11H~256H	1H~256H
PAL	1H~306H	11H~306H	11H~306H	1H~306H

LOW SPEED SHUTTER MODE (FIT

Low speed shutter mode (1/60~1/30 s) is available when "H" level inputs on SLEN. A setting mode is only serial setting mode. Former setting methods (serial setting mode) are applied to this mode. High resolution mode and substrate shutter mode is disable on this mode.



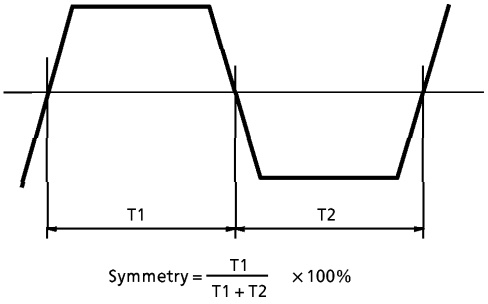
Allowance range of input shows as follows;

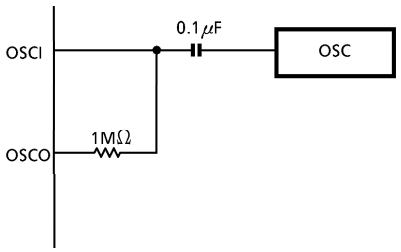
System	Input Range
NTSC	273H~515H
PAL	325H~614H

Shutter pulse is not allowed to change as follows;
- 10H before and after FSA/B in NTSC mode.
- 12H before and 11H after FSA/B in PAL mode.

INPUT OF MASTER CLOCK

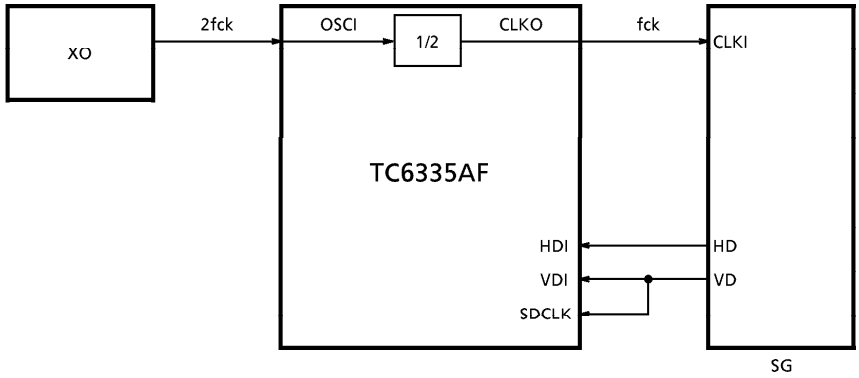
- It is necessary the symmetry of master clock put on OSCI is within 50 ± 10%.





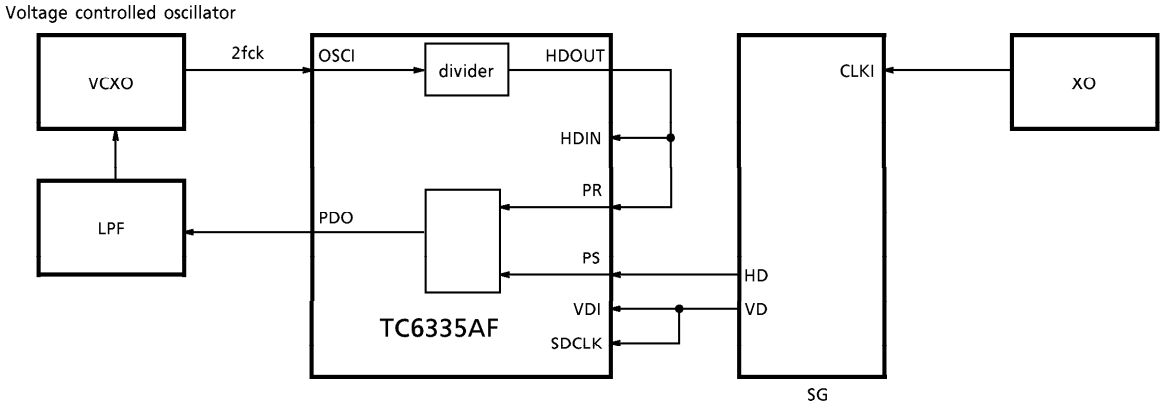
CONNECTION TO SYNCHRONIZATION GENERATOR IC

- Connection to synchronization generator IC
  (master clock is fck)



- Connection to synchronization generator IC
  (master clock is except fck)

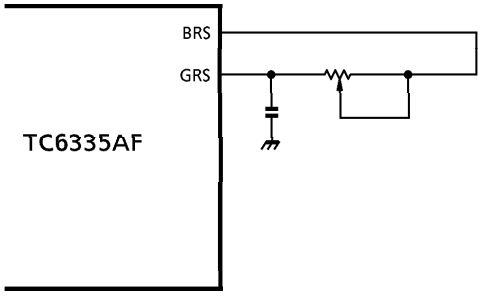
  If master clock of SG is except fck, it is necessary to lock the phase of an oscillator of SG and TC6317AF.
  Therefore TC6317AF has a divider dividing 2 fck into 1H and an internal phase comparator.



ADJUSTING PHASE OF THE PULSE

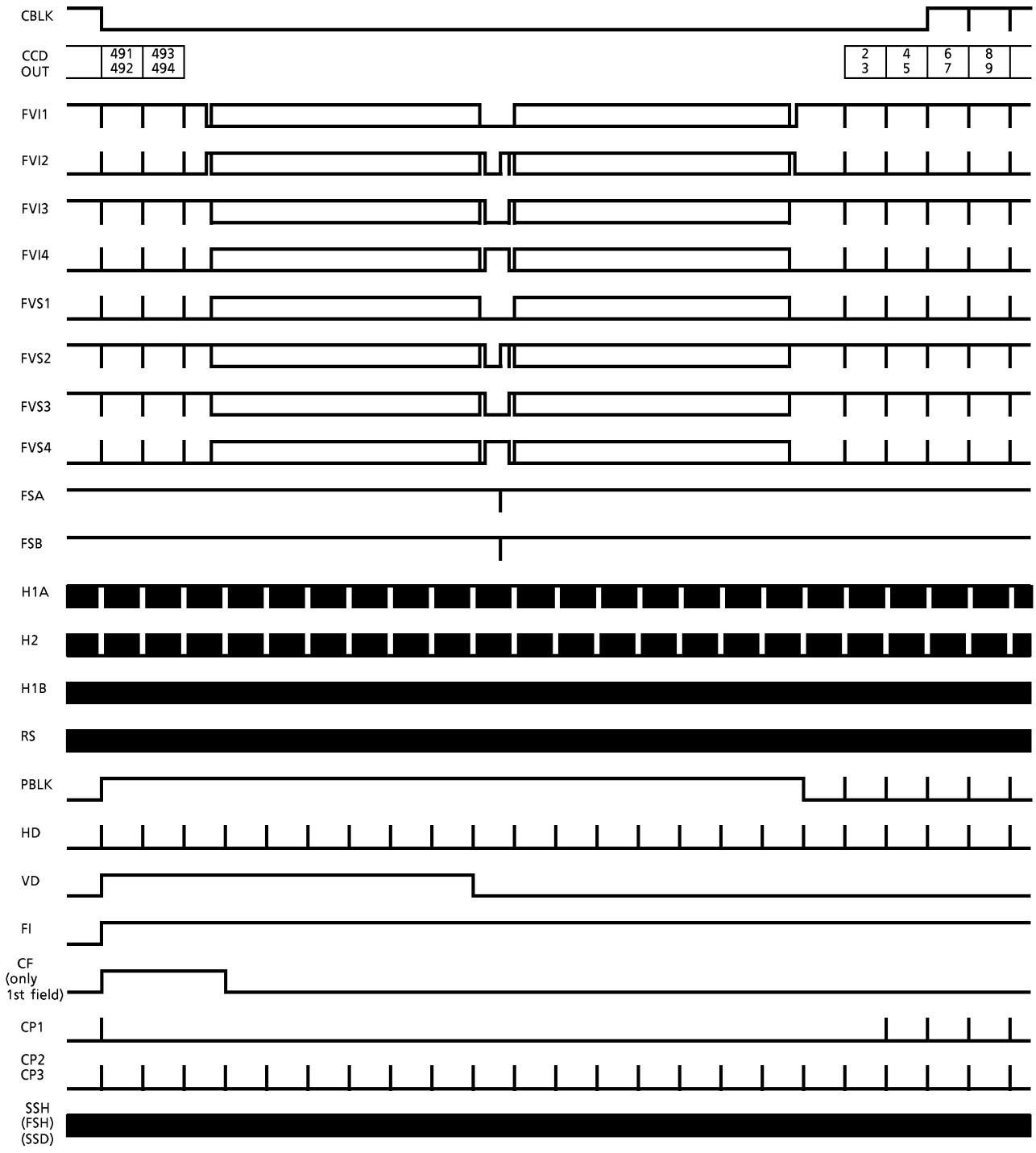
Adjusting phase and width of RS, SSH, FSH and SSD.

Adjusting phase of RS pulse shows as follows;

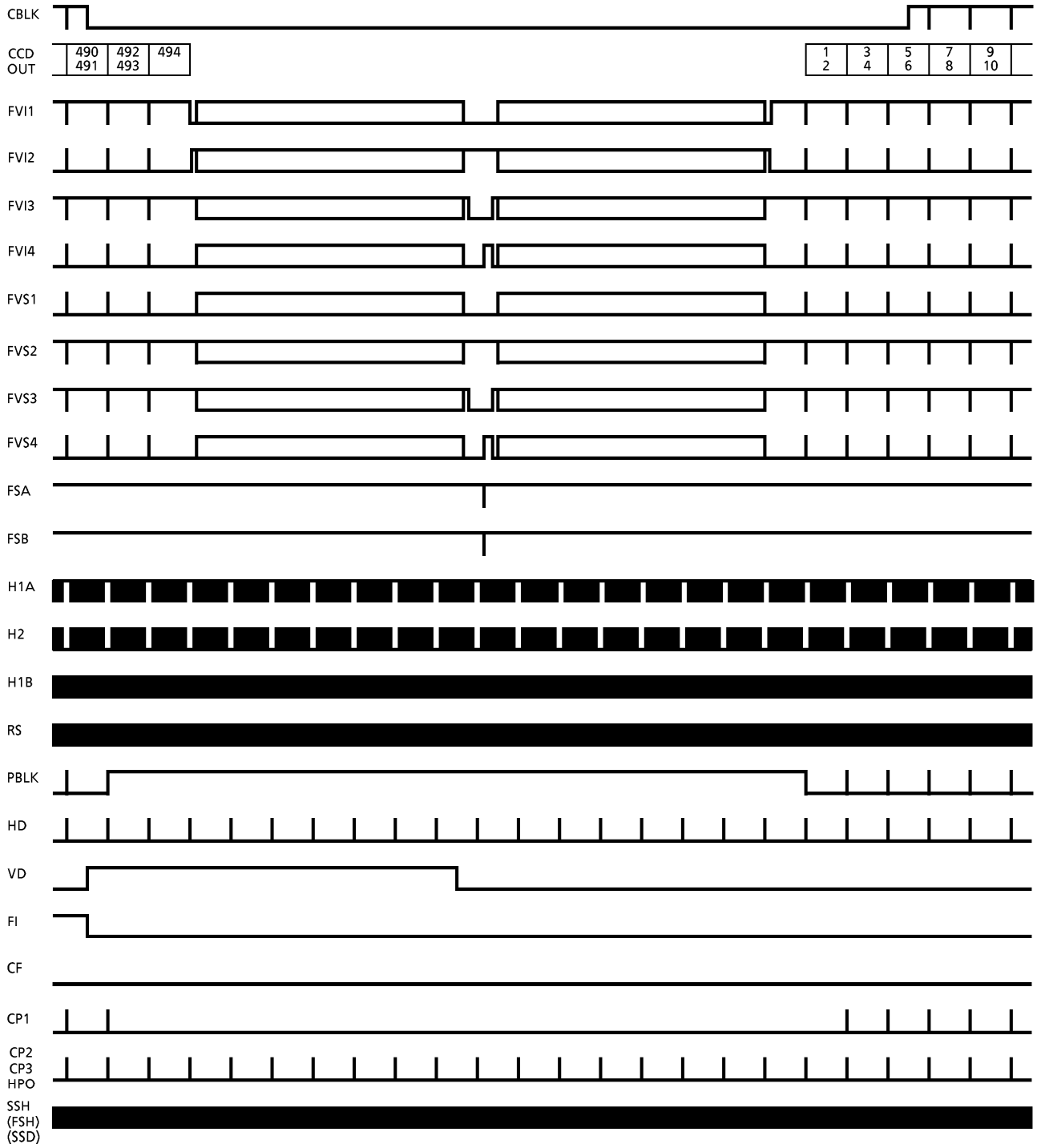


EDTV-Ⅱ Mode TIMING CHART

Odd Field / Normal Mode



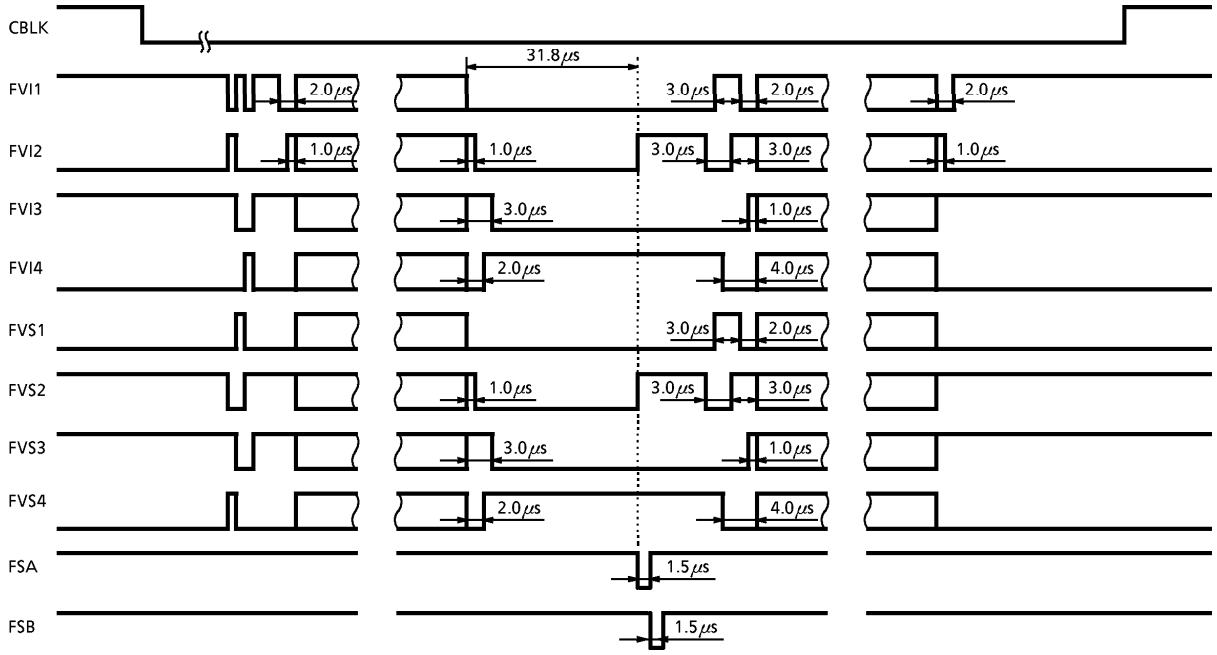
Even Field / Normal Mode



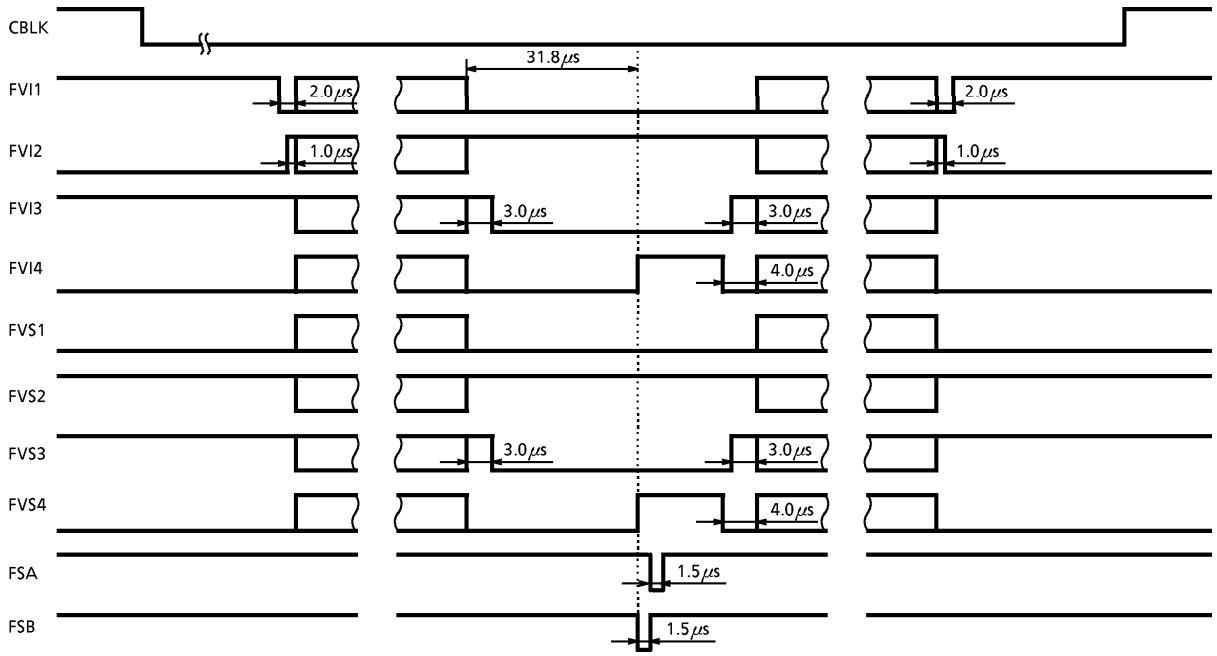
EDTV – II Mode (EXPANDED) (Field shift part)

Odd Field

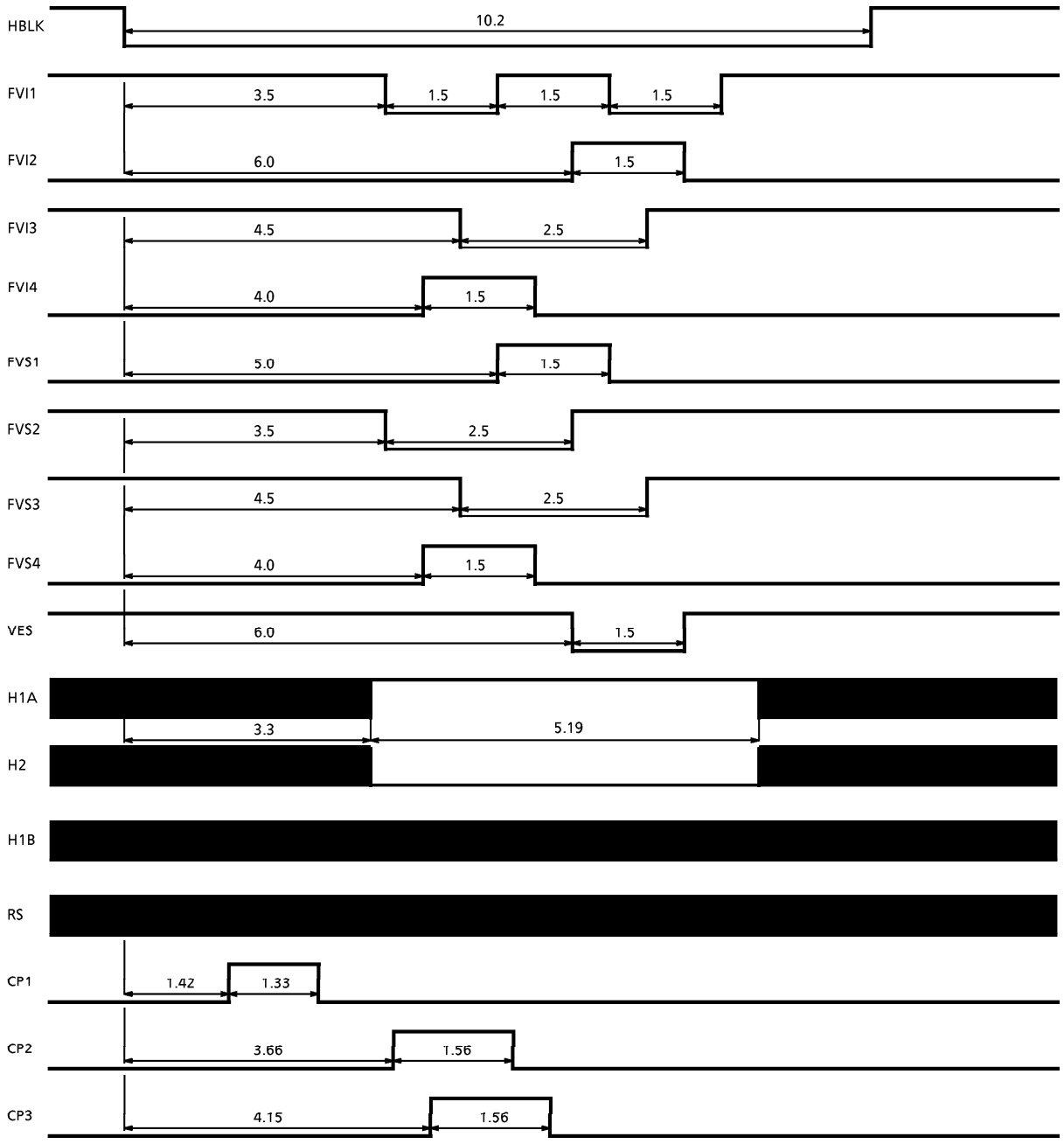
Unit : μs



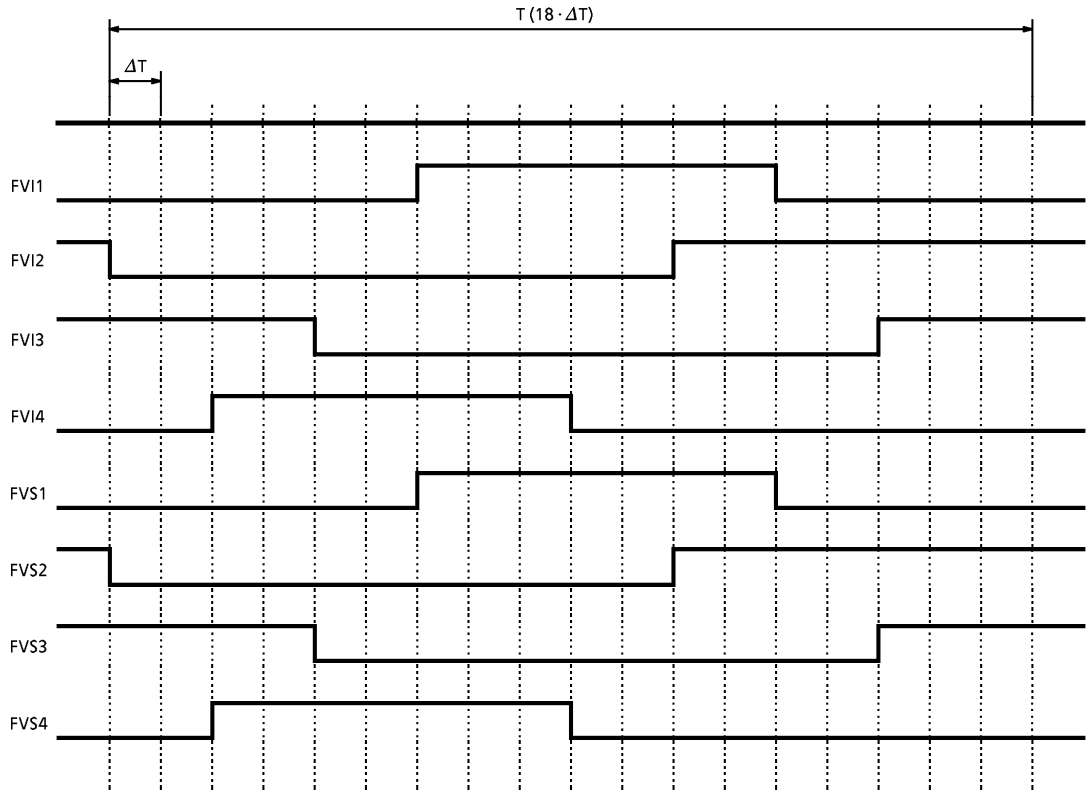
Even Field



EDTV – II Mode (EXPANDED) (Line shift part) Unit : μs



EDTV – II Mode (EXPANDED) (High speed transfer part)



Disuse signal transfer

ΔT = 44.4 (ns)

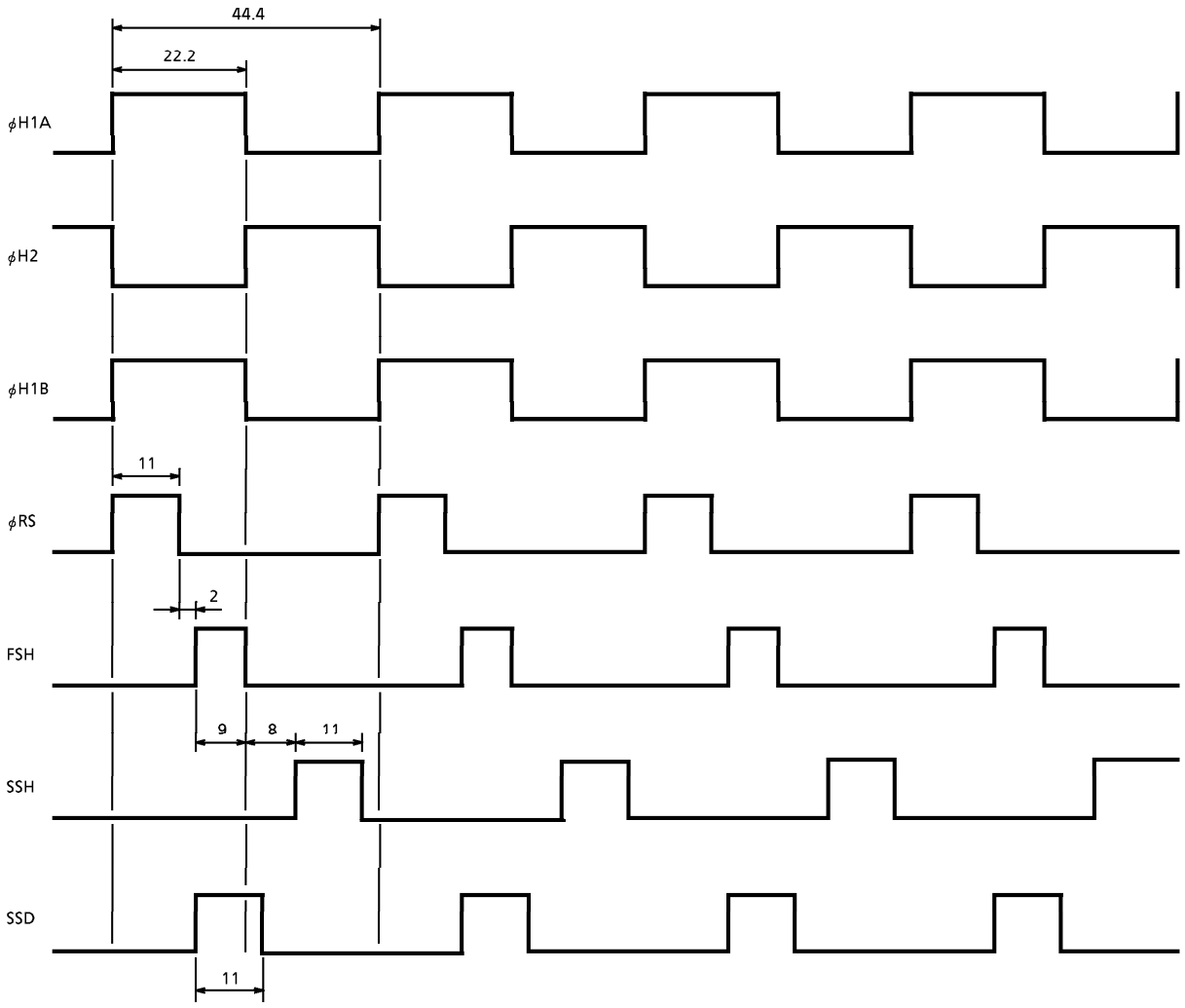
T = 0.8 (μs) (1.25MHz)

Signal transfer

ΔT = 88.9 (ns)

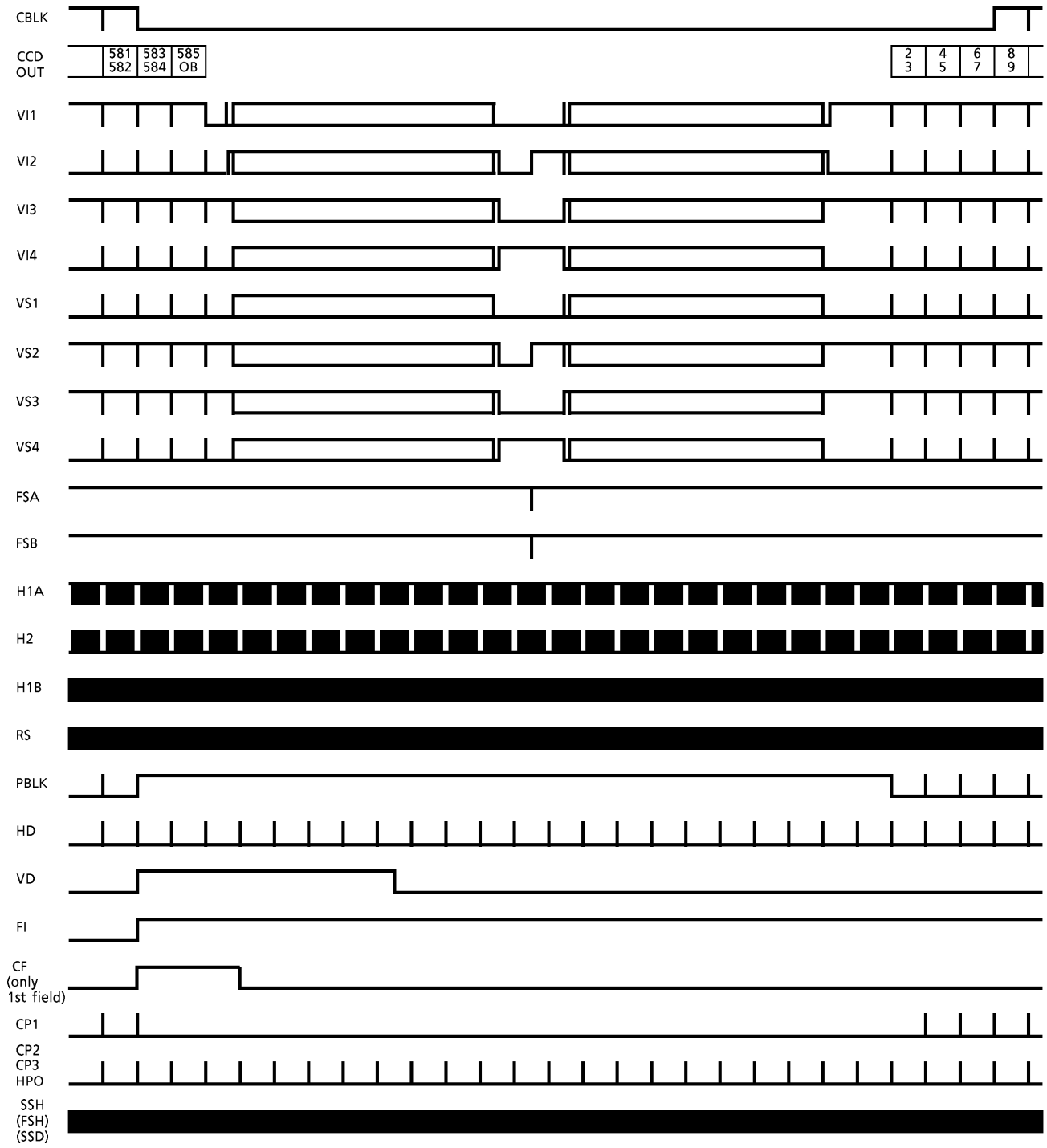
T = 1.6 (μs) (625kHz)

EDTV – II Mode (EXPANDED) (Horizontal rate timing) Unit : ns

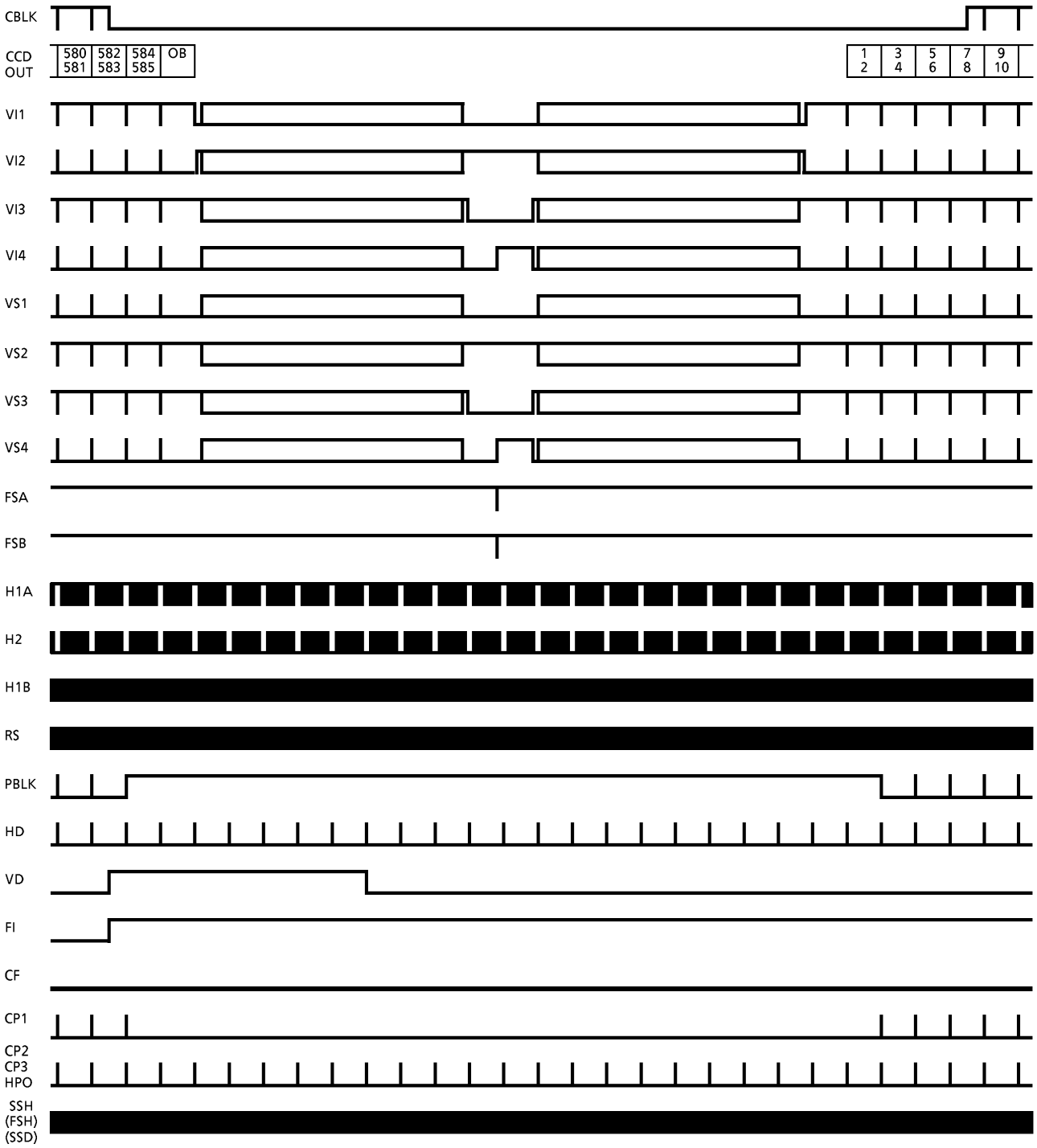


PAL – plus Mode TIMING CHART

Odd Field / Normal Mode



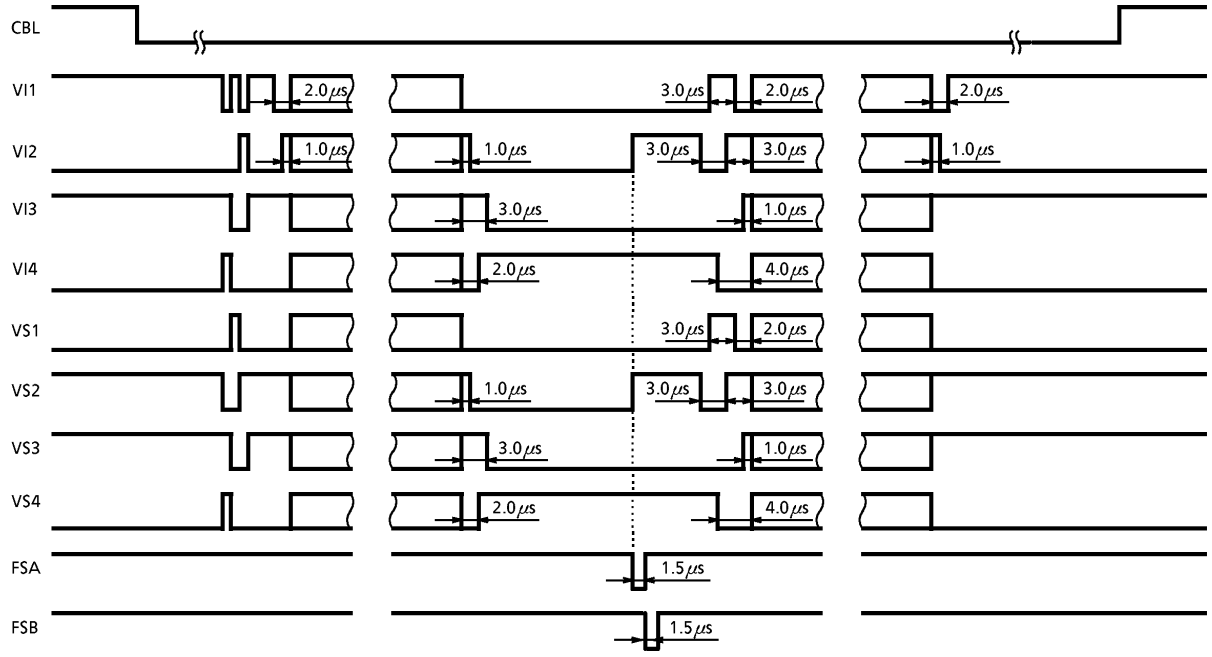
Even Field / Normal Mode



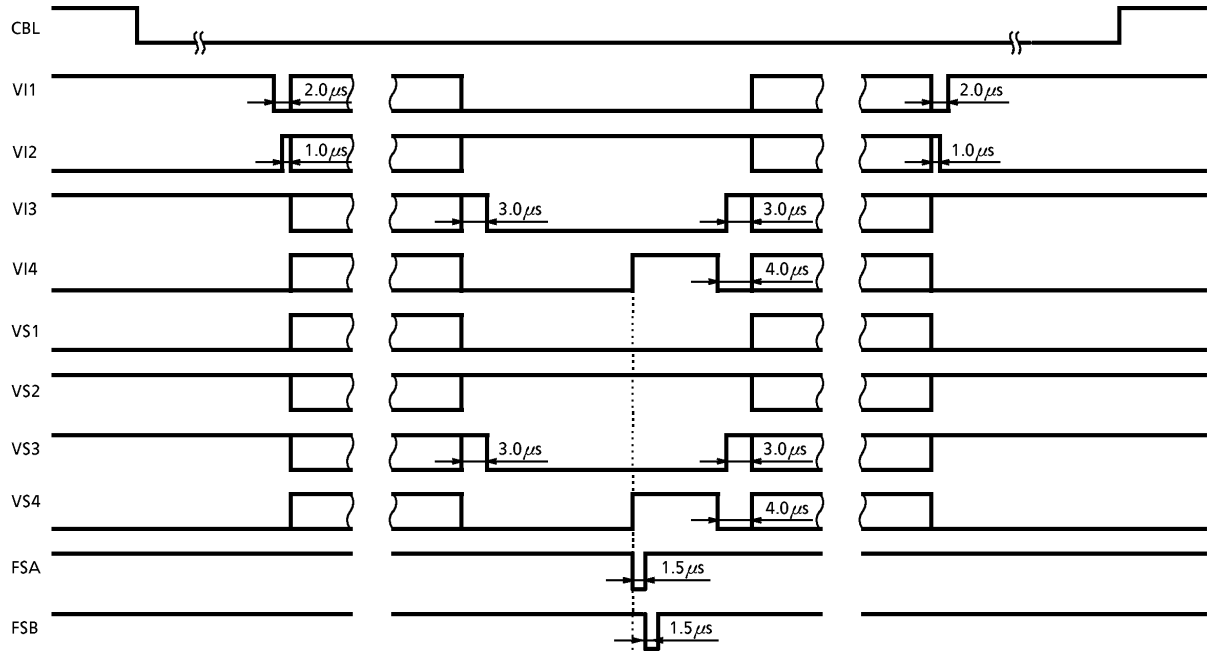
PAL – plus Mode (EXPANDED) (Field shift part)

Odd Field

Unit : μs

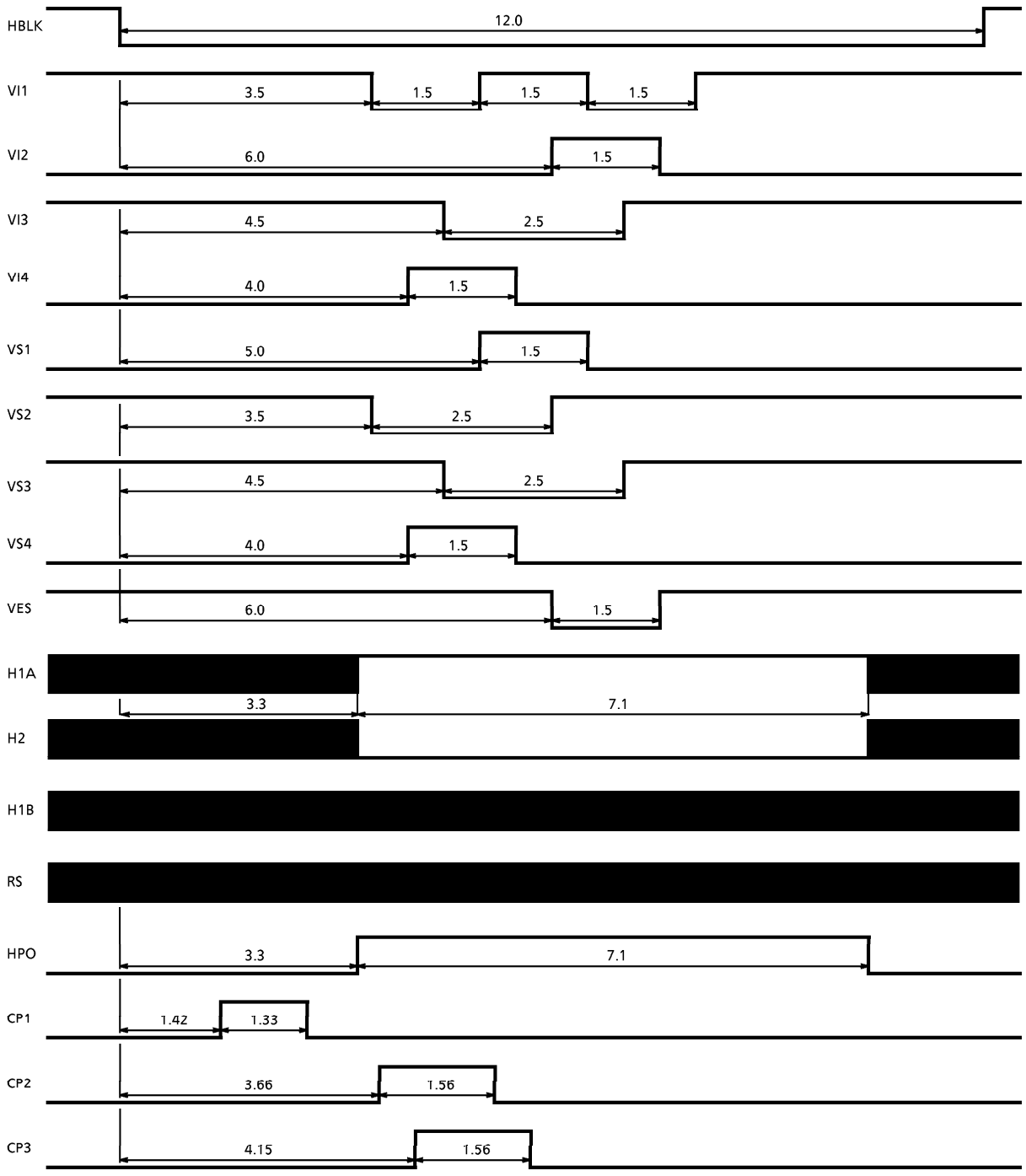


Even Field

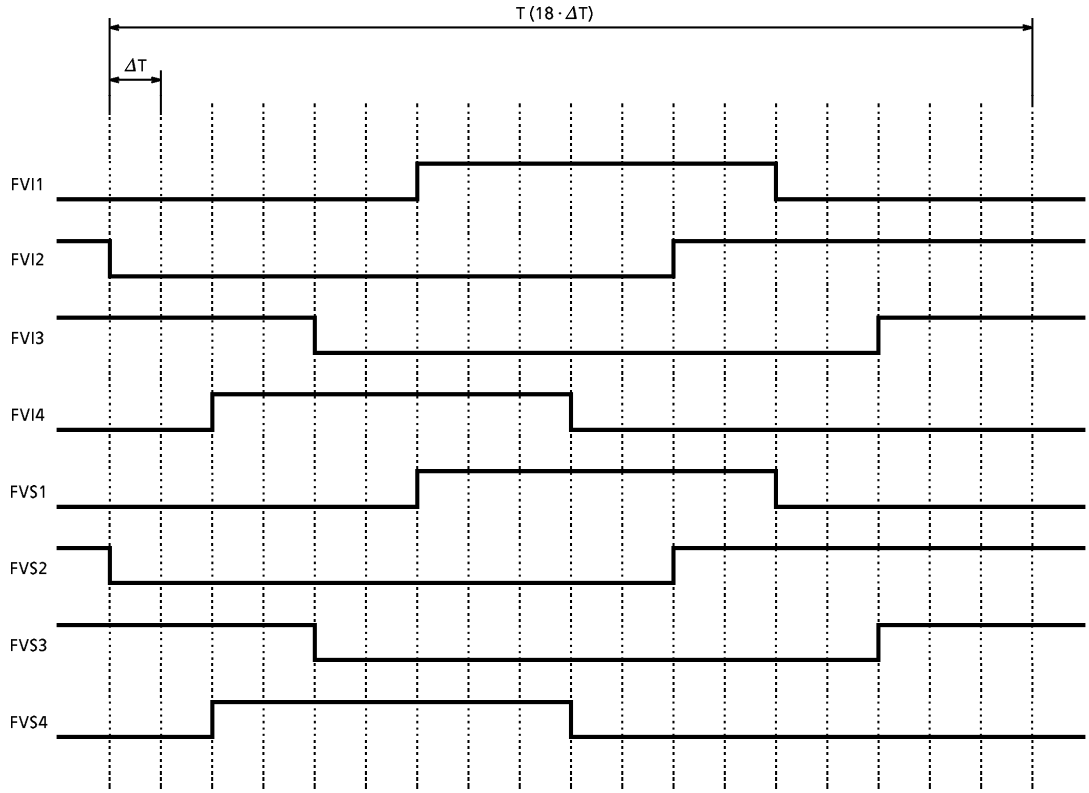


PAL – plus Mode (EXPANDED) (Line shift part)

Unit : μs



PAL – plus Mode (EXPANDED) (High speed transfer part)



Disuse signal transfer

$\Delta T = 44.4$ (ns)

$T = 0.8$ (μs) (1.25MHz)

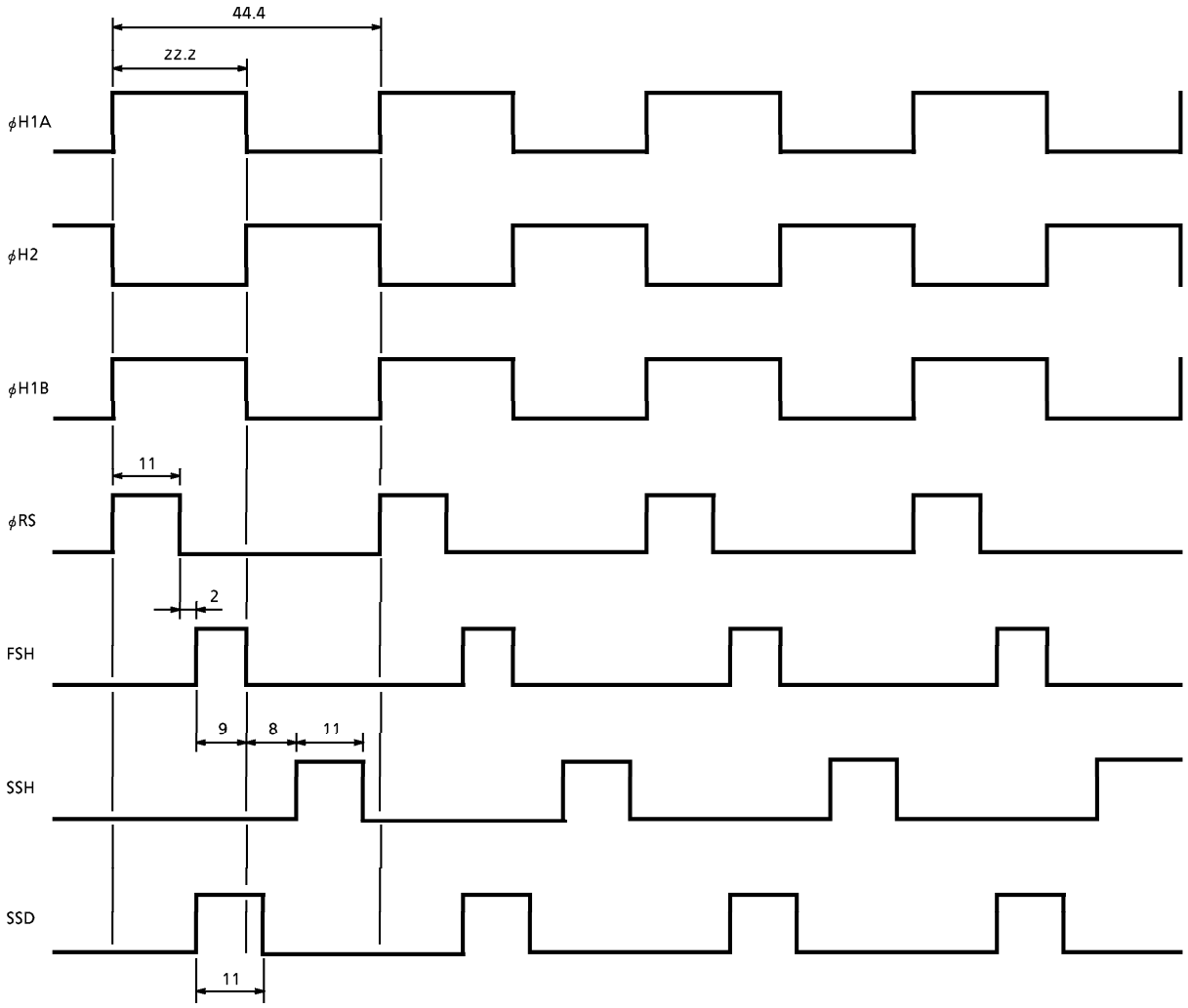
Signal transfer

$\Delta T = 88.9$ (ns)

$T = 1.6$ (μs) (625kHz)

PAL – plus Mode (EXPANDED) (Horizontal rate timing)

Unit : ns

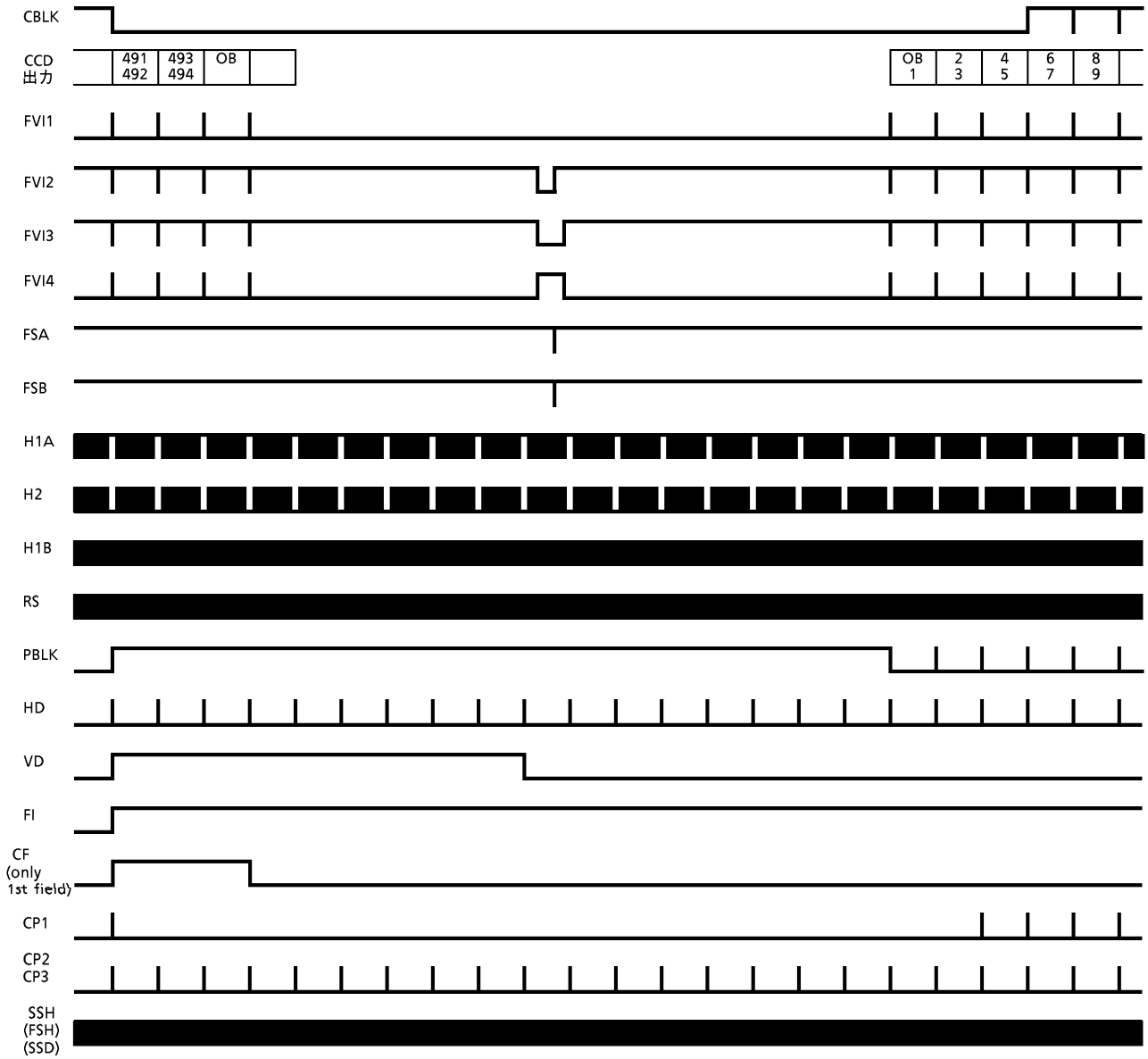


- IT drive (94 Pin : H)

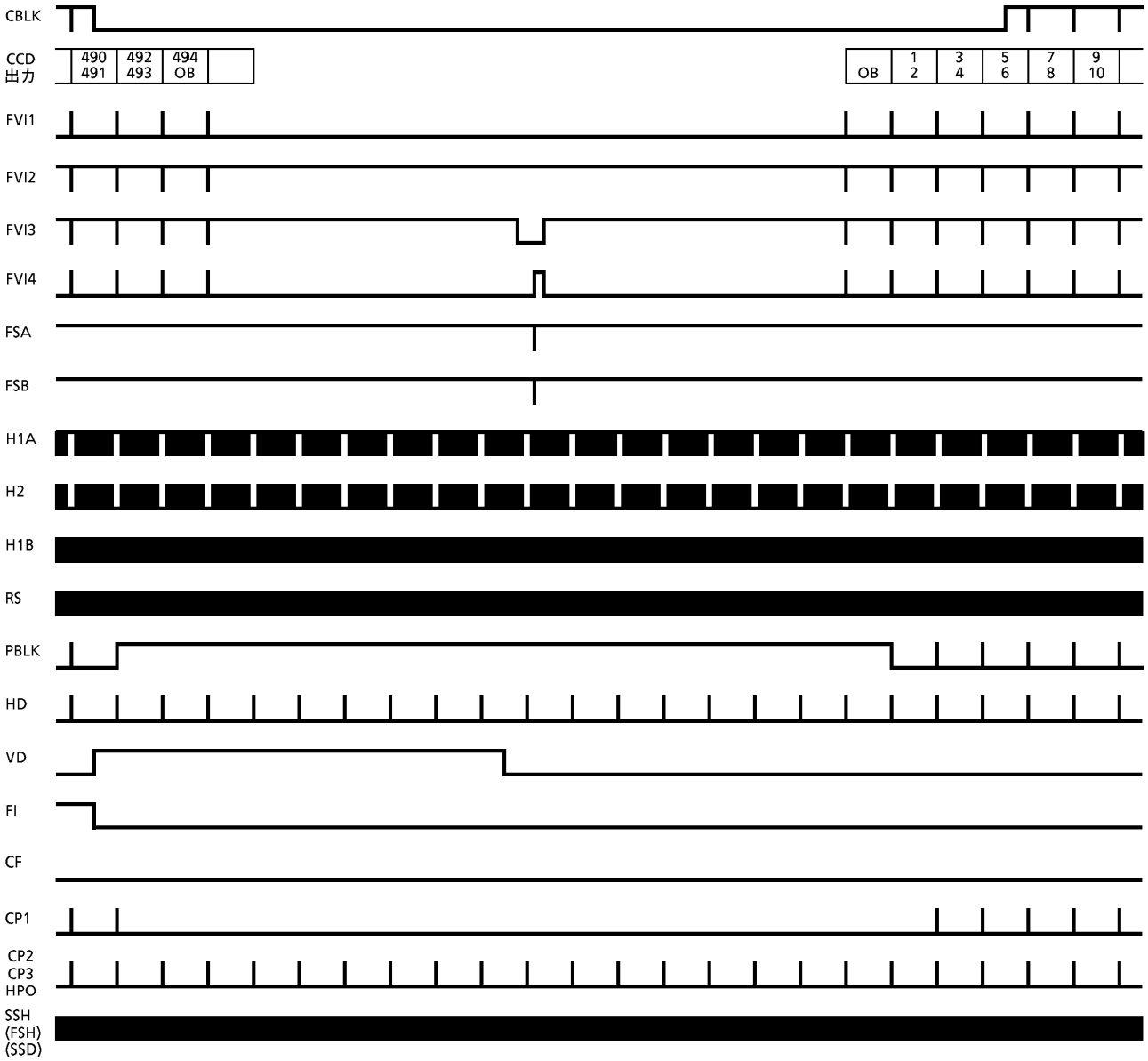
  (Sweep disable, 52 Pin : H)

  EDTV – II Mode TIMING CHART (11 Pin : L)

  Odd Field / Normal Mode



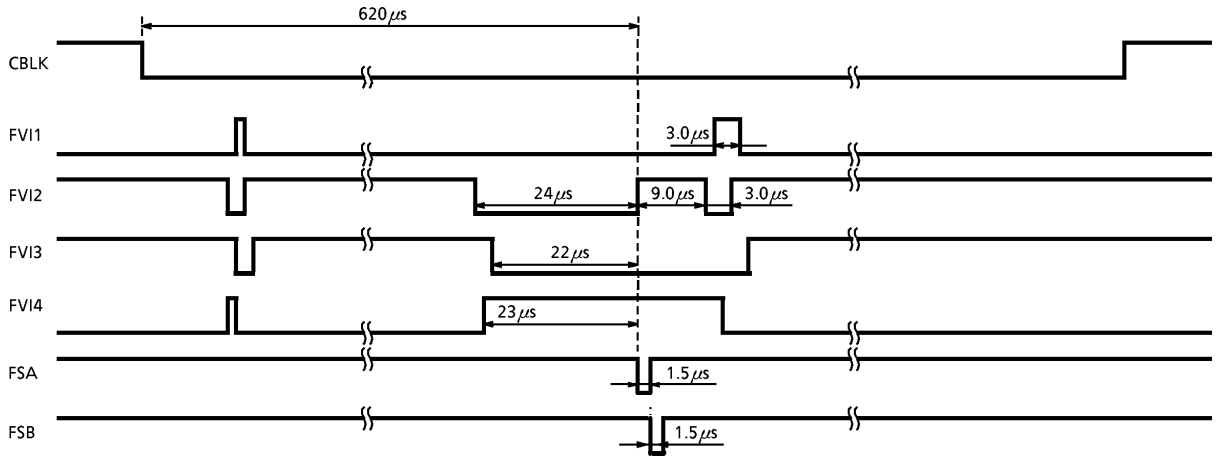
Even Field / Normal Mode



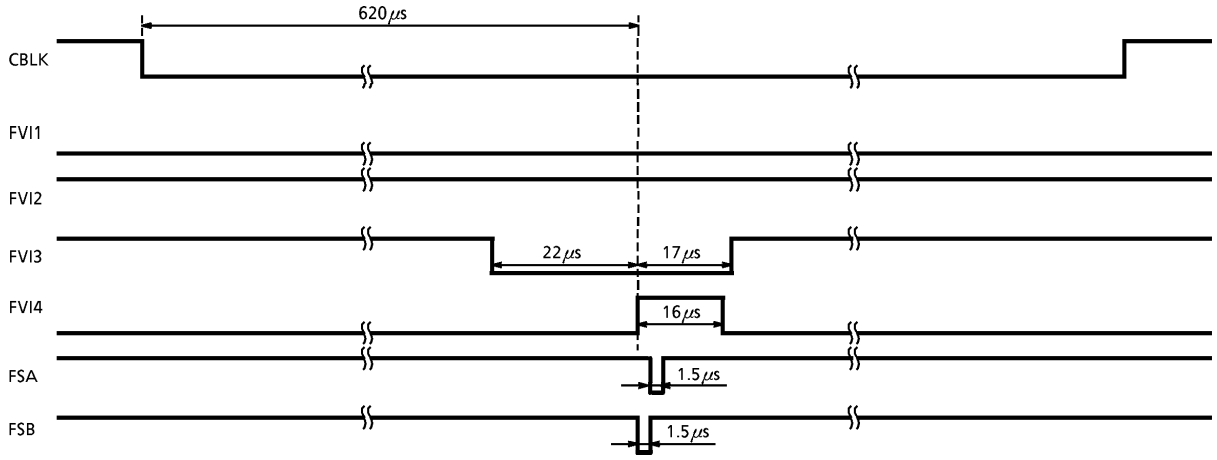
EDTV – II Mode (EXPANDED) (Field shift part)

Odd Field

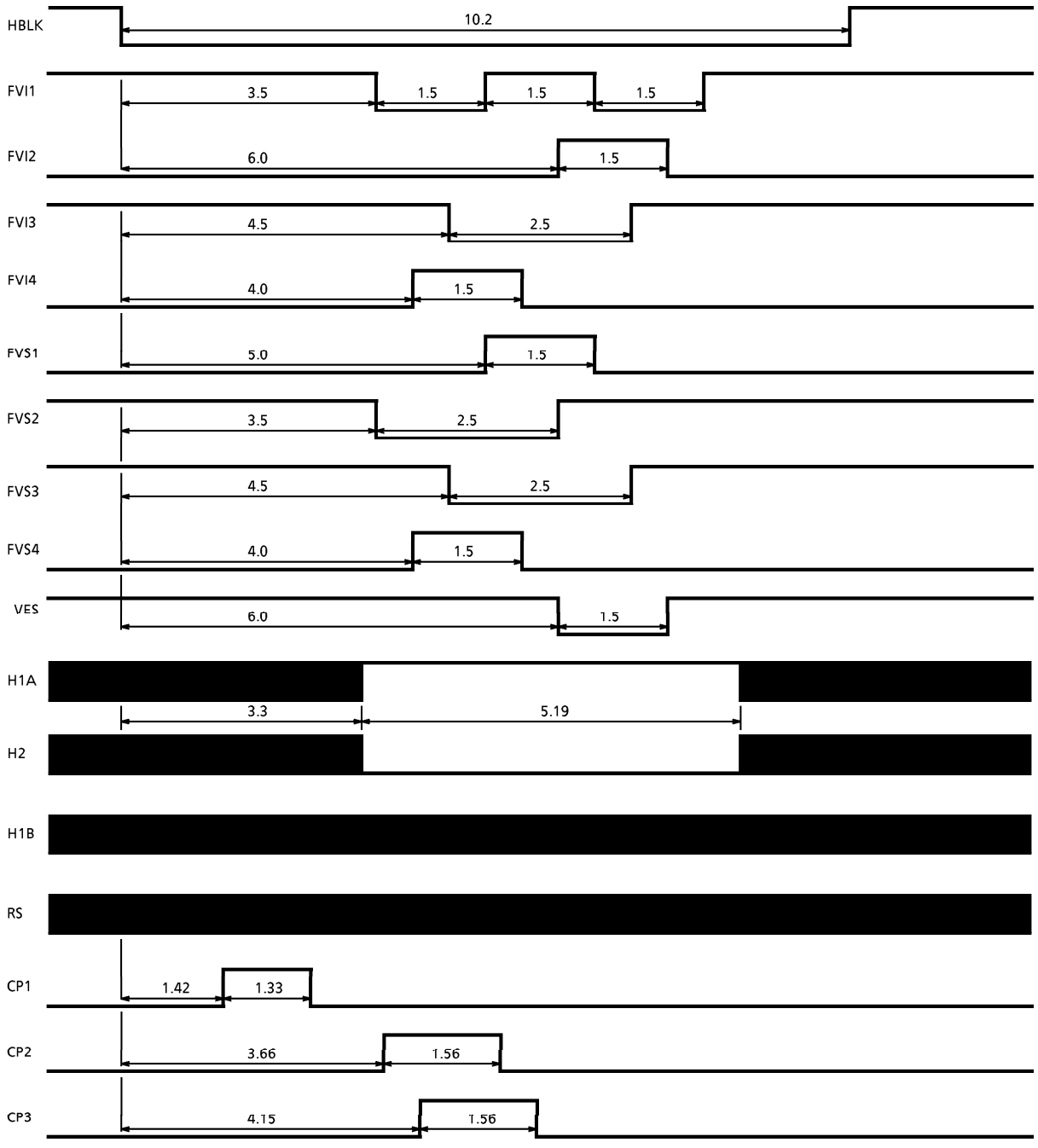
Unit : μs



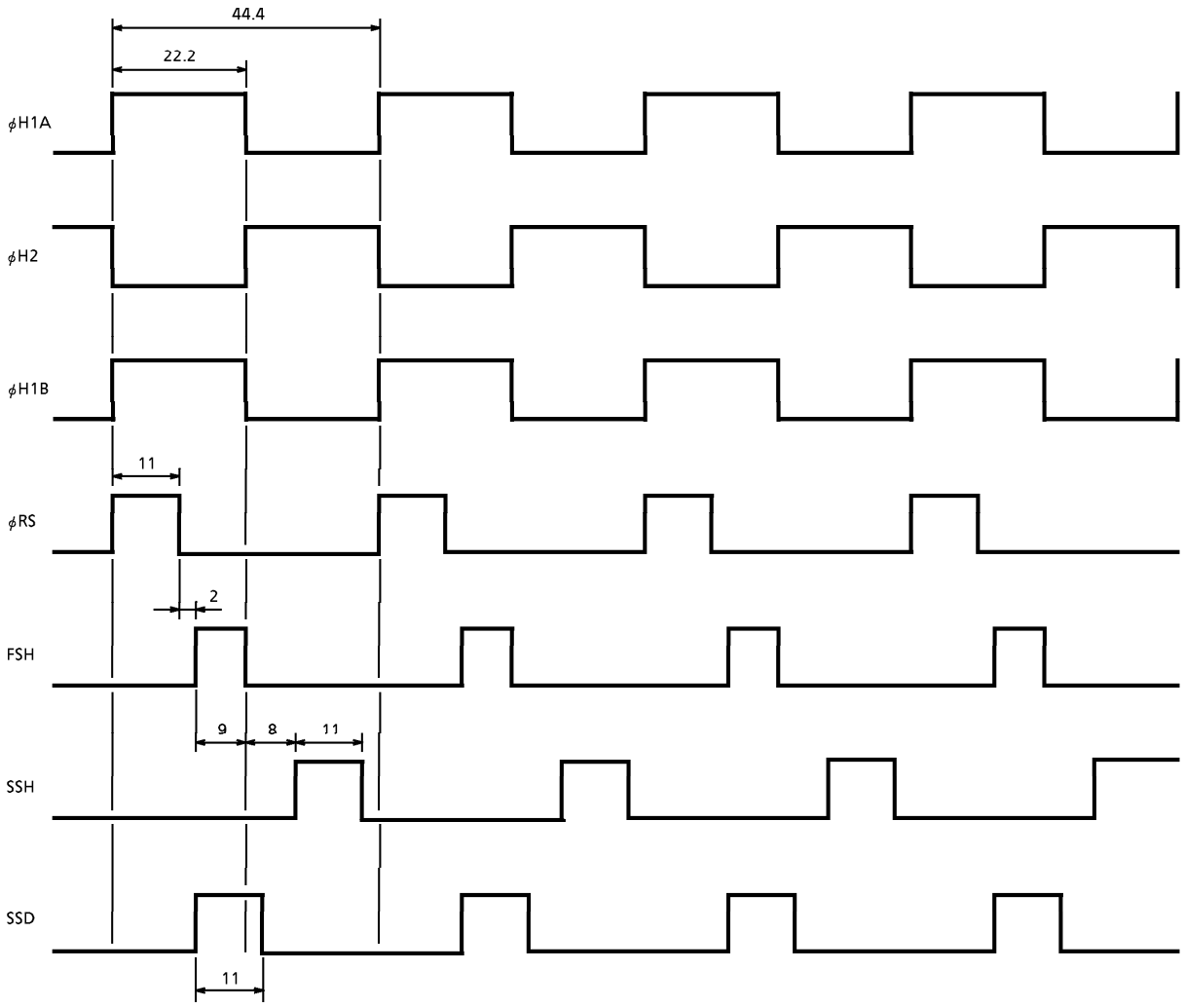
Even Field



EDTV – II Mode (EXPANDED) (Line shift part) Unit : μs

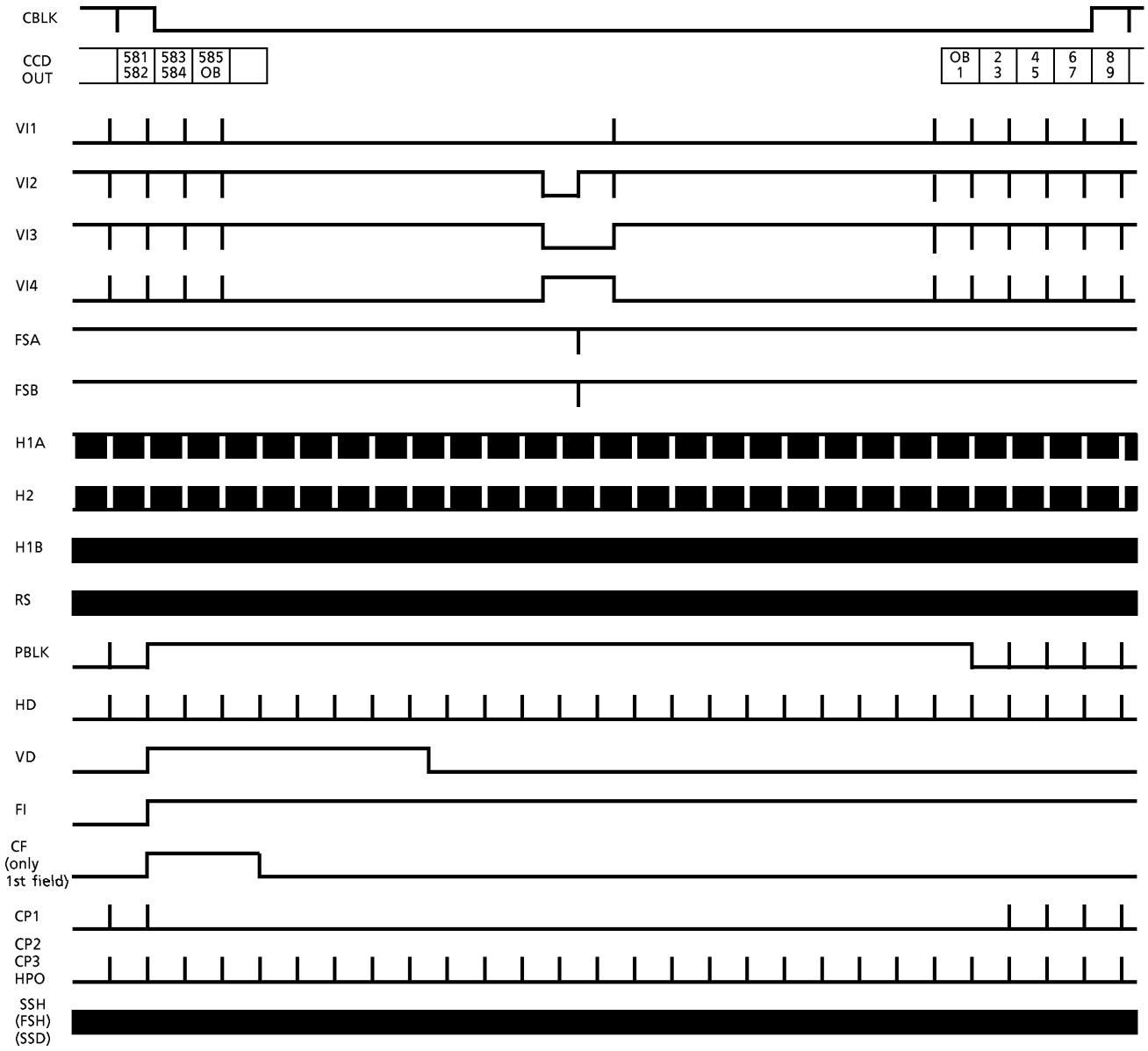


EDTV – II Mode (EXPANDED) (Horizontal rate timing) Unit : ns

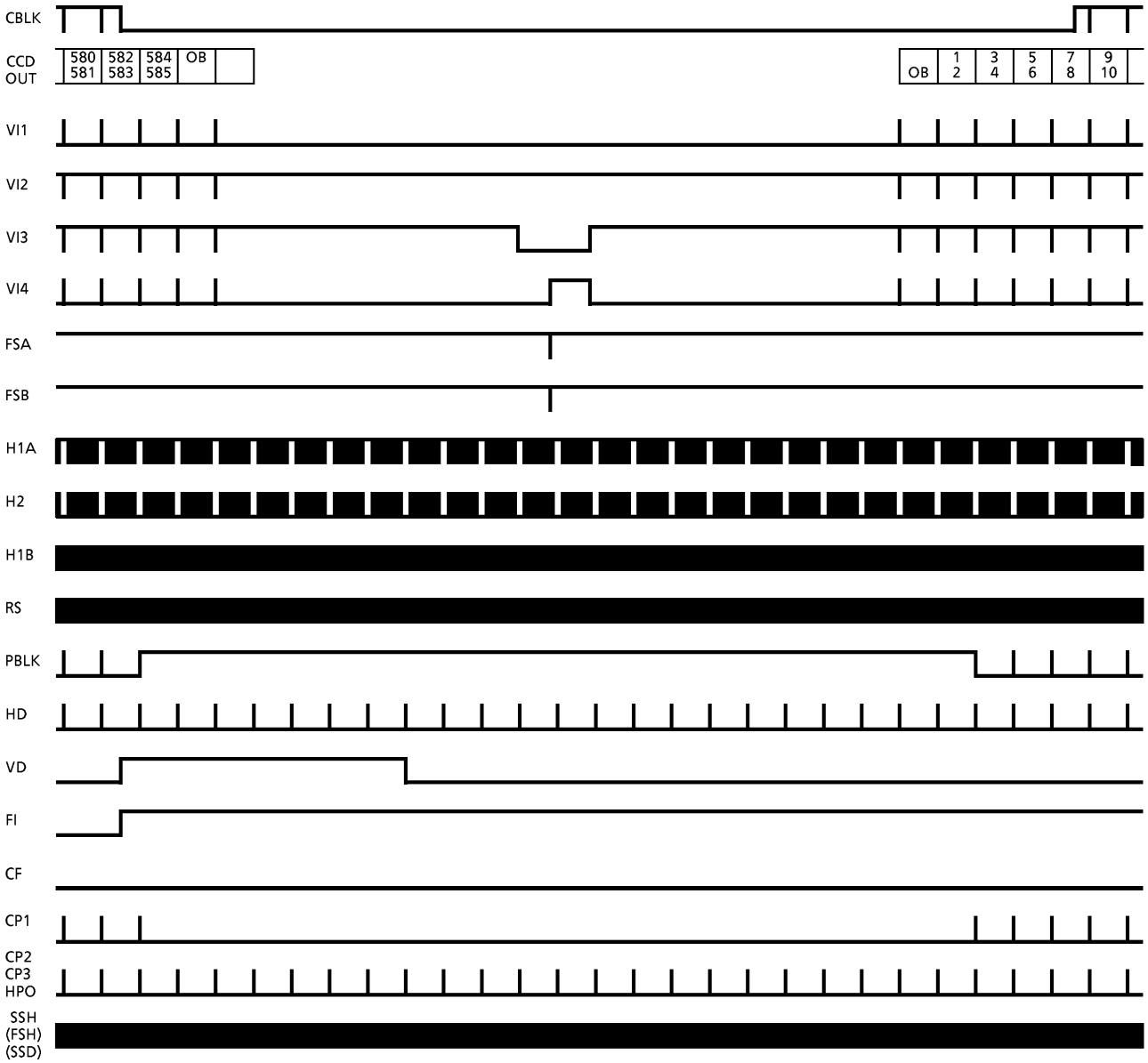


PAL – plus Mode TIMING CHART (11 Pin : H)

Odd Field / Normal Mode



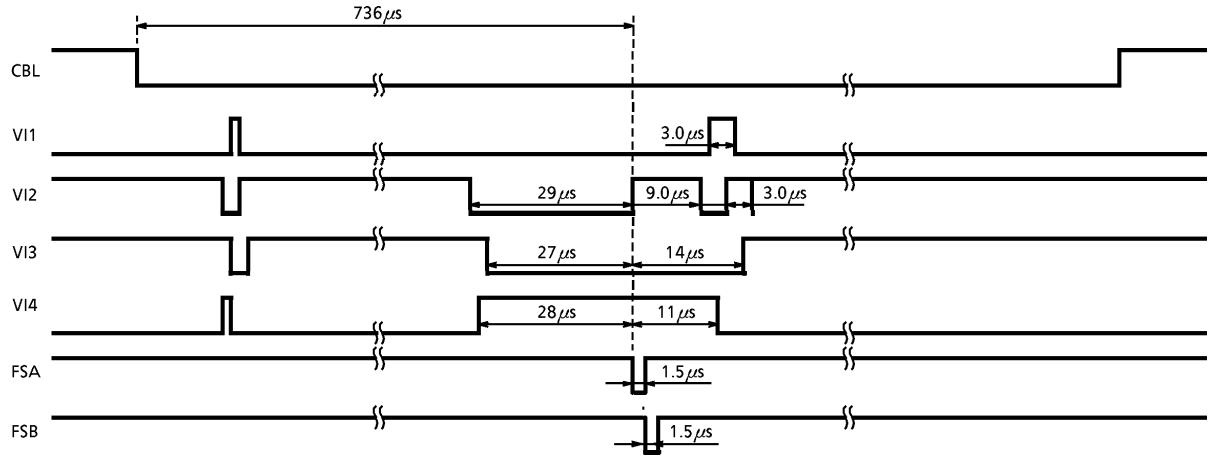
Even Field / Normal Mode



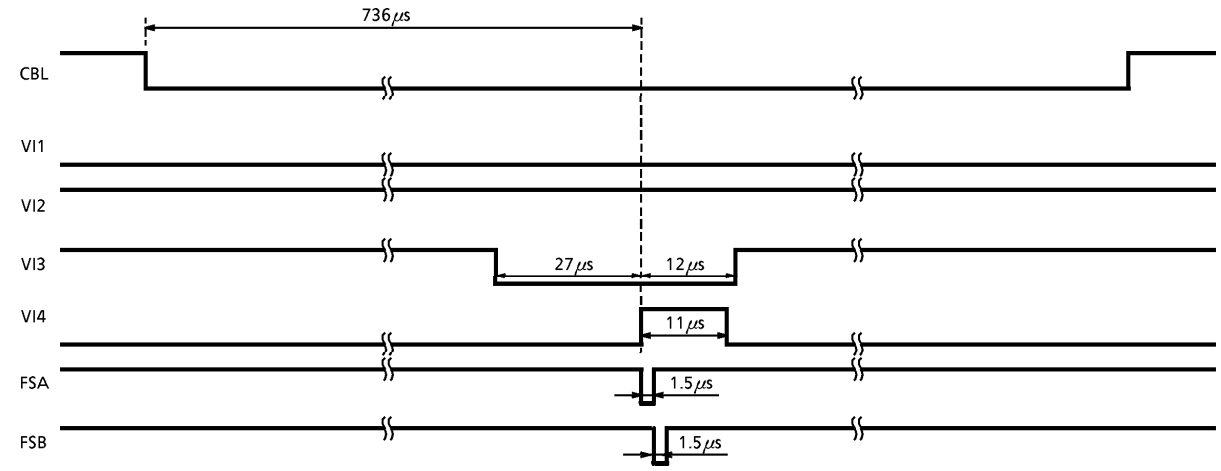
PAL – plus Mode (EXPANDED) (Field shift part)

Odd Field

Unit : μs

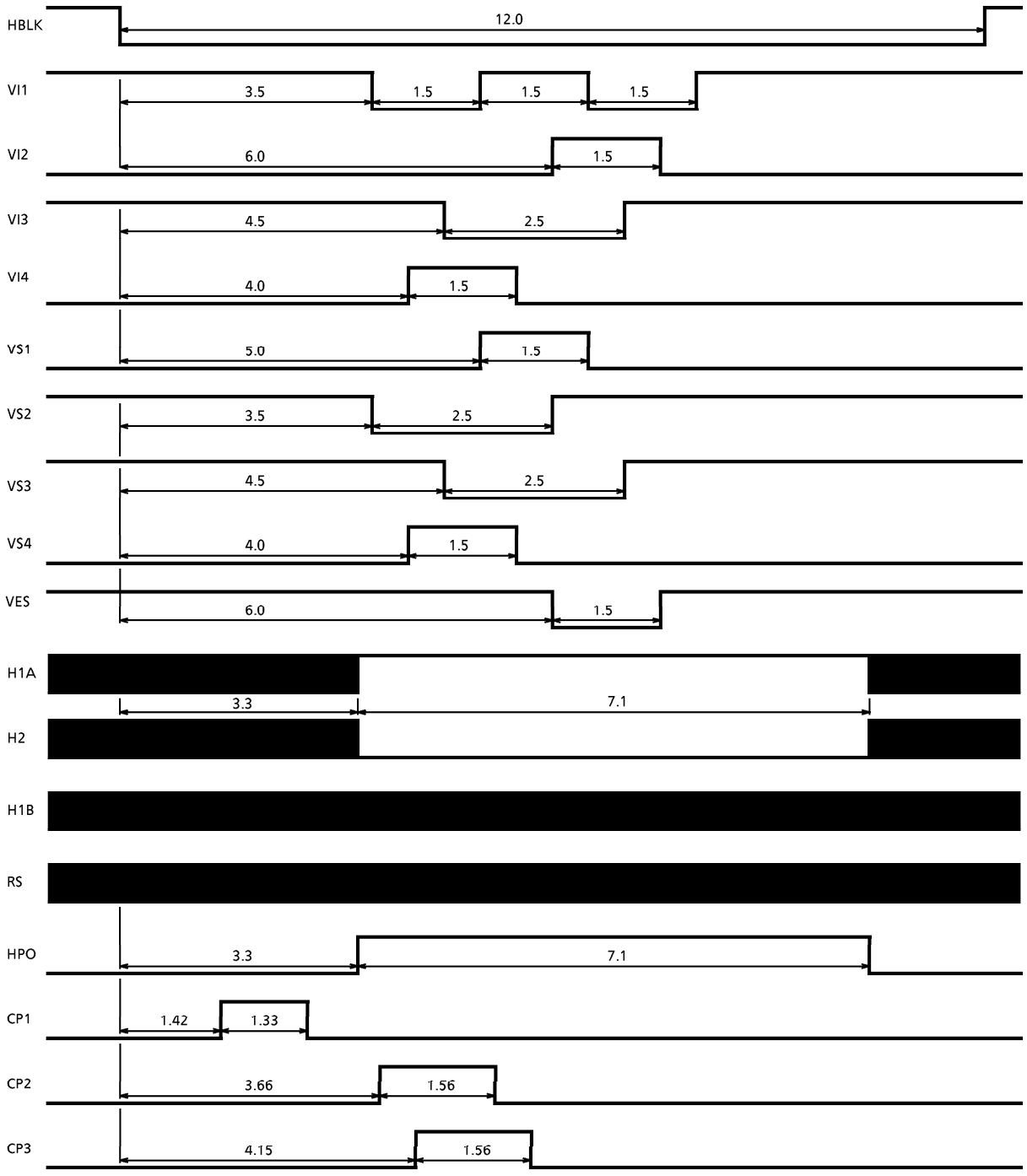


Even Field



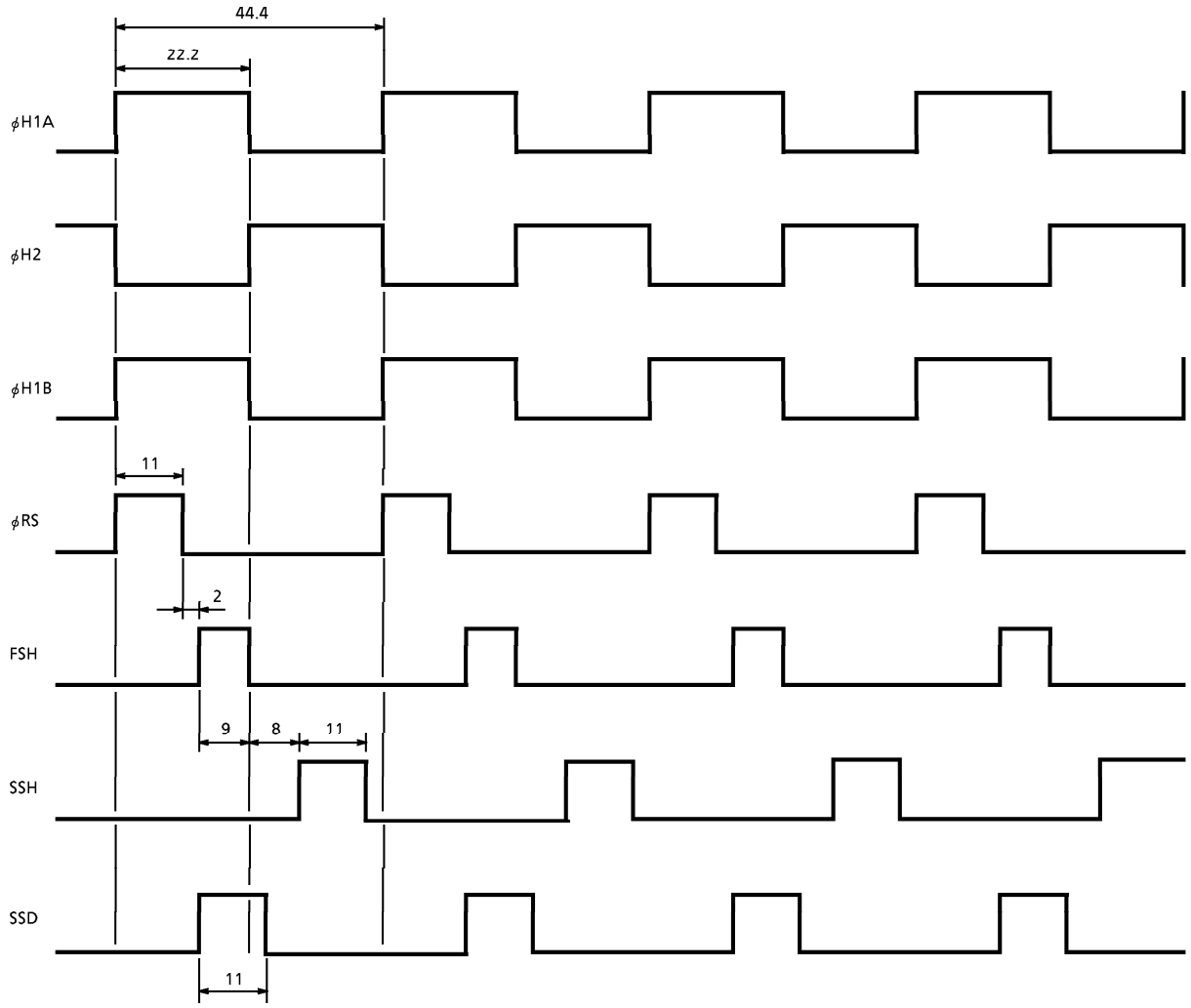
PAL – plus Mode (EXPANDED) (Line shift part)

Unit : μs



PAL – plus Mode (EXPANDED) (Horizontal rate timing)

Unit : ns

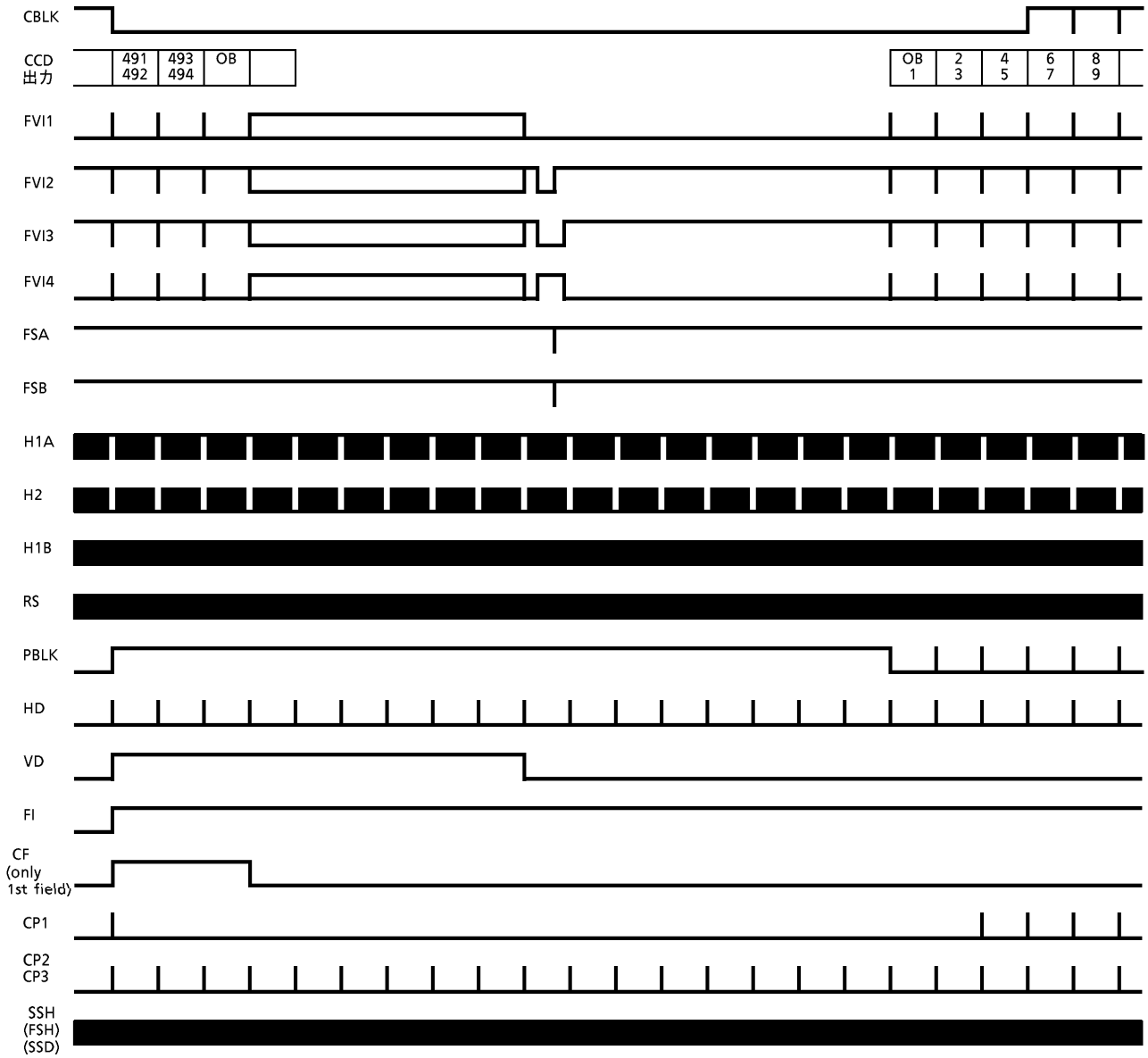


- IT drive (94 Pin : H)

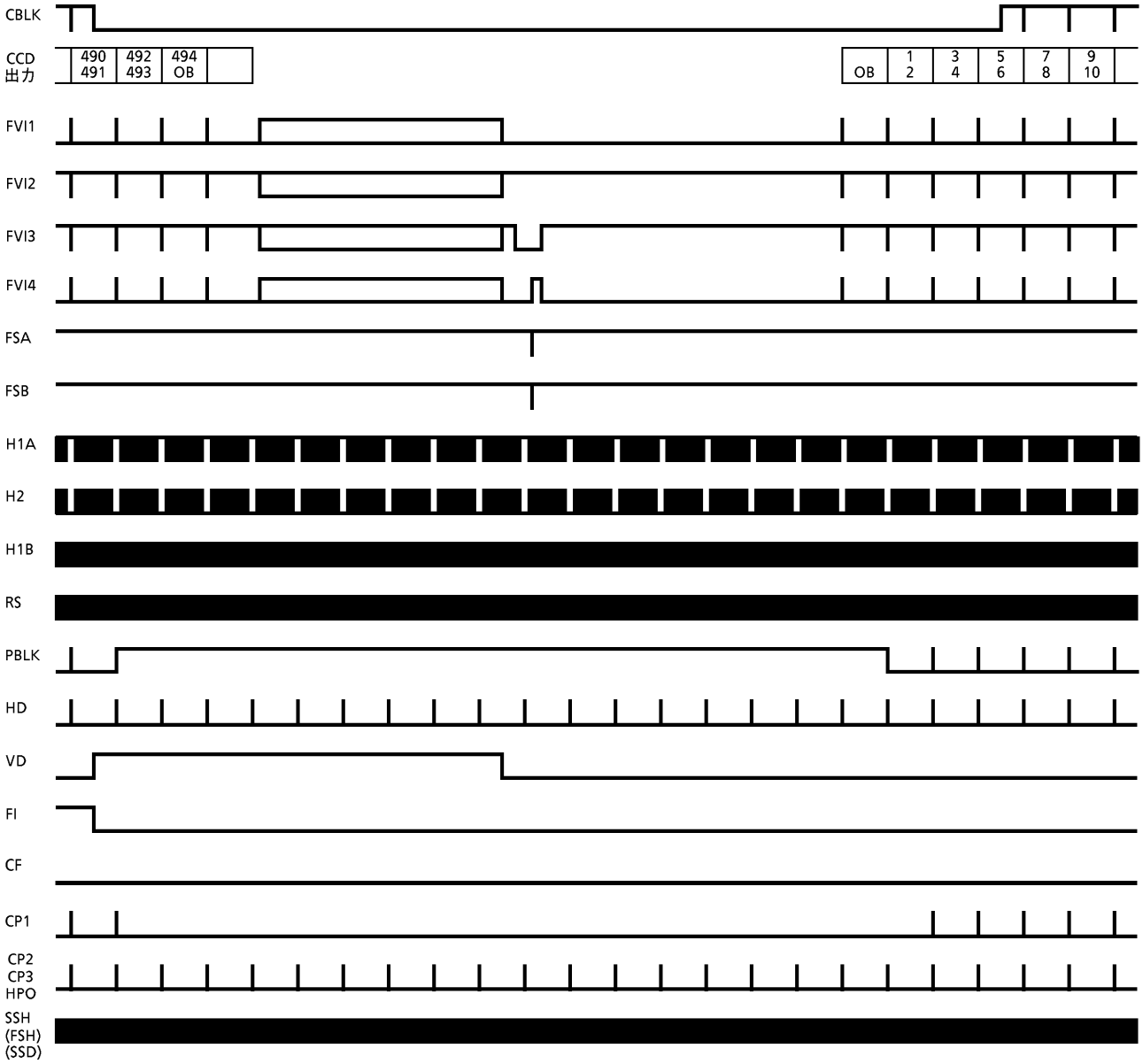
  (Sweep enable, 52 Pin : L)

  EDTV-II Mode TIMING CHART (11 Pin : L)

  Odd Field / Normal Mode



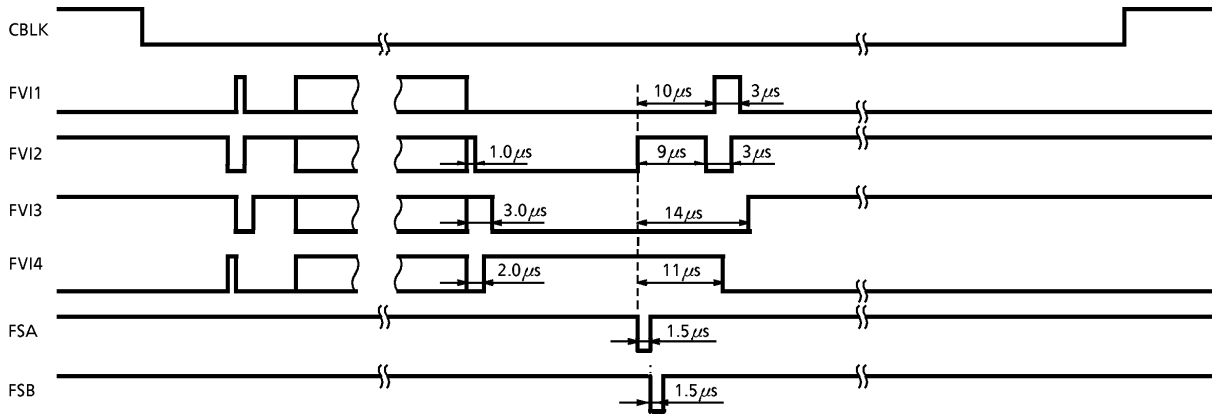
Even Field / Normal Mode



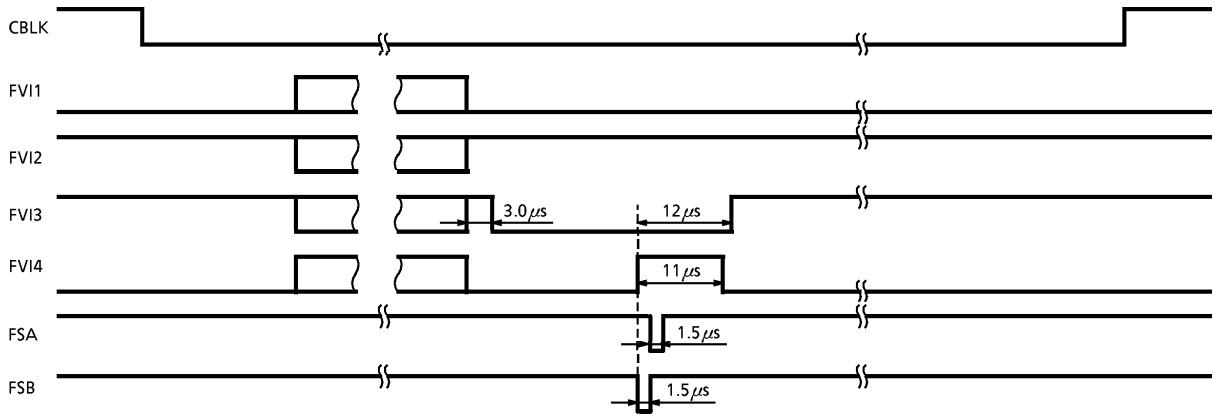
EDTV-Ⅱ Mode TIMING CHART

Odd Field

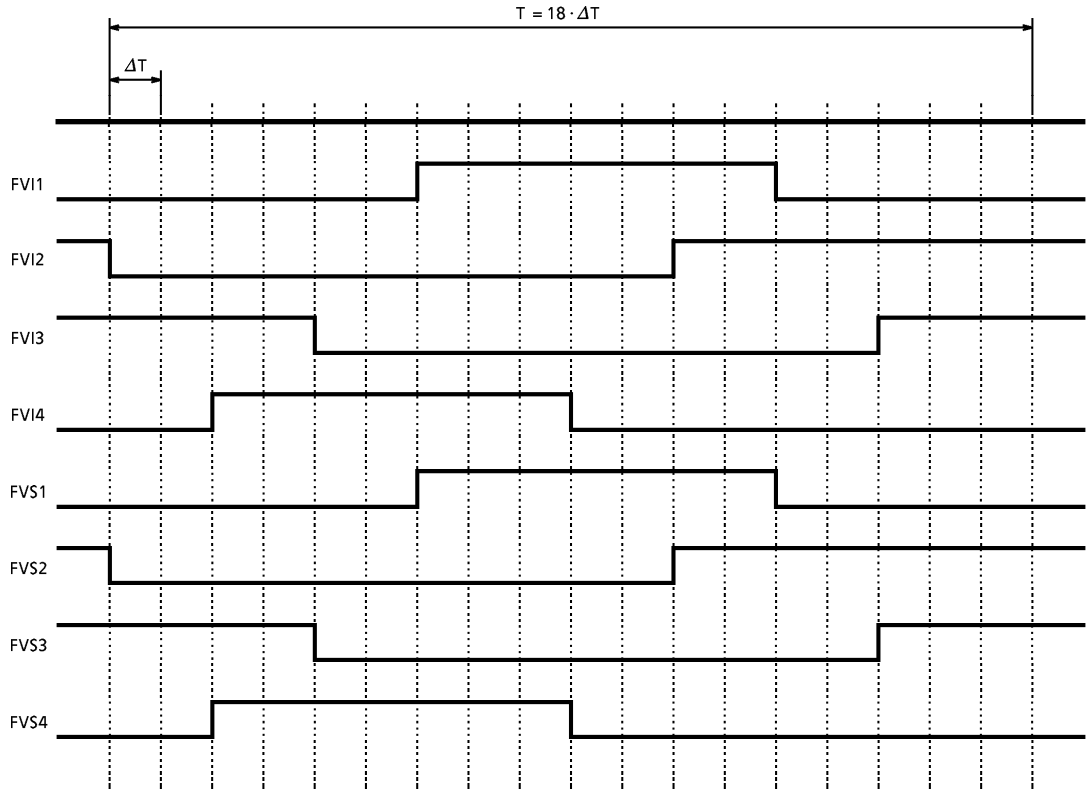
単位 : μs



Even Field



EDTV – II Mode (EXPANDED) (High speed transfer part)



Disuse signal transfer

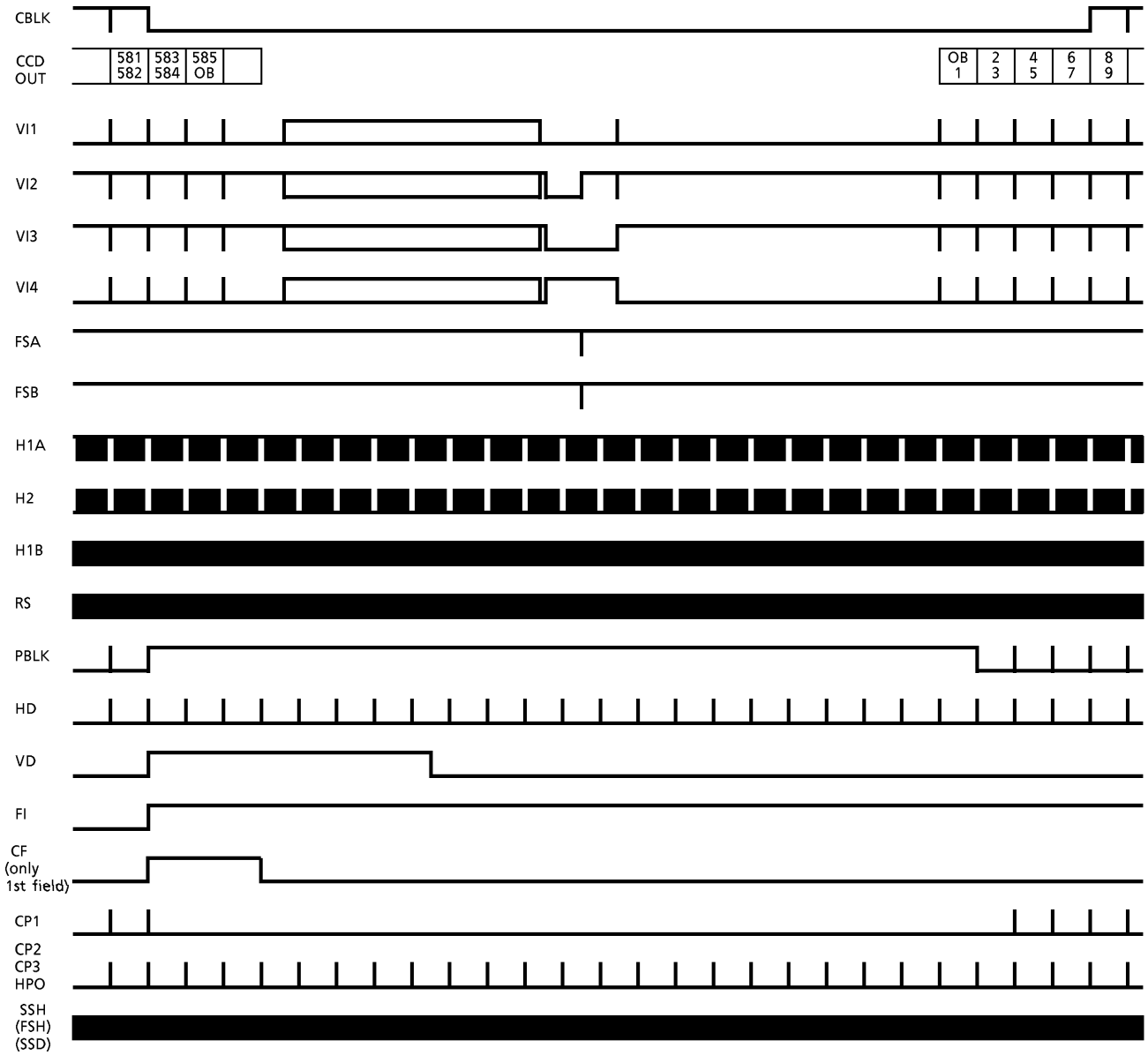
$\Delta T = 44.4$ (ns)

$T = 0.8$ (μs) (1.25MHz)

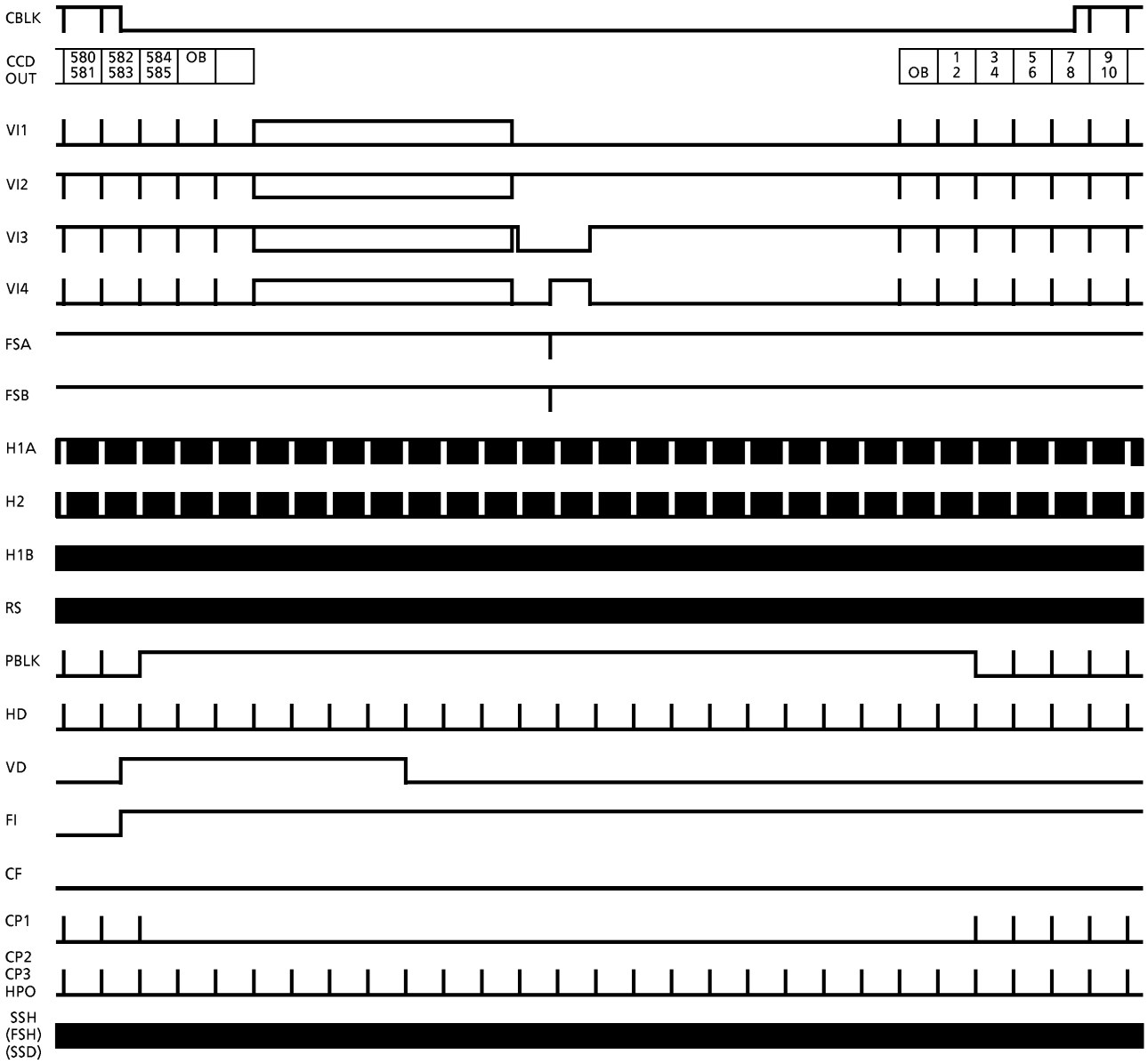
* Line shift part and H-type timing are same as sweep disable mode.

PAL – plus Mode TIMING CHART

Odd Field / Normal Mode



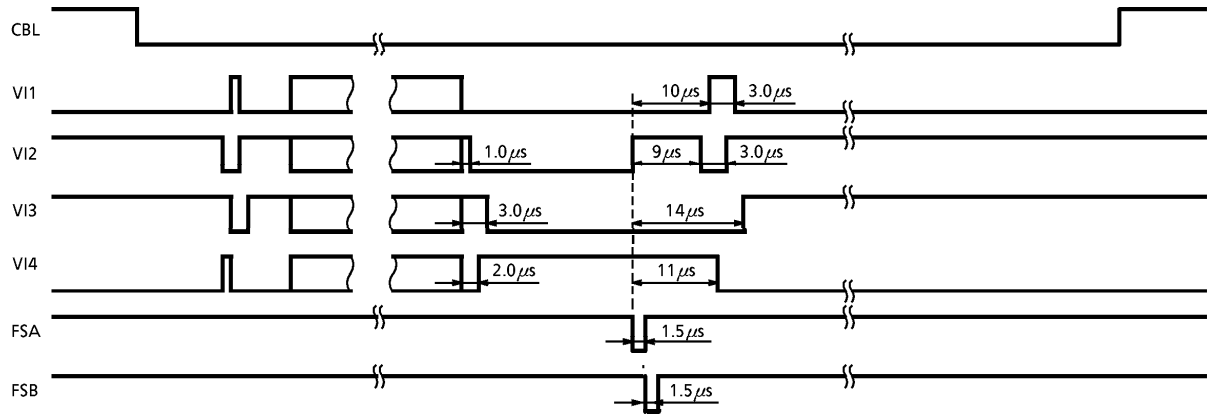
Even Field / Normal Mode



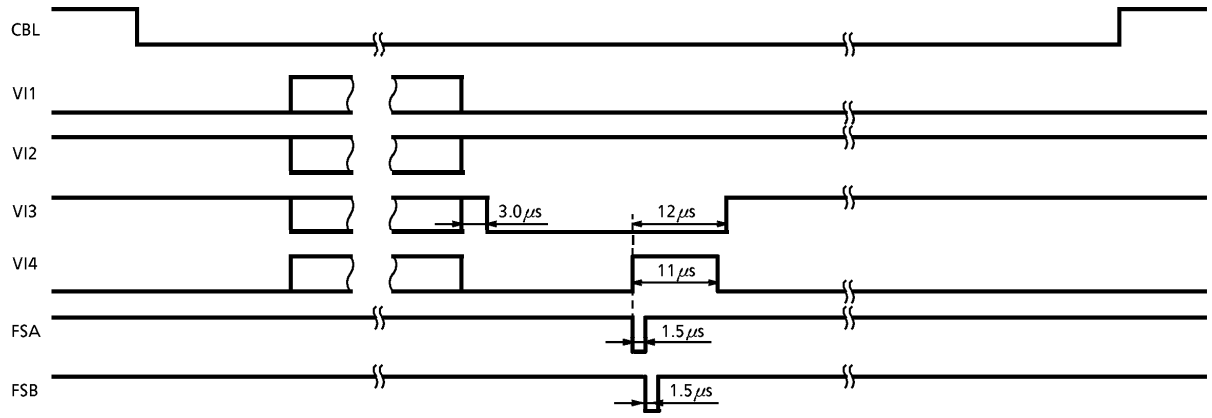
PAL – plus Mode (EXPANDED) (Field shift part)

Odd Field

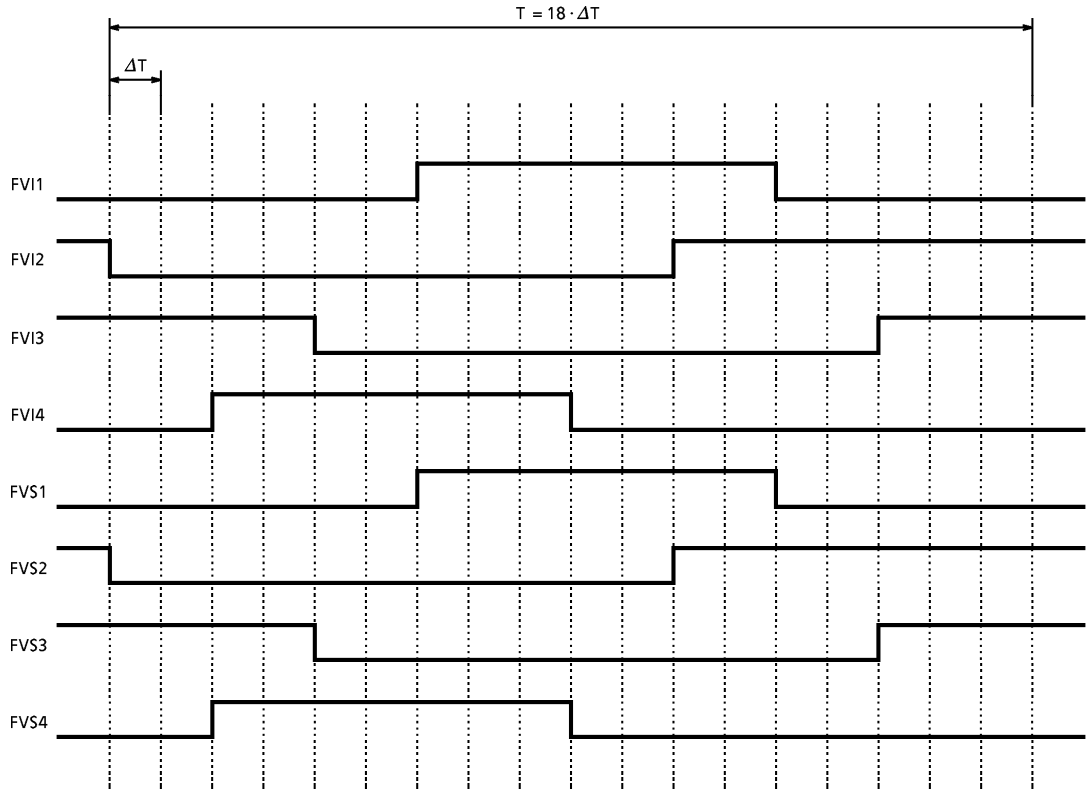
Unit : μs



Even Field



PAL – plus Mode (EXPANDED) (High speed transfer part)



Disuse signal transfer

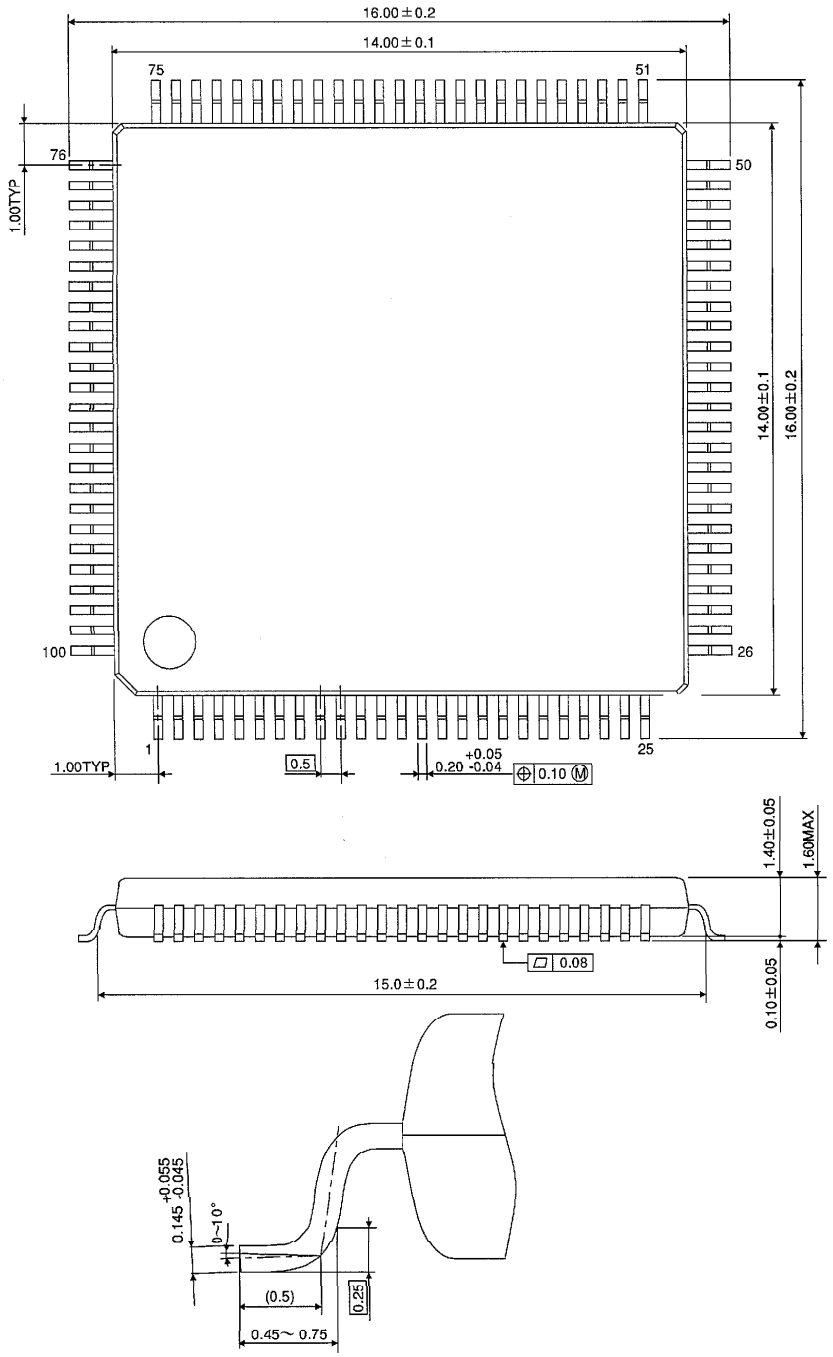
$\Delta T = 44.4$ (ns)

$T = 0.8$ (μs) (1.25MHz)

* Line shift part and H-type timing are same as sweep disable mode.

OUTLINE DRAWING

LQFP100-P-1414-0.50B Unit : mm



Weight : 0.35g (Typ.)