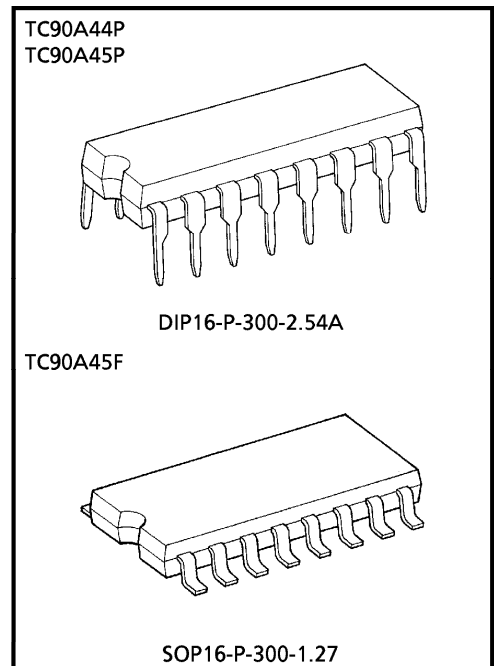


TC90A44P, TC90A45P, TC90A45F**NTSC 2-LINE DIGITAL Y / C SEPARATION IC**

The TC90A44P, TC90A45P/F separates luminance (Y) and chrominance (C) signals from NTSC system composite video signal by using 2 horizontal (H) lines separation. The Y/C separation unit for TV and VCR set is able to assembled at low cost, because it requires few external parts and no adjustment.

FEATURES

- TV system : NTSC
- PLL4 × multiplication circuit
- sync. tip clamping circuit
- Internal 8 bit A/D converter
- Internal 8 bit D/A converters (2 ch.)
- 1 H line memory
- Dynamic comb filter
- Color killer mode (Y/C separation OFF)
- DIP16/SOP16 package
- 5 V single power supply

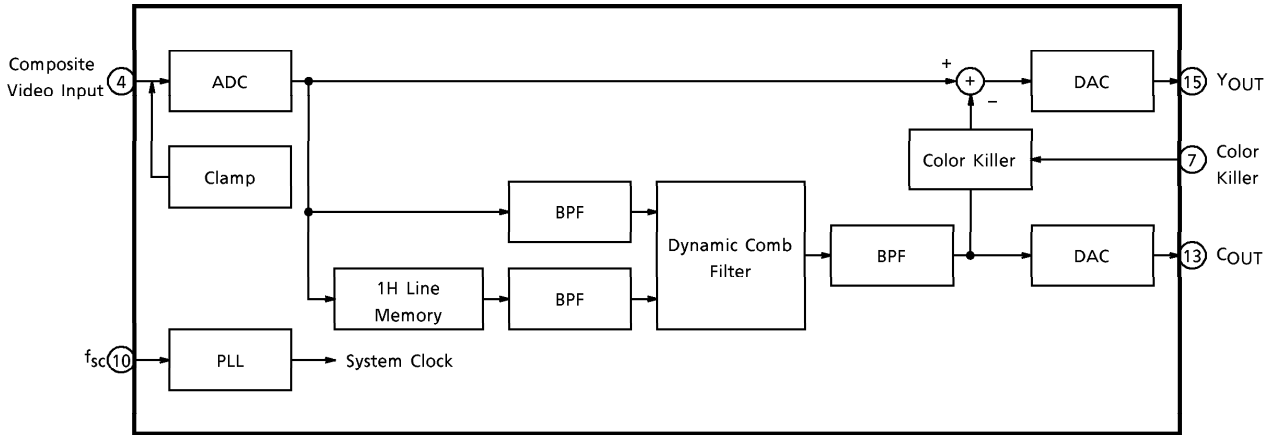
**Weight**

DIP16-P-300-2.54A : 1.00 g (Typ.)
SOP16-P-300-1.27 : 0.18 g (Typ.)

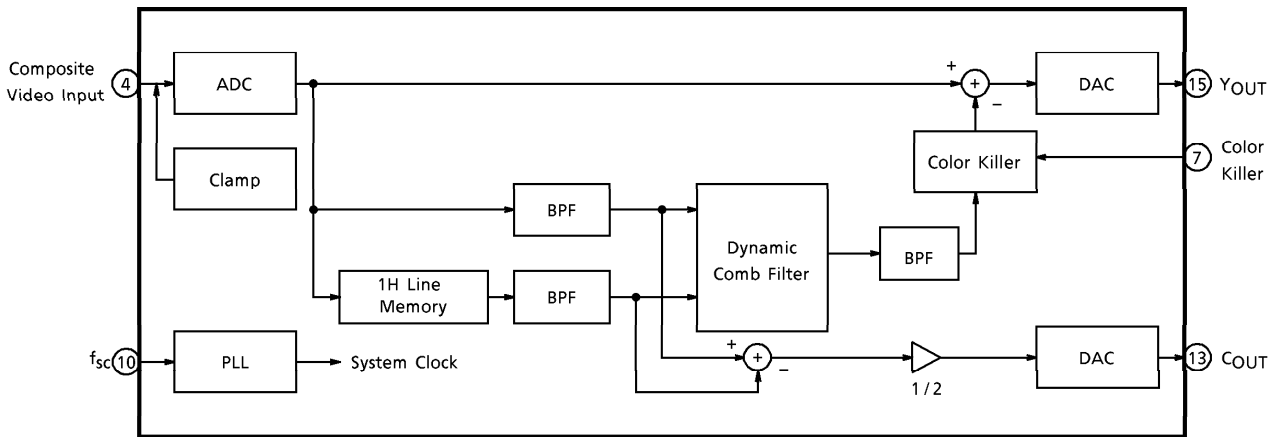
980910EBA1

- TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

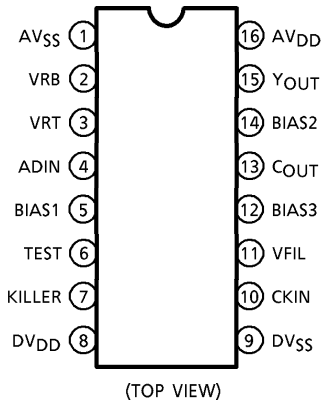
TC90A44P
BLOCK DIAGRAM



TC90A45P / F
BLOCK DIAGRAM

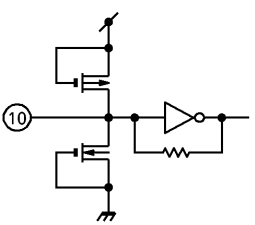
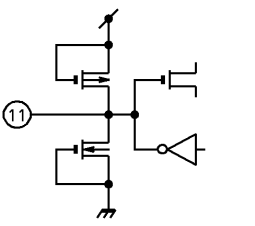
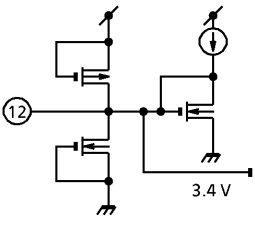
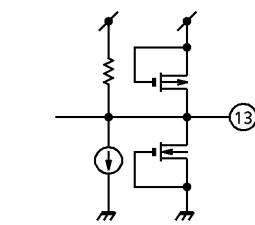
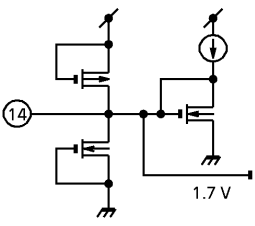
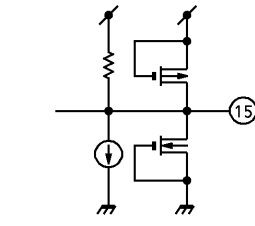


TERMINAL CONNECTION DIAGRAM



TERMINAL FUNCTION

PIN No.	NAME	FUNCTION	I/O	INTERFACE CIRCUIT
1	AV _{SS}	Ground for analog components.	—	—
2	VRB	ADC bias lower limit reference voltage. This defaults internally to approximately 2.25 V, so this pin should normally be connected to ground (AV _{SS}) through a 0.01 μ F capacitor.	—	
3	VRT	ADC bias higher limit reference voltage. This defaults internally to approximately 2.8 V, so this pin should normally be connected to ground (AV _{SS}) through a 0.01 μ F capacitor.	—	
4	ADIN	Composite video signal input.	I	
5	BIAS1	ADC bias voltage. This defaults internally to approximately 1.3 V, so this pin should normally be connected to ground (AV _{SS}) through a 0.01 μ F capacitor.	—	
6	TEST	Test terminal. Normally connected to ground (DV _{SS}).	—	
7	KILLER	This pin is switch for color killer circuit. H : For B/W signal, Y/C separation OFF. L : Normal Y/C separation	I	

PIN No.	NAME	FUNCTION	I/O	INTERFACE CIRCUIT
8	DV _{DD}	Power supply for digital components (+ 5 V).	—	—
9	DV _{SS}	Ground for digital components.	—	—
10	CKIN	Clock input. After applying capacitor for DC cut, input a color-burst-synchronized f_{sc} clock signal to this pin.	I	
11	VFIL	Connect a VCO filter to this pin.	—	
12	BIAS3	DAC bias voltage. This defaults internally to approximately 3.4 V, so this pin should normally be connected to ground (AV _{SS}) through a 0.01 μ F capacitor.	—	
13	C _{OUT}	Chrominance signal output.	O	
14	BIAS2	DAC bias voltage. This defaults internally to approximately 1.7 V, so this pin should normally be connected to ground (AV _{SS}) through a 0.01 μ F capacitor.	—	
15	Y _{OUT}	Luminance signal output.	O	
16	AV _{DD}	Power supply for analog components (+ 5 V)	—	—

FUNCTION BLOCK DESCRIPTIONS**(1) Input clamp (CLAMP)**

This is sync. tip clamp circuit for composite signal.

This circuit makes feedback so that the min. data after A/D converter at Y/C separation equal to internal DC bias level.

(2) A/D converter (ADC)

This is high speed series-parallel 8 bit A/D converter. Recommendable Input level is $0.75 V_{p-p}$ (Sync chip~white 100%).

(3) Line memory

This block is DRAM line memory for 1 H delay.

(4) Band-pass filter (BPF)

This filter extracts the signal of chrominance band from composite video signal. The center frequency is f_{sc} .

(5) Dynamic comb filter (DCF)

This block is logical comb filter to extract the chrominance signal. Filtering logic applies a correlation of two lines to reduce color dot crawl and cross color.

(6) Color killer circuit (KILLER)

This block is applied for black and white (B/W) signal white have no color burst. When pin 10 (KILLER) is "H", logic stop Y/C separation and output composite video signal from pin 14 (Y_{OUT}).

(7) PLL (4 times multiply clock generator)

This block is 4 times multiplier and makes $4f_{sc}$ as system clock.

This block supplies system clock ($4f_{sc}$) to each block via buffer and generates timing signal for memories.

(8) D/A converter (DAC)

This is high speed 8 bit D/A converter. Y output level is $1.73 V_{p-p}$ (Typ.).

C output level is $437 mV_{p-p}$ (Typ.). (Input condition is $0.75V_{p-p}$)

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Power Supply Voltage		V _{DD}	V _{SS} ~V _{SS} + 6.5	V
Input Voltage		V _{IN}	- 0.3~V _{DD} + 0.3	V
Power Dissipation	TC90A44P	P _D (Note)	600	mW
	TC90A44F		440	
Storage Temperature		T _{stg}	- 55~125	°C

(Note) : Ta = 70°C

RECOMMENDED OPERATING CONDITION

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Power Supply Voltage	V _{DD}	—	4.75	5.00	5.25	V
Input Voltage	V _{IN}	—	0	—	V _{DD}	V
Operating Temperature	T _{opr}	—	- 10	—	70	°C

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (Ta = 25°C, V_{DD} = 5 V)

CHARACTERISTIC		SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Power Supply Voltage		V _{DD}	1	CLOCK = 3.579545 MHz V _{IN} = 0.75 V _{p-p}	4.75	5.00	5.25	V
Supply Current		I _{DD}	1		45	60	75	mA
Output Voltage Level		Y _{OUT}	1		3.55	3.70	3.85	V
		C _{OUT}			3.70	3.85	4.00	
Terminal Voltage Level		VRB	1		2.15	2.25	2.35	V
		VRT			2.7	2.8	2.9	
		ADIN			2.35	2.45	2.55	
		BIAS1			1.0	1.3	1.7	
		BIAS2			1.2	1.7	2.1	
		BIAS3			3.0	3.4	4.0	
		VFIL			1.2	1.9	3.0	
		CKIN			1.8	2.3	2.8	
Input Voltage	High Level	V _{IH}	1		4	—	—	V
	Low Level	V _{IL}	1		—	—	1	V

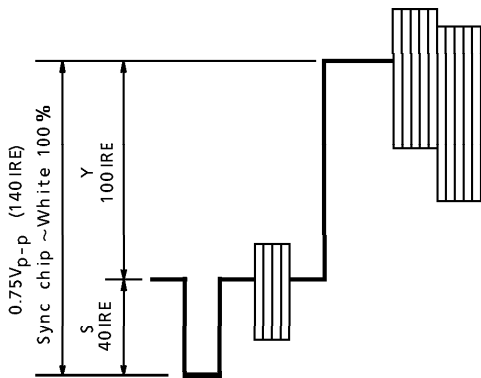
AC CHARACTERISTICS

(1) Y output (Ta = 25°C, VDD = 5 V, input clock : 3.579545 MHz 0.4 Vp-p, S1 = 1)

CHARACTERISTICS		SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Level		VIN	1	0~140 IRE	—	0.75	—	Vp-p
Low Frequency Gain		GV	1	S2 = 1, S3 = 1, S4 = 2 VIN = 15.73426 kHz, 0.75 Vp-p, Vdc = 2.5 V	6.8	7.2	7.7	dB
Frequency Response	f2 / f1	MTF1	1	S2 = 1, S3 = 1, S4 = 2 VIN = 0.75 Vp-p, Vdc = 2.5 V	- 0.8	- 1.0	- 2.0	dB
	f4 / f1	MTF2			- 1.5	- 2.0	- 3.0	
Comb Characteristics	f2 / f3	COMBY	1	VIN = 0.75 Vp-p, Vdc = 2.5 V	—	- 46	- 40	dB
Output Impedance		Zo	1	S2 = 2, S4 = 2 VIN = 15.73426 kHz, 0.75 Vp-p, Vdc = 2.5 V $Zo = \frac{V_1 - V_2}{V_2} \times 400$ V1 : S3 = 1, V2 : S3 = 2	250	400	700	Ω

(Note) : f1 = fH = 15.73426 kHz, f2 = fsc = 3.579545 MHz, f3 = fsc + 1 / 2fH = 3.587412 MHz,
f4 = 1 / 3 (4fsc) = 4.772727 MHz

CONDITION OF INPUT SIGNAL



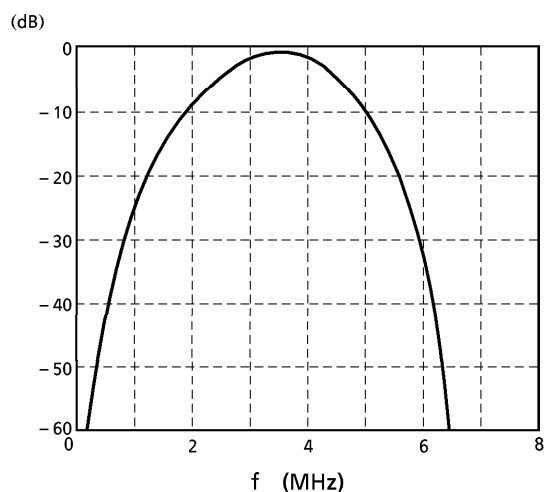
(2) C output ($T_a = 25^\circ\text{C}$, $V_{DD} = 5\text{ V}$, input clock : 3.579545MHz 0.4 V_{p-p}, $S_1 = 2$)

CHARACTERISTICS		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gain		C_V	1	$S_2 = 1, S_3 = 1, S_4 = 1$ $V_{IN} = 0.75 V_{p-p}$	5.7	6.2	6.7	dB
BPF Characteristics	TC90A44P	BWCW	1	$S_2 = 2, S_3 = 1, S_4 = 2$ $V_{IN} = 0.75 V_{p-p}$, $V_{dc} = 2.5\text{ V}$ $(f_{sc} - 503496\text{ Hz}) - (f_{sc})$	-2.5	-1.9	-1.5	dB
	TC90A45P / F				-1.5	-1.3	-1.0	
Comb Characteristics	TC90A44P	COMBC	1	$S_2 = 1, S_3 = 1, S_4 = 2$ $V_{IN} = 0.75 V_{p-p}$, $V_{dc} = 2.5\text{ V}$	—	-38	-35	dB
	TC90A45P / F				—	-46	-40	
Differential Gain		DG	1	$S_2 = 1, S_3 = 1, S_4 = 1$ Modulated lamp signal 140 IRE : 0.75 V	0	2	5	%
Differential Phase		DP			0	2	5	°
Output Impedance		Z_o	1	$S_2 = 2, S_4 = 2$ $V_{IN} = 15.73426\text{ kHz}$, 0.75 V _{p-p} , $V_{dc} = 2.5\text{ V}$ $Z_o = \frac{V_1 - V_2}{V_2} \times 400$ $V_1 : S_3 = 1, V_2 : S_3 = 2$	250	400	700	Ω

(3) PLL circuit characteristics

CHARACTERISTICS	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Pull-In Frequency Range	fck	1	—	3.5	3.6	3.7	MHz
Input Amplitude (f _{sc} Components)	Vck	1	—	0.35	0.5	—	V _{p-p}

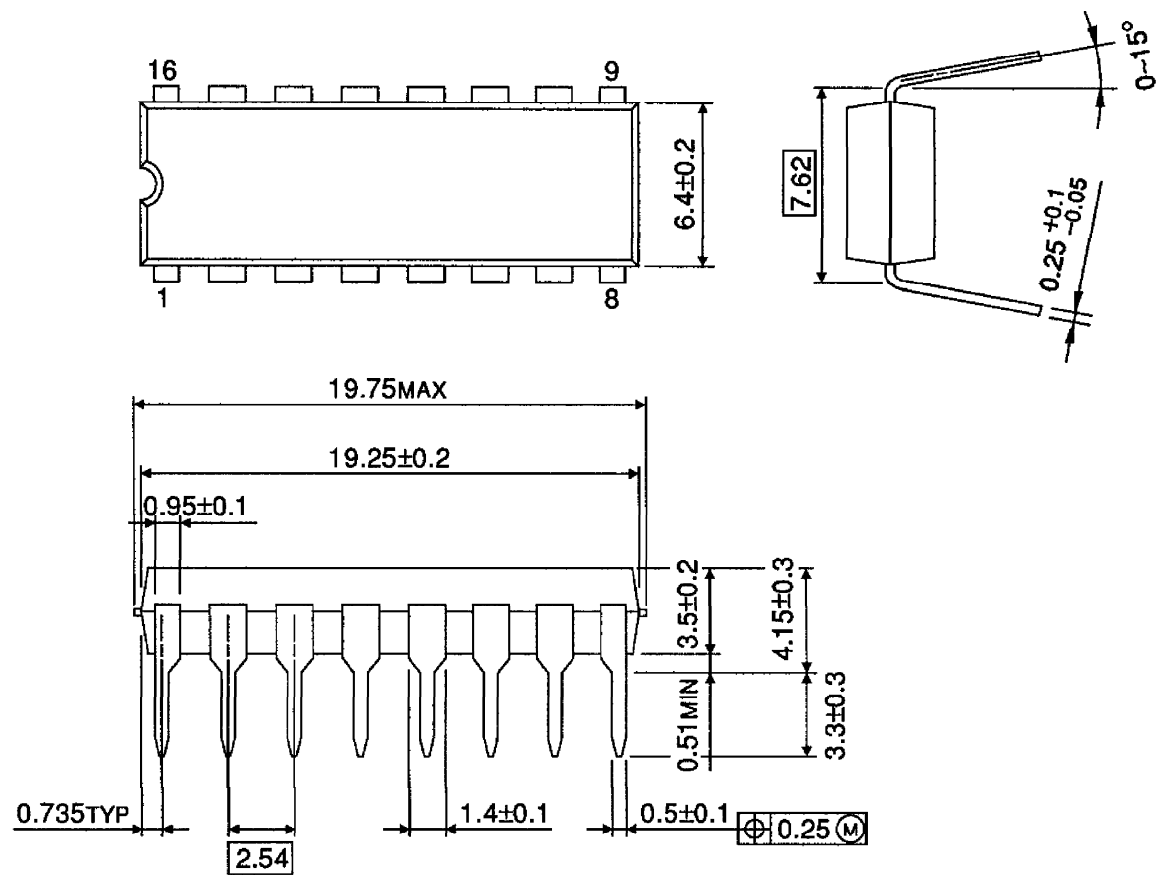
BPF CHARACTERISTICS OF COLOR SIGNAL OUTPUT (TC90A45P / F)



1 : ANALOG GND
 2 : DIGITAL GND

PACKAGE DIMENSIONS
DIP16-P-300-2.54A

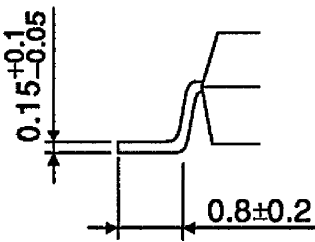
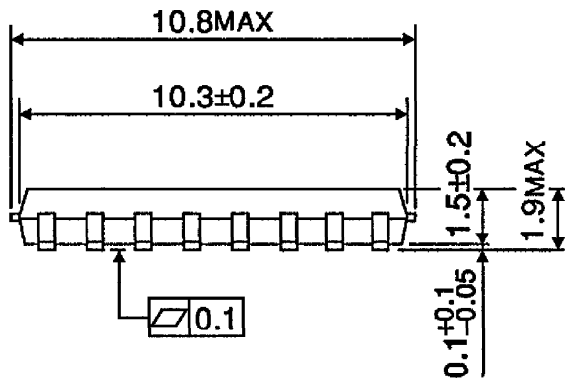
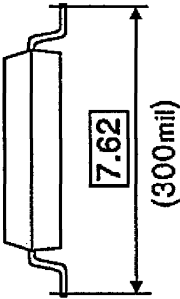
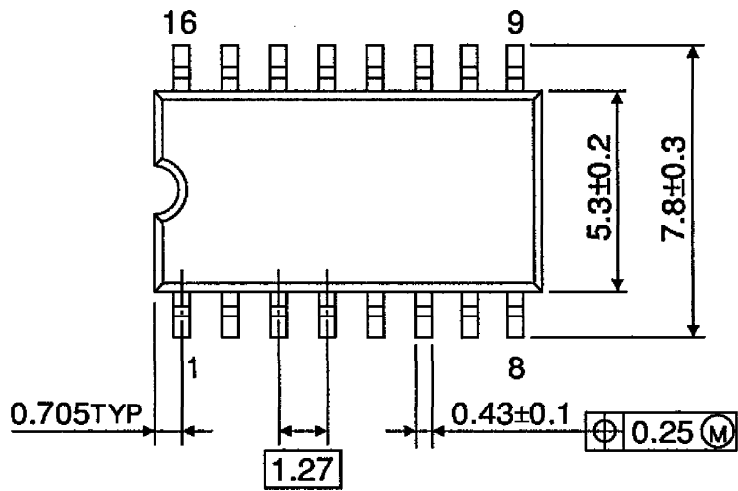
Unit : mm



Weight : 1.00 g (Typ.)

PACKAGE DIMENSIONS
SOP16-P-300-1.27

Unit : mm



Weight : 0.18 g (Typ.)