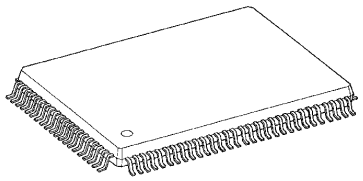
TENTATIVE TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC90A36F

FIELD DOUBL-SCAN CONVERTER IC FOR A MULTI-STANDARD COLOR TV

TC90A36F converts YUV signals with 50Hz or 60Hz of fv (Vertical Frequency) into YUV signals with 100Hz or 120Hz of fv with a field doubling method. TC90A36F includes two channels of A / D converter, three channels of D / A converter, an interface for an external FIFO memory, a clamp circuit for Y signal input and so on. A field doubling system can be completed with TC90A36F, VCOs and a 4 Meg FIFO memory.



QFP100-P-1420-0.65A

Weight : 1.6g (Typ.)

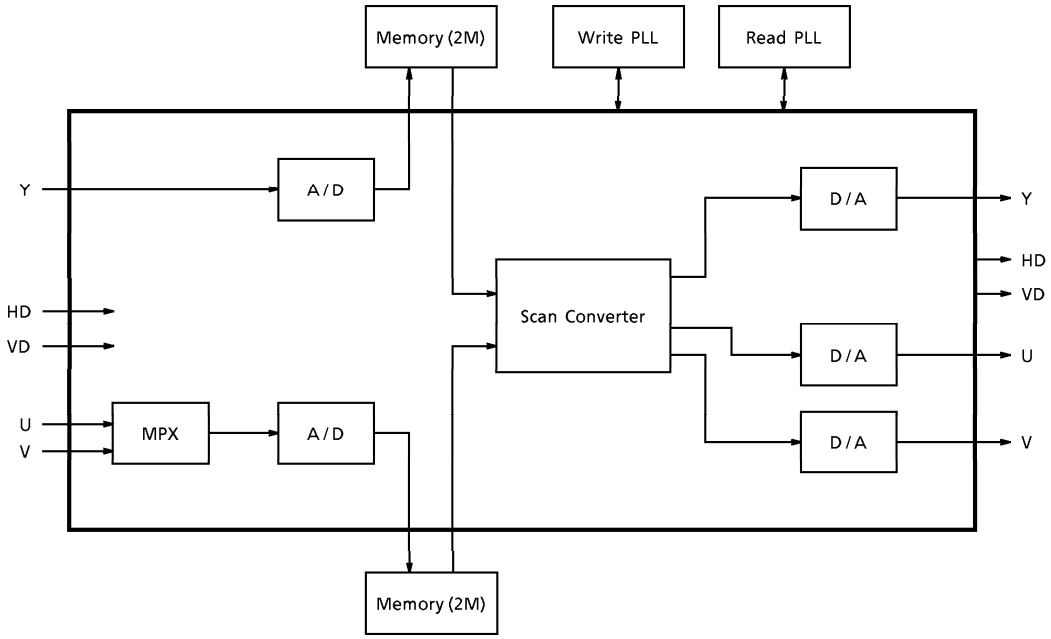
FEATURES

- Scan frequency converter

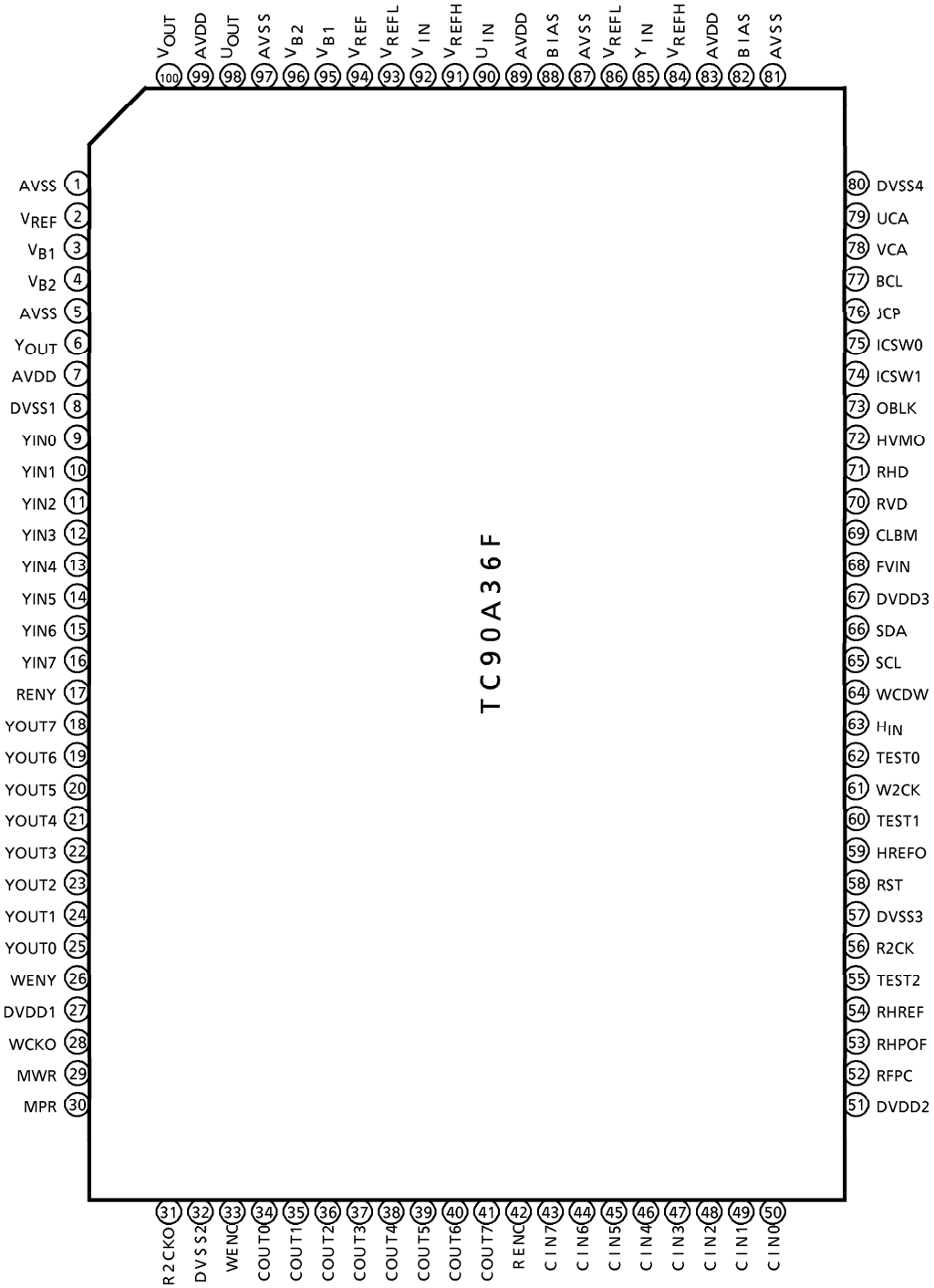
  for PAL system 15.625kHz / 50.00Hz→31.250kHz / 100.00Hz

  for NTSC system 15.734kHz / 59.94Hz→31.468kHz / 119.88Hz
- Horizontal time compression and expansion for a wide screen TV
- Picture freeze mode
- Two channels of 8-bit A / D converter
- Three channels of 8-bit D / A converter
- I^2C bus interface
- Power supply voltage : 5V

BLOCK DIAGRAM



PIN CONNECTION



PIN FUNCTION
(100-pin FP)

PIN No.	PIN NAME	I / O	FUNCTION
1	AVSS	—	V_{SS} (Y DAC)
2	V_{REF}	—	V_{REF} (Dynamic range setting)
3	V_{B1}	—	Bias 1 (Y DAC)
4	V_{B2}	—	Bias 2 (Y DAC)
5	AVSS	—	V_{SS}
6	Y_{OUT}	—	Y Signal Output (Y DAC)
7	AVDD	—	Power Supply Voltage (5V ± 5%) (Y DAC)
8	DVSS1	—	Digital V_{SS}
9	YIN0	I	Y Signal Input (LSB) (from Y field memory)
10	YIN1	I	Y Signal Input (from Y field memory)
11	YIN2	I	Y Signal Input (from Y field memory)
12	YIN3	I	Y Signal Input (from Y field memory)
13	YIN4	I	Y Signal Input (from Y field memory)
14	YIN5	I	Y Signal Input (from Y field memory)
15	YIN6	I	Y Signal Input (from Y field memory)
16	YIN7	I	Y Signal Input (MSB) (from Y field memory)
17	RENY	O	Read Enable Output
18	YOUT7	O	Y Signal Output (MSB) (to Y field memory)
19	YOUT6	O	Y Signal Output (to Y field memory)
20	YOUT5	O	Y Signal Output (to Y field memory)
21	YOUT4	O	Y Signal Output (to Y field memory)
22	YOUT3	O	Y Signal Output (to Y field memory)
23	YOUT2	O	Y Signal Output (to Y field memory)
24	YOUT1	O	Y Signal Output (to Y field memory)
25	YOUT0	O	Y Signal Output (LSB) (to Y field memory)
26	WENY	O	Write Enable Output
27	DVDD1	—	Digital Power Supply Voltage (5V ± 5%)
28	WCKO	O	Clock Output
29	MWR	O	Write Reset Output
30	MRR	O	Read Reset Output
31	R2CKO	O	Clock Output
32	DVSS2	—	Digital GND
33	WENC	O	Write Enable Output
34	COUT0	O	C Signal Output (LSB)
35	COUT1	O	C Signal Output
36	COUT2	O	C Signal Output
37	COUT3	O	C Signal Output

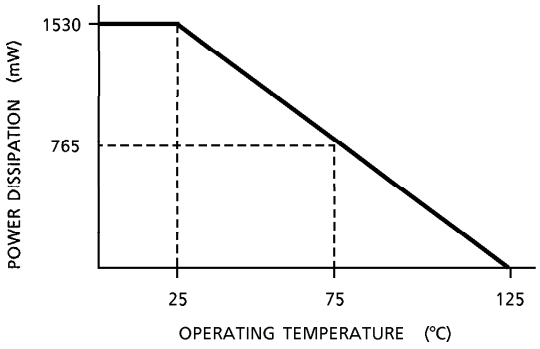
PIN No.	PIN NAME	I/O	FUNCTION
38	COUT4	O	C Signal Output
39	COUT5	O	C Signal Output
40	COUT6	O	C Signal Output
41	COUT7	O	C Signal Output (MSB)
42	RENC	O	Read Enable Output
43	CIN7	I	C Signal Input (MSB)
44	CIN6	I	C Signal Input
45	CIN5	I	C Signal Input
46	CIN4	I	C Signal Input
47	CIN3	I	C Signal Input
48	CIN2	I	C Signal Input
49	CIN1	I	C Signal Input
50	CIN0	I	C Signal Input (MSB)
51	DVDD2	—	Digital Power Supply Voltage (5V ± 5%)
52	RFPC	O	Phase Comparison Error Output
53	RHPOF	O	Horizontal APC Off Control Output
54	RHREF	O	H Reference Output for AFC (1950fH)
55	TEST2	I	Test Pin2
56	R2CK	I	Clock Input
57	DVSS3	—	Digital GND
58	RST		System Reset Input
59	HREFO	O	H Reference Output for AFC
60	TEST1	I	Test Pin1
61	W2CK	I	Clock Input
62	TEST0	I	Test Pin0
63	H_{IN}	I	Horizontal Synchronous Signal Input
64	WCDW	O	1/2 Divider ON/OFF Control Output
65	SCL	O	I^2C Bus Clock Input
66	SDA	I/O	I^2C Bus Data I/O
67	DVDD3	—	Digital Power Supply Voltage
68	FVIN	I	Vertical Synchronous Input
69	CLBM	O	Black Peak Mask Clamp Pulse Output
70	RVD	O	Vertical Drive Output
71	RHD	O	Horizontal Drive Output
72	HVMO	O	VSM Mask Signal Input
73	OBLK	O	External Blanking Output
74	ICSW1	O	Latter-stage Clamp Pulse Output
75	ICSW0	O	Test
76	JCP	O	Caption Position Timing Output

PIN No.	PIN NAME	I/O	FUNCTION
77	BCL	O	Clamp Pulse Output (Y/U/V)
78	VCA	O	Clamp Output (V)
79	UCA	O	Clamp Output (V)
80	DVSS4	—	Digital V_{SS}
81	AVSS	—	V_{SS} (Y ADC)
82	BIAS	—	Bias (Y ADC)
83	AVDD	—	Power Supply Voltage (5V ± 5%) (Y ADC)
84	V_{REFH}	—	V_{REFH} (Y ADC)
85	Y_{IN}	—	Input
86	V_{REFL}	—	V_{REFL} (Y ADC)
87	AVSS	—	V_{SS} (C (U/V) ADC)
88	BIAS	—	Bias (C (U/V) ADC)
89	AVDD	—	Power Supply Voltage (5V ± 5%) (C (U/V) ADC)
90	UIN	—	U Signal Input
91	V_{REFH}	—	V_{REFH} (C (U/V) ADC)
92	V_{IN}	—	V Signal Input
93	V_{REFL}	—	V_{REFL} (C (U/V) ADC)
94	V_{REF}	O	V Signal Input C (U/V) DAC Reference voltage input (Dynamic range setting)
95	V_{B1}	—	Bias 1 (C (U/V) ADC)
96	V_{B2}	—	Bias 2 (C (U/V) ADC)
97	AVSS	—	V_{SS} (C (U/V) ADC)
98	U_{OUT}	O	U Signal Output
99	AVDD	—	Power Supply Voltage (5V ± 5%) (C (U/V) ADC)
100	V_{OUT}	O	V Signal Output

MAXIMUM RATINGS (Ta = 25°C)

ITEM	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{DD}	−0.3~7	V
Input Voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Power Dissipation	P_D (Note)	1530	mW
Storage Temperature	T_{stg}	−40~125	°C

(Note) When using the device at above Ta = 25°C, decrease the power dissipation by 15.3mW for each increase of 1°C, as below, when mounted on a PCB.



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Power Supply Voltage	V_{DD}	—	4.75	5	5.25	V
Input Voltage	V_{IN}	—	0	—	V_{DD}	V
Operating Temperature	T_{opr}	—	−20	—	70	°C

DC CHARACTERISTICS (unless otherwise specified, Ta = 25°C, V_{DD} = 5.0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Power Dissipation	I_{DD}	V_{DD} = 5.0V		—		mA
High-level Input Voltage 1 (*1)	V_{IH1}		3.5	—	—	V
High-level Input Voltage 2 (*2)	V_{IH2}		4	—	—	V
High-level Input Voltage 3 (*3)	V_{IH3}		2.4	—	—	V
Low-level Input Voltage 1 (*1)	V_{IL1}			—	1.5	V
Low-level Input Voltage 2 (*2)	V_{IL2}			—	1	V
Low-level Input Voltage 3 (*3)	V_{IL3}			—	0.8	V
High-level Input Current	I_{IL}		− 10	—	10	μA
Low-level Input Current	I_{IH}		− 10	—	10	μA
High-level Output Voltage (*4)	V_{OH}	I_{OH} = − 4mA	2.4	—	—	V
		I_{OH} = − 1.0μA	V_{DD} − 0.05	—	—	
Low-level Output Voltage (*4)	V_{OL}	I_{OL} = + 4mA	—	—	0.4	V
		I_{OH} = 1.0μA	—	—	0.05	

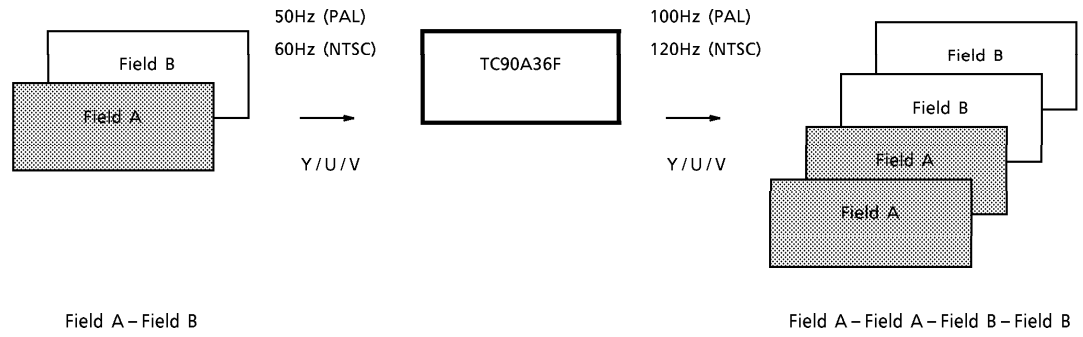
(*1) CMOS input : TEST2, RST, TEST1, TEST0, HIN
(*2) CMOS Schmitt input : SCL, SDA
(*3) TTL input : YIN0-7, CIN7-0, R2CK, W2CK, FVIN
(*4) Output : RENY, YOUT7-0, WENY, WCKO, MWR, MRR, WENC, COUT0-7, RENC, RFPC, RHPOF, RHREF, HREFOWCDW, CLBM, RVD, RHD, HVMO, OBLK, ICSW1, ICSW0, JCP, BCL, VCA, UCA, YCA

AC CHARACTERISTICS (unless otherwise specified, Ta = 25°C, V_{DD} = 5.0V)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	MIN	TYP.	MAX	UNIT	NOTE
Input Setup Time	Ts1	—	0	—	—	ns	RENY, RENC for R2CKO rising-up edge
	Ts2	—	0	—	—		MRR for R2CKO rising-up edge
	Ts3	—	25	—	—		WENY, WENC for WCKO rising-up edge
	Ts4	—	25	—	—		MWR for WCKO rising-up edge
	Ts5	—	12	—	—		YOUT, COUT for WCKI rising-up edge
	Ts6	—	5	—	—		YIN, CIN for R2CKO rising-up edge
Input Hold Time	Th1	—	5	—	—	ns	RENY, RENC for R2CKO rising-up edge
	Th2	—	10	—	—		MRR for R2CKO rising-up edge
	Th3	—	20	—	—		WENY, WENC for WCKO rising-up edge
	Th4	—	20	—	—		MWR for WCKO rising-up edge
	Th5	—	30	—	—		YOUT, COUT for WCKI rising-up
	Th6	—	6	—	—		YIN, CIN R2CKO rising-up

FUNCTIONS

TC90A36F converts 50-Hz PAL YUV signals to 100Hz; 60-Hz NTSC YUV signals to 120Hz.



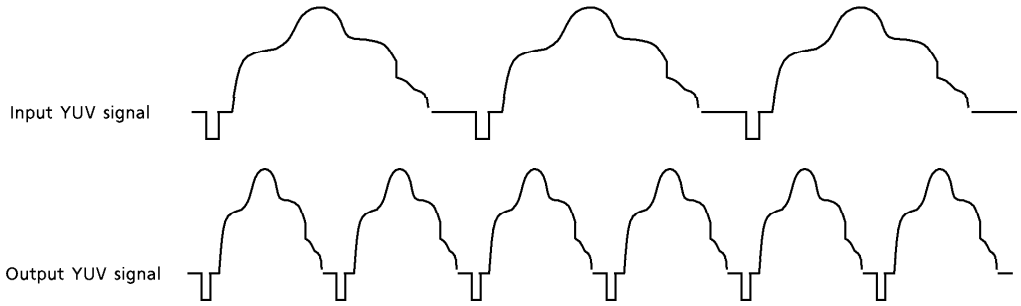


Figure Output signal image

The relation between input and output signals is as follows :

	INPUT SIGNAL	OUTPUT SIGNAL
PAL	15.625kHz / 50.00Hz	31.250kHz / 100.0Hz
NTSC	15.734kHz / 59.94kHz	31.648kHz / 119.88Hz

The number of output lines is as shown below :

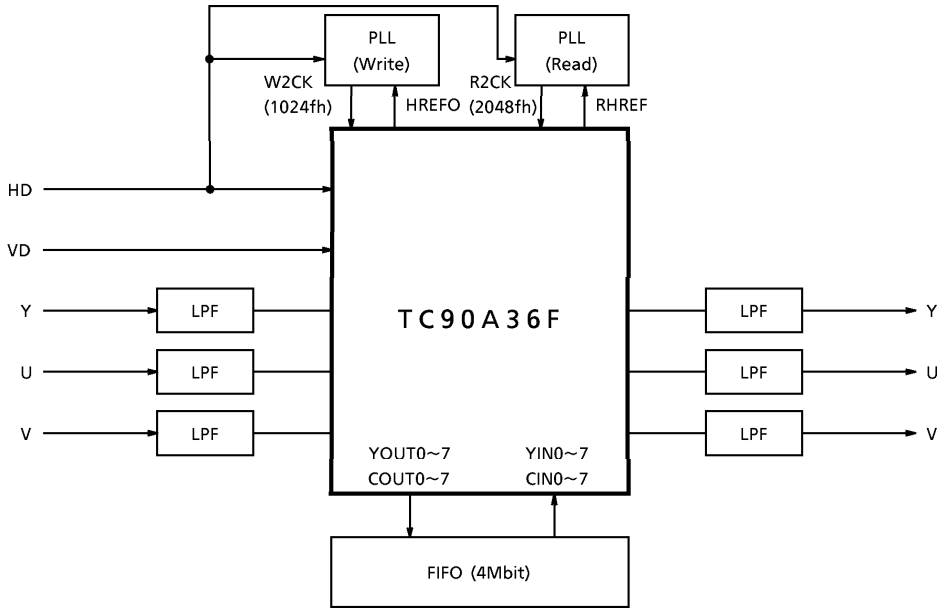
Standard signal	PAL	Repetition of 312H – 312.5H – 313H – 312.5H
	NTSC	Repetition of 262H – 262.5H – 263H – 262.5H
Non-standard signal	Repetition of [frame cycle × 1 / 2 (below 1H truncated)] – [field cycle × 2 frame cycles × 1 / 2 (below 1H truncated)] Example : Repetition of 262H 262H – 262H – 262H – 262H Repetition of 262H – 263H 262H – 262H – 262H – 264H	

(*) TC90A36F does not support a function for doubling the number of lines in a field.

GENERATION OF DOUBLE-SCAN CLOCK

For double-scan conversion, the clock used to read data needs double the frequency of the clock used to write data in memory.

TC90A36F controls for write input HD signal and phase compare AFC. For read, to avoid skew in the upper screen, TC90A36F controls the frequency compare AFC. Thus, a separate PLL VCO is required for read and write.



[External IC]

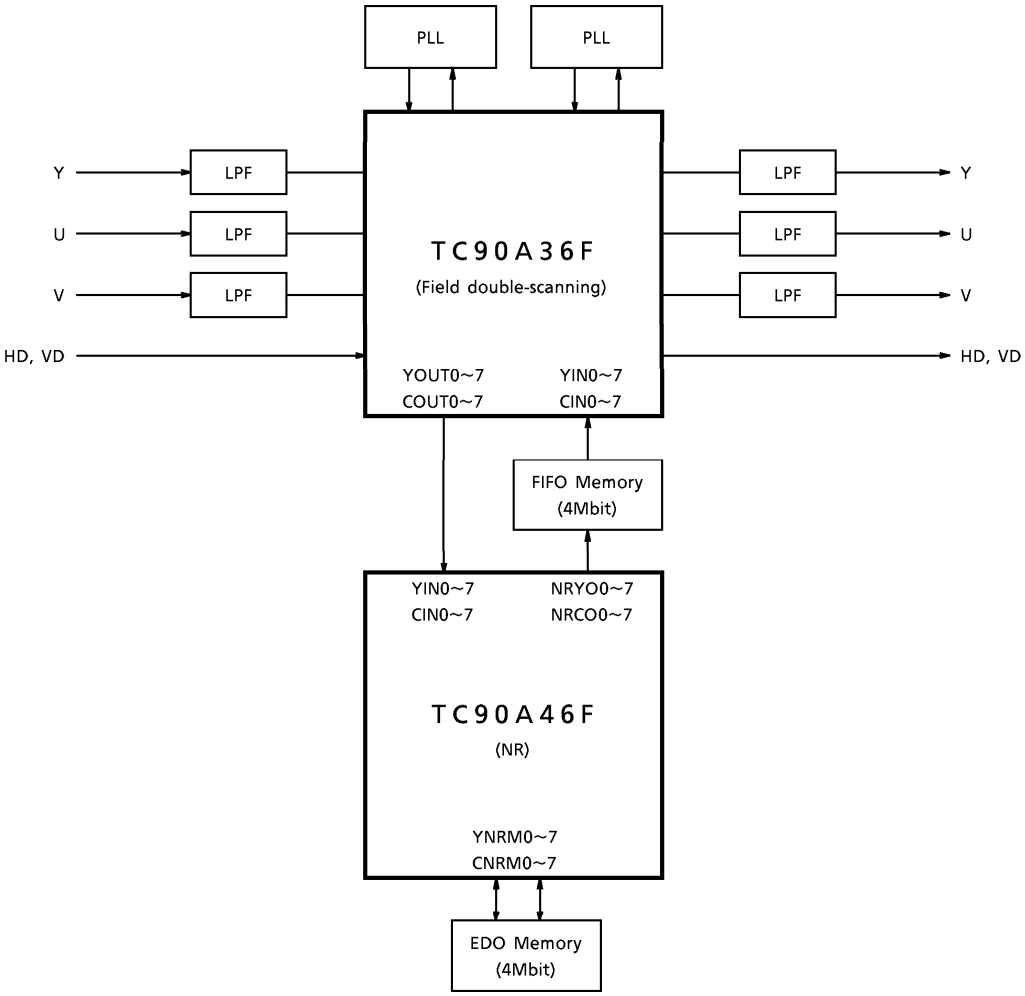
VCO IC for clock PLL×1 for read and×1 for write

TLC29321 by Texas Instruments

Field memory

MSM518221×2 by Oki

Combining an IC for noise reduction adds an NR function in addition to field double-scanning.



HOW TO SET FIELD DOUBLE-SCAN CONVERSION

TC90A36F performs field double-scan conversion by reading data written to field memory using a clock. Set the read clock to a frequency double that of the write clock.

HOW TO SET FREQUENCY OF READ / WRITE CLOCKS

[Sub-address 00HEX, WHCNT (write AFC horizontal divider ratio)]

Use the above register to set the clock used to write data to memory.

The write clock frequency Fwck is determined as follows :

$$Fwck = (WHCNT + 1) \times 2 \times fh$$

For example, setting WHCNT = 1FF HEX,

WHCNT + 1 = 1FF HEX + 1 HEX = 512

Fwck = 512 × 2 × fh = 1024fh = 16MHz (PAL).

If the picture is not compressed, set to the same frequency as that in RHACNT (read horizontal AFC divider ratio), sub-address 07 HEX.

If the picture is compressed (wide-screen display with 4:3 aspect ratio), depending on the compression ratio, set a value which is smaller than the uncompressed value.

[Sub-address 07 HEX, RHACNT (read horizontal counter divider ratio)]

In nomal Double Scan mode, set to the same as that in RHACNT.

[Sub-address 07 HEX, RHACNT (read horizontal AFC divider ratio)]

Use the above register to set the clock frequency used to read data from memory.

In Double Scan mode, set to the same as that in WHCNT.

The read clock frequency Frck is determined as follows :

$$Frck = (RHACNT + 1) \times 4 \times fh$$

For example, setting RHACNT = 1FF HEX,

1FF HEX + 1 HEX = 200 HEX = 512

Frck = 256 × 4 × 16.852kHz = 32MHz (PAL).

INPUT / OUTPUT INTERFACE

TC90A36F incorporates a two-channel 8-bit AD converter for Y and C (U / V) signals and a three-channel 8-bit DA converter for YUV signal output.

(1) Input interface

Input data are the YUV signal and HD and VD pulses for timing. The input dynamic range of the AD converter is from 1.5 to 3.5V. The sampling rate is 1024fh.

The Y signal is clamped in the built-in clamp circuit. The clamp level is 32 LSB. The UV signal is clamped externally using the level error output (UCA, VCA) and timing signal (BCL). The clamp level in the IC is 128 LSB.

Input the horizontal timing signal HD (pin 63 : H_{IN}) with positive polarity.

For the vertical signal VD (pin 68 : FVIN), set the polarity in the I^2C bus register (VINP, sub-address : 00HEX).

(2) Output interface

The DA converter for the YUV signal operates at 2048fh clock for PAL. Set the output dynamic range for the Y signal using pin 2; for the UV signal, using pin 94. Obtain 4V using resistance division (for example : 15kΩ to 3.8kΩ) between power supplies and input (voltage cannot be less than 3.8V).

Set the Y blanking level using register YBLL (sub-address : 22 HEX). (Normally, same as the input clamp level, 32 LSB.)

Set the C blanking level using register CBLL (sub-address : 23 HEX). (Normally, same as the input clamp level, 128 LSB.)

Control picture mute using register MUTE (sub-address : 23 HEX). At mute, fixed to the blanking level.

The IC features a function for adding a side panel. The side panel level can be varied using the Y signal only (YSPL at sub-address : 22 HEX). Set the timing by setting to the first part of H blanking using register HSPS (sub-address : 15 HEX); reset the timing by setting to the latter part of H blanking using register HSPR (sub-address : 16 HEX). If a side panel is not added to the output picture, set the output level to the same as the Y blanking level and set the timing to other than the picture period.

(3) Timing signals

The IC outputs timing signals necessary for field double-scanning.

RVD (pin 70) Verstical drive timing signal output. Set the polarity in RVDP (sub-address : 17 HEX).

RHD (pin 71) Horizontal drive timing signal output. Set the polarity in PRHD and the pulse width in RHDW (sub-address : 9 HEX).

HVMO (pin 72) Mask signal output for speed modulation off. Set the horizontal timing in HVMOS (sub-address : 13 HEX) and HVMOR (sub-address : 14 HEX).

OBLK (pin 73) Blanking signal output. Set the horizontal timing in OHBLS (sub-address : F HEX) and OHBLR (sub-address : 10 HEX). Set the vertical timing in OVBLS (sub-address : 1C HEX) and OVBLR (sub-address : 1D HEX).

ICSW1 (pin 74) Clamp pulse output at latter stage. Set the pulse width in ALCW and the phase in ACLP (sub-address : CHEX).

CLBM (pin 69) Black peak mask signal output. Set the horizontal timing in HBMS (sub-address : 11 HEX) and HBMR (sub-address : 12 HEX). Set the vertical timing in VBMS (sub-address : 1E HEX) and VBMR (sub-address : 1F HEX).

JCP (pin 76) General-purpose port for vertical timing signal. Set timing in JCPS (sub-address : 20 HEX) and JCPR (sub-address : 21 HEX).

I^2C BUS FUNCTIONS

As the interface for controlling operation, TC90A36F uses the I^2C bus standard defined by Philips. The I^2C bus specifications are used for performing data transmission between ICs using a common serial bus in a system consisting of multiple ICs. TC90A36F is designed to operate on the I^2C bus.

1. Outline

The I^2C bus consists of two lines : SCL and SDA.

Data are transferred on the SDA line in units of 8bits in sync with the clock for the SCL line. Transfer start and end are controlled by changing SDA when the SCL line is at high level. Acknowledge in units of bytes is defined so that when 8-bit data are transferred, 1-bit acknowledge is transferred.

Although the I^2C bus assumes multiple masters, TC90A36F only supports a slave function. Therefore, data are transferred between master and slave (in this case, TC90A36F) all at one time. Transfer start, end, slave selection, and operating mode are all controlled by the then master. Thus, the SCL line is always controlled by the master and the slave (TC90A36F) only inputs. The SDA line is bidirectional. Input and output are switched according to the register address of the slave (TC90A36F). The SDA line is driven by the master or TC90A36F with open drain. The line is pulled up by a pull-up resistor.

The master must control transfer (eg, SDA line input / output switching) depending on the operating mode (read / write) of the slave address (TC90A36F).

2. Address

With the I^2C bus, two 8-bit addresses are allocated to the slaves.

As the I^2C bus register table shows, with TC90A36F, 14 HEX is allocated as the write address; 15 HEX as the read address. In addition, an 8-bit sub-address is set. Data are transmitted by specifying these addresses and sub-address.

3. Data block

As the I^2C bus data, any number of bytes of data can be transferred in units of 8bits. However, with TC90A36F, as the I^2C bus register table shows, only 8bits of data are transferred to both 14 and 15 HEX all at one time.

All TC90A36F registers are static, they hold their values until overwritten. After power on, the slave registers are undefined. Initialize the registers by inputting low level to RST (pin 28).

4. Transfer sequence

4.1 Transfer start and end

Data are transferred in sync with the SCL line. At standby, set both the SCL and SDA lines to high impedance. Because both SCL and SDA lines are pulled up, they are at high level. Data transfer starts if the SDA line falls while the SCL line is at high level. Data transfer ends if the SDA line rises while the SCL line is at high level. During data transfer, such sequences do not occur (see sequences 1 and 2).

4.2 SCL line and SDA line timing

The SDA line data must be valid between the rise and fall of the SCL line. The sure way to send data is for the sender to output data to the SDA line after checking that the SCL line has fallen. Due to this restriction, a start or end sequence does not occur during data transfer.

4.3 Acknowledge

When 8-bit data are correctly received in the write register, TC90A36F sets the SDA line to low level. Detecting this, the master knows that the data are correctly received. If acknowledge remains at high level, data are not correctly received; thus, the master must resend the data.

4.4 Data transmit order

The SDA line has a positive polarity. Data are transferred from the MSB to the LSB of the address.

4.5 Data transmit / receive switch timing

After transferring the 8-bit address, to receive acknowledge, the master sets the SDA line to high impedance after the SCL line falls. TC90A36F outputs acknowledge to the SDA line in sync with the fall of the SCL line. The SDA line reverts to high impedance after the SCL line falls following output of acknowledge.

EXAMPLE OF I²C BUS CONTROL

After power on, first, the master sets the SCL and SDA lines to high impedance.

Then, the master inputs low level to RST (pin 28) of TC90A36F and initializes the device. Low level can be input to RST by external R and C, or a pulse can be input from a microcontroller.

At this point, TC90A36F can be externally controlled. The write register at address 14 HEX is initialized to 00 HEX.

If any slave register initial settings are to be changed, send the initial data.

Transfer is explained in more detail below using an example where data 01 HEX are sent to address 14 HEX and sub-address 22 HEX.

The master outputs high level to the SCL and SDA lines. Then, as the transfer start condition, the master sets the SDA line to low level then the SCL line to low level.

Next, the master transfers an address. Transfer starts from the MSB. As the data string for address 14 HEX, the master sends 00010100 (transfer sequentially from the MSB). To transfer the first bit, the master sets the SDA line to low level, the SCL line to high level then low level. Then, the master sets the SDA line to low level, low level, low level, low level, high level, low level, low level. After each setting, the master sets the SCL line to low level, high level, low level. When the master transfers the 8bits of the address, the master sets the SCL line to high level to check that the acknowledge is low level. After checking, the master sets the SCL line to low level and moves on to transfer the sub-address.

Sub-address transfer starts from the MSB. As the data string for sub-address 22 HEX, the master sends 00100010 (transfer sequentially from the MSB). To transfer the first bit, the master sets the SDA line to low level, the SCL line to high level then low level. Then, the master sets the SDA line to low level, low level, high level, low level, low level, low level, high level, low level. After each setting, the master sets the SCL line to low level, high level, low level. When the master transfers the 8bits of the address, the master sets the SCL line to high level to check that the acknowledge is low level. After checking, the master sets the SCL line to low level and moves on to transfer the data.

The data string of (S) data 01 HEX is 00000001. The master sets the SDA line to low level, low level, low level, low level, low level, low level, low level, high level. After each setting, the master sets the SCL line to low level, high level, low level.

After transferring the 8bits of data, the master sets the SCL line to high level to check that the acknowledge is low level. After checking, the master sets the SCL line to low level. To complete the sequence, the master sets the SDA line to low level, the SCL line to high level, then the SDA line to high level to end the transfer. After that, the master sets both the SCL and SDA lines to high impedance. This is the end of the transfer.

To transfer data to another register, use the same procedure with a different sub-address and data string.

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	NIQM	YCAP	YCAP	CCAP	VINP	VINFOF	VLSOF	WHCNT								

NIQM CMPX polarity Swaps IMX and QMX.

NCCA CCLP UV invert polarity Swaps ICA and QCA for color clamp.
If ICA and QCA are inverted, color clamp does not apply; thus, inverts NCCA. When clamp is applied but I and Q (or U and Y) are inverted, invert both NIQM and NCCA.

YCAP Y clamp output polarity

CCAP C clamp output polarity
Used when clamp control is inverted. So, even if the signal for clamp control has negative polarity, clamp can be applied. The Y clamp level is A/D output fixed level (01000000); therefore, the A/D output Y signal must have positive polarity.

VINP V input signal phase When positive-polarity edge is used : 1
When negative-polarity edge is used : 0

VIFOF V input signal phase On : 1, Off : 0 (Normally on)

VLSOF V latch 1-clock jitter protection circuit V phase
On : 1, Off : 0 (Normally on)

WHCNT Write AFC horizontal divider value
Determines the clock frequency for writing to memory, fwck.
$fwck = (WHCNT + 1) \times 2 \times fh$
Without compression, match with RHACNT; with compression, reduce the value by the compression ratio.

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0						WHENP									

WHENNP Write horizontal enable phase Sets the write horizontal start position.

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2							WHENW									

WHENW Write horizontal enable width Sets the number of write horizontal pixels.
Set so that $WHENW = RHENW \times 2 + 1$

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3	BCLW						BCLP									

BCLW ADC clamp pulse width

BCLP ADC clamp pulse phase

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4			STILL	1			WVPS									

STILL Still 1 : Still screen (halts write to memory)
WVPS Write-read vertical phase reference
Using the write vertical counter as a reference, controls the reset signal phase when double-speed V is generated.

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
5	WYDL					CLVMS	WVENP									

WYDL Write Y phase correction Adjusts the write Y / C delay.
Used together with WCDL for adjusting the write Y / C delay.
CLVMS Clamp V mask 1 : Masks during BCL write V.
WVENP Write vertical enable phase Phase during write V.

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
6	WCDL				PWCN	PMWR	WVENW									

WCDL Write C phase correction Adjusts the write Y / C delay.
PWCN Write enable polarity 0 : Positive polarity, 1 : negative polarity
PMWR Write reset polarity 0 : Positive polarity, 1 : negative polarity
WVENW Write vertical enable width Width during write V

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7	RHCNT								RHACNT							

RHCNT RHCNT Read horizontal AFC divider width
Read horizontal counter divider ratio.
For field double scan, set to the same value as that of RHACNT at sub address 07HEX.
RHCNT Read horizontal counter divider value
Determines the read clock frequency frck.
$frck = (RHACNT + 1) \times 4 \times fh$

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
8		RHACNT		RHCNT				RHIR								

RHIR VD interlace phase
Sets the interlace position in the VD even field.
The typical value is RHACNT / 2.

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
9						RHFRON	RHVRON	MDHD	MDHR	PRHD	RHDW					

RHFRON Horizontal frame phase matching switch 0 : fix
RHVRON Horizontal field phase matching switch 0 : fix
MDHD Read horizontal counter reset switch 1 : fix
MDHR Read horizontal counter pull-in switch 1 : fix
PRHD RHD polarity 0 : Positive polarity, 1 : negative polarity
RHDW RHD width

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A								RHENP								

RHENP Read horizontal enable phase Sets the read horizontal start position.

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B								RHENW								

RHENW Read horizontal enable width Sets the number of read horizontal pixels.

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C	ALCW						ACLP									

ALCW Output clamp width
ACLP Output clamp phase

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D								IHBLS								

IHBLS Internal horizontal blanking setting

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E								IHBLR								

IHBLR Internal horizontal blanking resetting

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F								OHBLS								

OHBLS Output horizontal blanking setting

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
10								OHBLR								

OHBLR Output horizontal blanking resetting

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
11								HBMS								

HBMS Horizontal black peak mask setting

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
12								HBMR								

HBMR Horizontal black peak mask resetting

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
13	IVBOF	OVBOF	VBMOF	RVEOF				HVMOS								

IVBOF	IVBLK OFF	0 : Normal	0 : Off
OVBOF	OVBLK OFF	0 : Normal	0 : Off
VBMOF	VMASK OFF	0 : Normal	0 : Off
RVEOF	R-VEN OFF	0 : Normal	0 : Off
HVMOS	Horizontal VSM OFF setting	(1024fH Unit)	

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
14	IHBOF	OHBOF	HBMOF	RHEOF	ACLS	PREN		HVMOR								

IHBOF	Internal horizontal blanking off	0 : Normal	1 : Off
OHBOF	Output horizontal blanking off	0 : Normal	1 : Off
HBMOF	Horizontal black peak mask off	0 : Normal	1 : Off
RHEOF	Read horizontal enable off	0 : Normal	1 : Off
ACLS	Clamp / black peak mask separate output switch	fix 1	
PREN	Read enable polarity	0 : Positive polarity	1 : Negative polarity
HVMOR	Horizontal VSM OFF resetting	(1024fH Unit)	

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
15	RYDL							HSPS								

RYDL Read Y phase correction
HSPS Horizontal side panel phase setting

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
16	RCDL							HSPR								

RCDL Read C phase correction
HSPR Horizontal side panel phase resetting

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
17				VWHM	PRVD	PMRR		RVDP								

VWHM Double scan V mode
PRVD RVD polarity 0 : Positive polarity 1 : Negative polarity
PMRR MRR polarity 0 : Positive polarity 1 : Negative polarity
RVDP RVD phase Vertical Drive output phase setting (1H (32μs) unit)

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
18								RVENP								

RVENP Read vertical enable phase (1H (32μs) unit)

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
19								RVENW								

RVENW Read vertical enable width (1H (32μs) unit)

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1A								IVBLS								

IVBLS Internal vertical blanking setting

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1B								IVBLR								

IVBLR Internal vertical blanking resetting

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1C								OVBLS								

OVBLS Output vertical blanking setting (1H (32μs) unit)

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1D								OVBLR								

OVBLR Output vertical blanking resetting (1H (32μs) unit)

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1E								VBMS								

VBMS Vertical black peak mask setting (1H (32μs) unit)

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1F								VBMR								

VBMR Vertical black peak mask resetting (1H (32μs) unit)

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
20								JCPS								

JCPS Vertical timing signal setting (1H (32μs) unit)

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
21								JCPR								

JCPR Vertical timing signal setting (1H (32μs) unit)

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
22	YSPL							YBLL								

YSPL Y side panel resetting (1024fH unit)
YBLL Y blanking level

Sub Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
23	YCAOUT			MUTE	RHPOF	ICSW1	ICSW0	YDLO	CBLL							

MUTE	Mute control	0 : Normal 1 : Picture Mute
RHPOF	Read PLL phase compare off	
ICSW1		
ICSW0		
YDLO	Y 1-clock delay correction	0 : Normal 1 : 1024fH delay
CBLL	C blanking level	normally 128

EXAMPLE OF I²C BUS SETTINGS

(Note) This is an example of I²C bus settings. For real-world applications, the setting values must be adjusted.

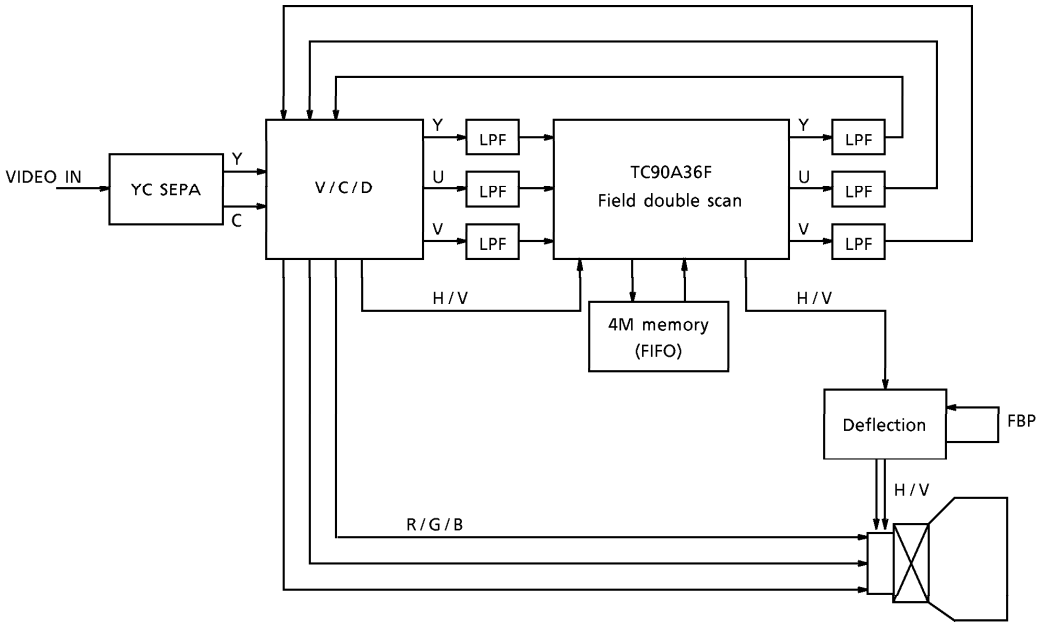
SUB	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	SET VALUE [HEX]
0	CMPX Polarity NIQM	CCLP UV inversion NCCA	YCLP Polarity YCAP	CCLP Polarity CCAP	FVIN Polarity VINP	VFIL OFF VIFOF	V phase OFF VLSOF	Write AFC horizontal divider value WHCNT 8	7	6	5	4	3	2	1	0	
	1	1	1	1	0	0	0	1	1	1	1	1	1	1	1	1	F1FF
1	TEST TSWH1						Write horizontal enable phase WHENP 9	8	7	6	5	4	3	2	1	0	
	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0066
2							Write horizontal enable width WHENW 9	8	7	6	5	4	3	2	1	0	
	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	0301
3	ADC clamp pulse width BCLW 5	4	3	2	1	0	ADC clamp pulse phase BCLP 9	8	7	6	5	4	3	2	1	0	
	0	1	0	0	1	1	0	0	0	0	1	0	0	1	0	0	4C24
4			Still STILL	O/E inversion WOEN			Write/read vertical reference phase WVPS 9	8	7	6	5	4	3	2	1	0	
	0	0	0	1	0	0	0	0	0	1	1	1	0	0	0	0	1070
5	Write Y phase correction WYDL 3	2	1	0		CLP VMASK CLVMS	Write vertical enable phase WVENP 9	8	7	6	5	4	3	2	1	0	
	1	0	0	1	0	0	0	0	0	0	0	1	0	1	0	0	9414
6	Write C phase correction WCDL 3	2	1	0	W-EN Polarity PWEN	W-RST Polarity PMWR	Write vertical enable width WVENW 9	8	7	6	5	4	3	2	1	0	
	1	0	1	1	0	0	0	1	0	0	1	0	0	1	0	1	B125
7	Read horizontal AFC divider value RHCNT 7	6	5	4	3	2	1	0	Read horizontal counter divider value RHACNT 7	6	5	4	3	2	1	0	
	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
8		RHACNT 8		RHCNT 8				VD interlace phase RHIR 8	7	6	5	4	3	2	1	0	
	0	1	0	1	0	0	0	0	1	1	1	1	1	0	1	0	50FA
9						H frame phase switch RHFRON	H field phase switch RHVRON	R-HOUT RSTSW MDHD	R-HOUT Pull-in switch MDHR	R-HD Polarity PRHD	RHD width RHDW 5	4	3	2	1	0	
	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	01A0

SUB	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	SET VALUE [HEX]
A								Read horizontal enable phase RHENP									
								8	7	6	5	4	3	2	1	0	
	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	0	0056
B								Read horizontal enable width RHENW									
								8	7	6	5	4	3	2	1	0	
	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0180
C	Output clamp width ACLW							Output clamp phase ACLP									
	5	4	3	2	1	0		8	7	6	5	4	3	2	1	0	
	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	4010
D								Internal horizontal blanking set IHBLS									
								8	7	6	5	4	3	2	1	0	
	0	0	0	0	0	0	0	1	1	1	0	1	1	0	0	0	01D8
E								Internal horizontal blanking reset IHBLR									
								8	7	6	5	4	3	2	1	0	
	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	0	
F								Output horizontal blanking set CHBLS									0056
								8	7	6	5	4	3	2	1	0	
	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	
10								Output horizontal blanking reset CHBLR									
								8	7	6	5	4	3	2	1	0	
	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0030
11								Horizontal black peak mask set HBMS									
								8	7	6	5	4	3	2	1	0	
	0	0	0	0	0	0	0	1	1	1	0	1	0	0	0	0	01D0
12								Horizontal black peak mask reset HBMR									
								8	7	6	5	4	3	2	1	0	
	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0060

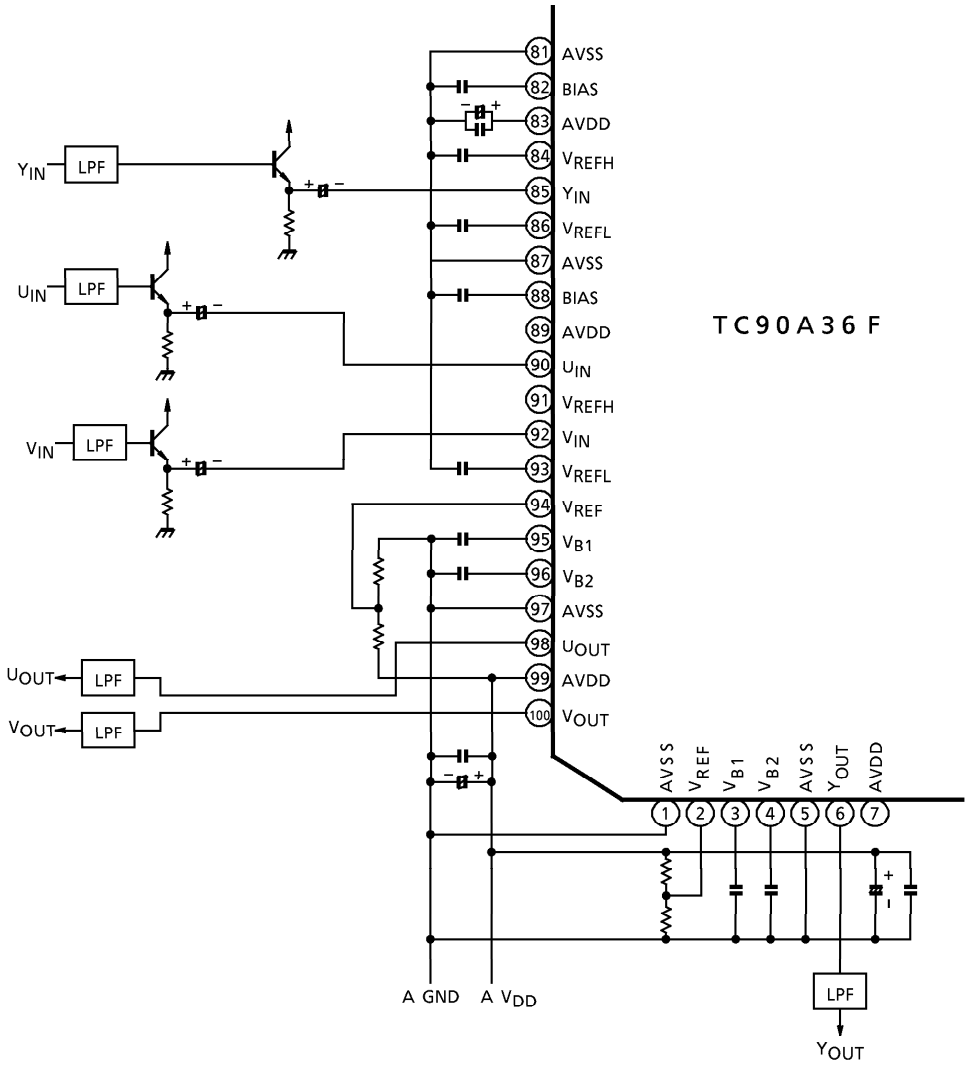
SUB	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	SET VALUE [HEX]
13	IVBLK OFF IVBOF	OVBLK OFF OVBOF	VBMASK OFF VBMOF	R-VEN OFF RVEOF				Horizontal speed modulation off set HVMOS									
								8	7	6	5	4	3	2	1	0	
	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0180
14	IHBLK OFF IHBOF	CHBLK OFF OHBOF	HBMASK OFF HBMOF	R-HEN OFF RHEOF	CLPBM SEPA ACLS	R-HEN Polarity PREN		Horizontal speed modulation off reset HVMOR									
								8	7	6	5	4	3	2	1	0	
	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0808
15	Read Y phase RYDL							Horizontal side panel set HSPS									
	3	2	1	0				8	7	6	5	4	3	2	1	0	
	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	01FF
16	Read C phase RCDL							Horizontal side panel reset HSPR									
	3	2	1	0				8	7	6	5	4	3	2	1	0	
	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0066
17				RVD Mode VWHM	RVD Polarity PRVD	MRR Polarity PMRR		RVD phase RVDP									
								8	7	6	5	4	3	2	1	0	
	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	004B
18								Read vertical enable phase RVENP									
								8	7	6	5	4	3	2	1	0	
	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	005F
19								Read vertical enable width RVENW									
								8	7	6	5	4	3	2	1	0	
	0	0	0	0	0	0	0	1	0	0	1	1	0	1	0	0	0125
1A								Internal vertical blanking set IVBLS									
								8	7	6	5	4	3	2	1	0	
	0	0	0	0	0	0	0	1	0	0	1	1	0	1	0	0	0134
1B								Internal vertical blanking reset IVBLR									
								8	7	6	5	4	3	2	1	0	
	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0018

SUB	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	SET VALUE [HEX]
1C								Output vertical blanking set OVBLS									
								8	7	6	5	4	3	2	1	0	
	0	0	0	0	0	0	0	1	0	0	1	1	0	1	0	0	0134
1D								Output vertical blanking reset OVBLR									
								8	7	6	5	4	3	2	1	0	
	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0018
1E								Vertical black peak mask set VBMS									
								8	7	6	5	4	3	2	1	0	
	0	0	0	0	0	0	0	1	0	0	1	1	0	1	0	0	0134
1F								Vertical black peak mask reset VBMR									
								8	7	6	5	4	3	2	1	0	
	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	001F
20								Caption compression position set JCPS									
								8	7	6	5	4	3	2	1	0	
	0	0	0	0	0	0	0	1	0	0	1	1	0	1	0	0	0134
21								Caption compression position reset JCPR									
								8	7	6	5	4	3	2	1	0	
	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	001F
22	Y side panel level YSPL								Y blanking level YBLL								
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	2020
23		JCP YCAOUT	ICSWO YCAOUT		RPLL PD-OFF			Y 1CK DLY	C blanking level CBLL								
				MUTE	RHPOF	ICSW1	ICSW0	YDL0	7	6	5	4	3	2	1	0	
	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0880

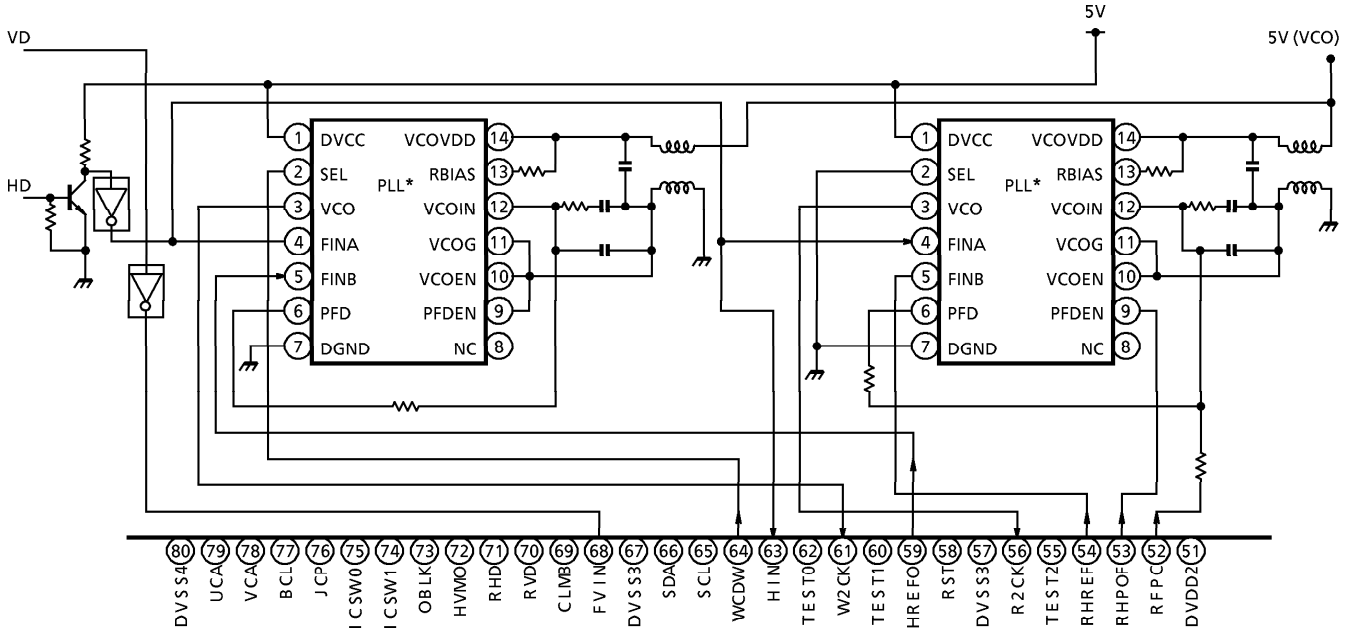
SCHEMATIC OF FIELD DOUBLE SCAN SYSTEM



EXAMPLE OF A/D CONVERTER AND D/A CONVERTER PERIPHERAL CIRCUIT



EXAMPLE OF VCO PERIPHERAL CIRCUIT

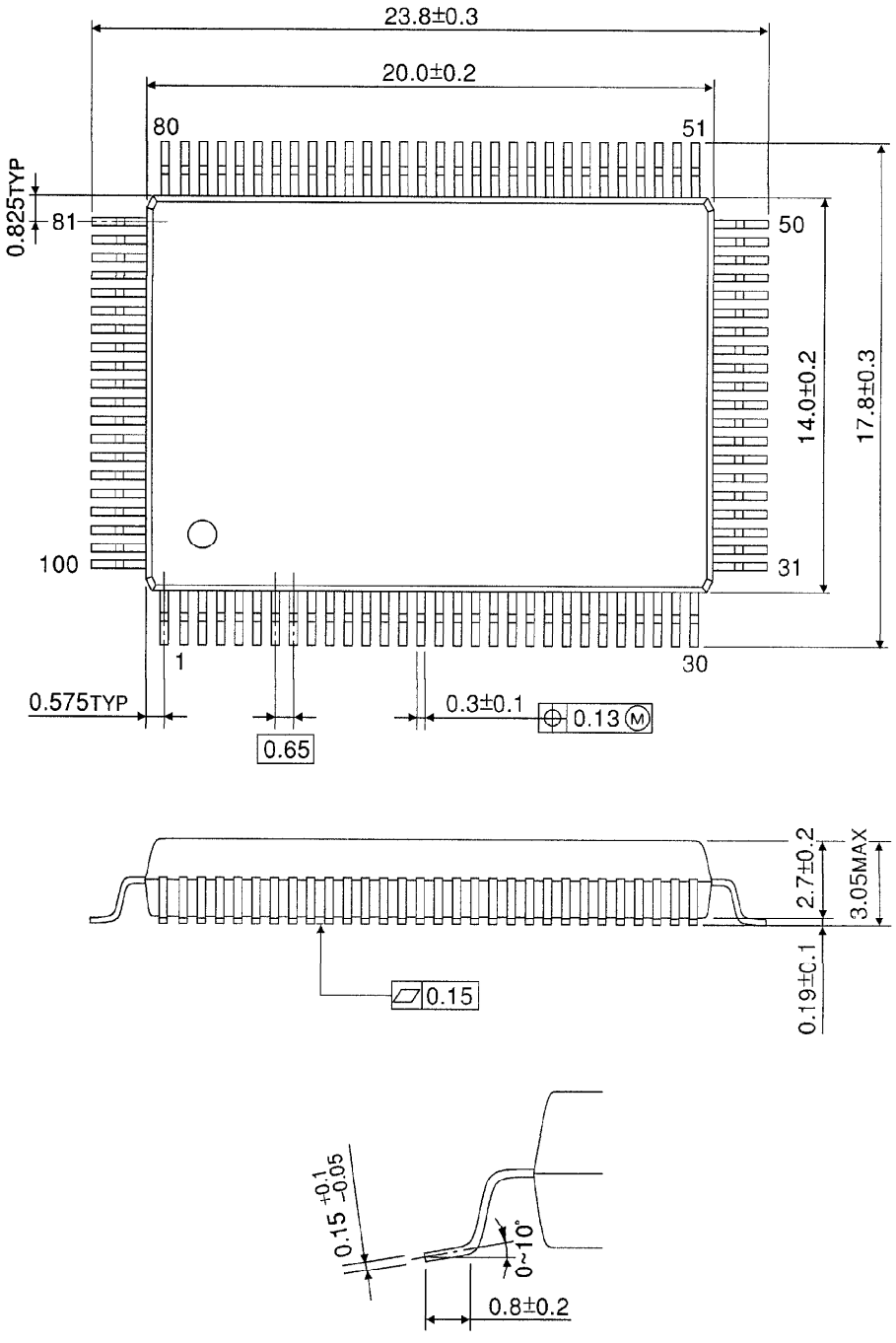


TC90A36F

PLL* : TEXAS INSTRUMENTS TLC2932

PACKAGE DIMENSIONS

QFP100-P-1420-0.65A Unit : mm



Weight : 1.6g (Typ.)