

32-bit RISC Microcontroller

CMOS

FR Family MB91F109

MB91F109

■ DESCRIPTION

The MB91F109 is a standard single-chip microcontroller constructed around the 32-bit RISC CPU (FR* family) core with abundant I/O resources and bus control functions optimized for high-performance/high-speed CPU processing for embedded controller applications. To carry out hi-speed performance of CPU instructions, instruction/data Flash memory of 254 Kbytes and RAM of 2 Kbytes + 2 Kbytes are embedded in the MB91F109.

The MB91F109 is optimized for applications requiring high-performance CPU processing such as navigation systems, high-performance FAXs and printer controllers.

* : FR Family stands for FUJITSU RISC controller.

■ FEATURES

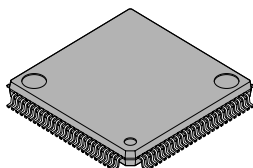
FR CPU

- 32-bit RISC, load/store architecture, 5-stage pipeline
- Operating clock frequency: Internal 25 MHz/external 25 MHz (PLL used at source oscillation 12.5 MHz)
- General purpose registers: 32 bits × 16
- 16-bit fixed length instructions (basic instructions), 1 instruction/1 cycle
- Memory to memory transfer, bit processing, barrel shifter processing: Optimized for embedded applications
- Function entrance/exit instructions, multiple load/store instructions of register contents, instruction systems supporting high level languages

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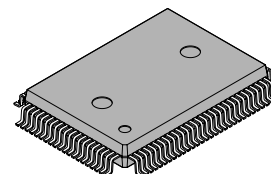
■ PACKAGES

100-pin Plastic LQFP



(FPT-100P-M05)

100-pin Plastic QFP



(FPT-100P-M06)

- Register interlock functions, efficient assembly language coding
- Branch instructions with delay slots: Reduced overhead time in branch executions
- Internal multiplier/supported at instruction level
 - Signed 32-bit multiplication: 5 cycles
 - Signed 16-bit multiplication: 3 cycles
- Interrupt (push PC and PS): 6 cycles, 16 priority levels

External bus interface

- Without Clock doubler: Maximum internal bus 25 MHz, maximum external bus 25 MHz operation
- 25-bit address bus (32 Mbytes memory space)
- 8/16-bit data bus
- Basic external bus cycle: 2 clock cycles
- Chip select outputs for setting down to a minimum memory block size of 64 Kbytes: 6
- Interface supported for various memory technologies
 - DRAM interface (area 4 and 5)
- Automatic wait cycle insertion: Flexible setting, from 0 to 7 for each area
- Unused data/address pins can be configured as input/output ports
- Little endian mode supported (Select 1 area from area 1 to 5)

DRAM interface

- 2 banks independent control (area 4 and 5)
- Normal mode (double CAS DRAM)/high-speed page mode (single CAS DRAM)/Hyper DRAM
- Basic bus cycle: Normally 5 cycles, 2-cycle access possible in high-speed page mode
- Programmable waveform: Automatic 1-cycle wait insertion to RAS and CAS cycles
- DRAM refresh
 - CBR refresh (interval time configurable by 6-bit timer)
 - Self-refresh mode
- Supports 8/9/10/12-bit column address width
- 2CAS/1WE, 2WE/1CAS selective

DMA controller (DMAC)

- 8 channels
- Transfer incident/external pins/internal resource interrupt requests
- Transfer sequence: Step transfer/block transfer/burst transfer/continuous transfer
- Transfer data length: 8 bits/16 bits/32 bits selective
- NMI/interrupt request enables temporary stop operation

UART

- 3 independent channels
- Full-duplex double buffer
- Data length: 7 bits to 9 bits (non-parity), 6 bits to 8 bits (parity)
- Asynchronous (start-stop system), CLK-synchronized communication selective
- Multi-processor mode
- Internal 16-bit timer (U-TIMER) operating as a proprietary baud rate generator: Generates any given baud rate
- Use external clock can be used as a transfer clock
- Error detection: Parity, frame, overrun

10-bit A/D converter (successive approximation conversion type)

- 10-bit resolution, 4 channels
- Successive approximation type: Conversion time of 5.6 μ s at 25 MHz
- Internal sample and hold circuit
- Conversion mode: Single conversion/scanning conversion/repeated conversion/stop conversion selective
- Start: Software/external trigger/internal timer selective

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16-bit reload timer

- 3 channels
- Internal clock: 2 clock cycle resolution, divide by 2/8/32 selective

Other interval timers

- 16-bit timer: 3 channels (U-TIMER)
- PWM timer: 4 channels
- Watchdog timer: 1 channel

Bit search module

First bit transition "1" or "0" from MSB can be detected in 1 cycle

Interrupt controller

- External interrupt input: Non-maskable interrupt ($\overline{\text{NMI}}$), normal interrupt $\times 4$ (INT0 to INT3)
- Internal interrupt incident: UART, DMA controller (DMAC), 10-bit A/D converter, 16-bit reload-timer, PWM timer, U-TIMER and delayed interrupt module
- Priority levels of interrupts are programmable except for non-maskable interrupt (in 16 steps)

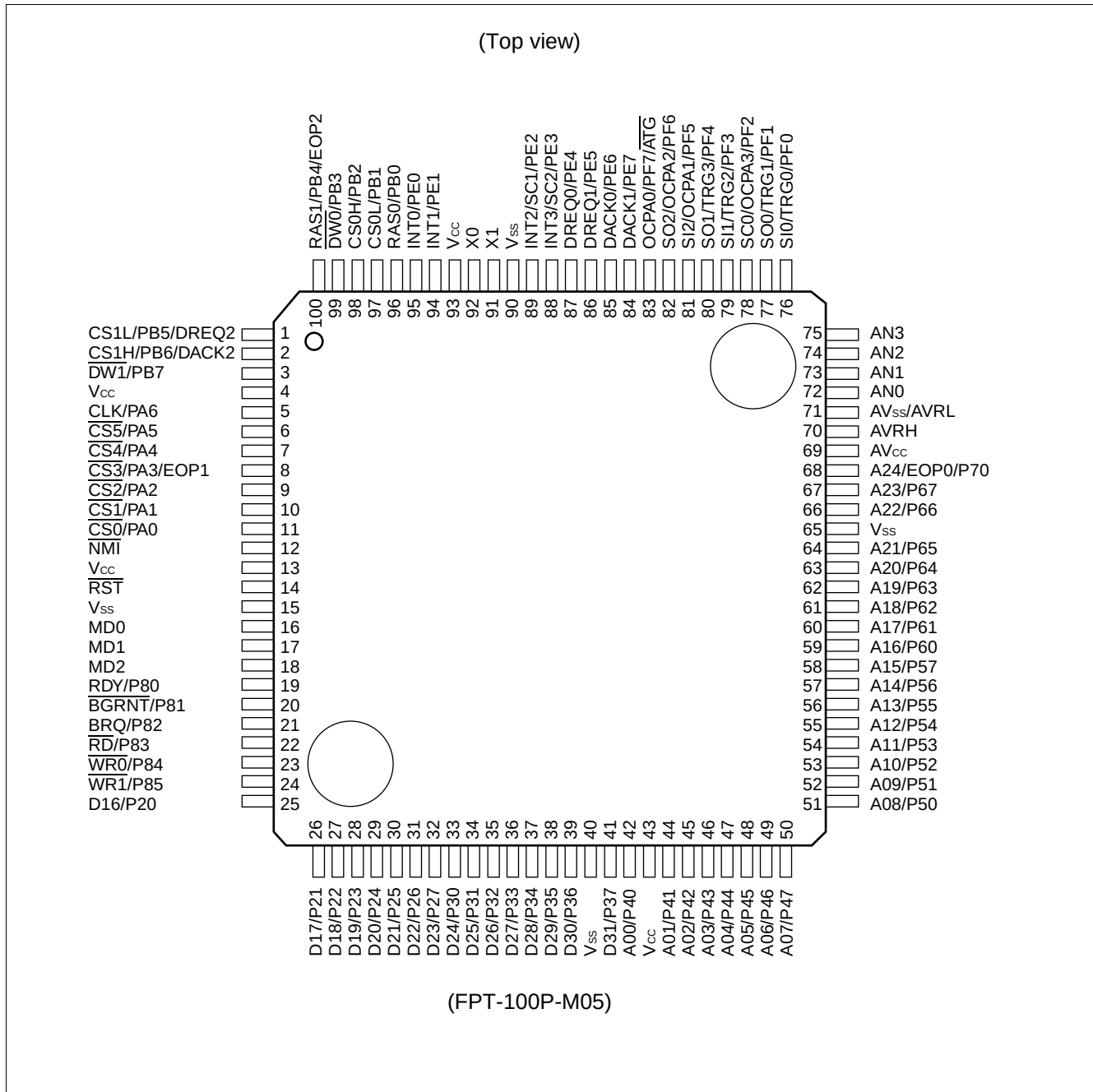
Others

- Reset cause: Power-on reset/software reset/external reset
- Low-power consumption mode: Sleep mode/stop mode
- Clock control
Gear function: Operating clocks for CPU and peripherals are independently selective
Gear clock can be selected from 1/1, 1/2, 1/4 and 1/8 (or 1/2, 1/4, 1/8 and 1/16)
(However, operating frequency for peripherals is less than 25 MHz.)
- Packages: LQFP-100 and QFP-100
- CMOS technology (0.5 μm)
- Power supply voltage: 3.15 V $\sim$ 3.6 V

■ PRODUCT LINEUP

Part number	MB91F109
Parameter	
Classification	Mass production products Flash (mask ROM products)
Flash size	254 Kbytes
IRAM size	—
CROM size	—
CRAM size	2 Kbytes
RAM size	2 Kbytes
I \$	—
Other	Under trial manufacture

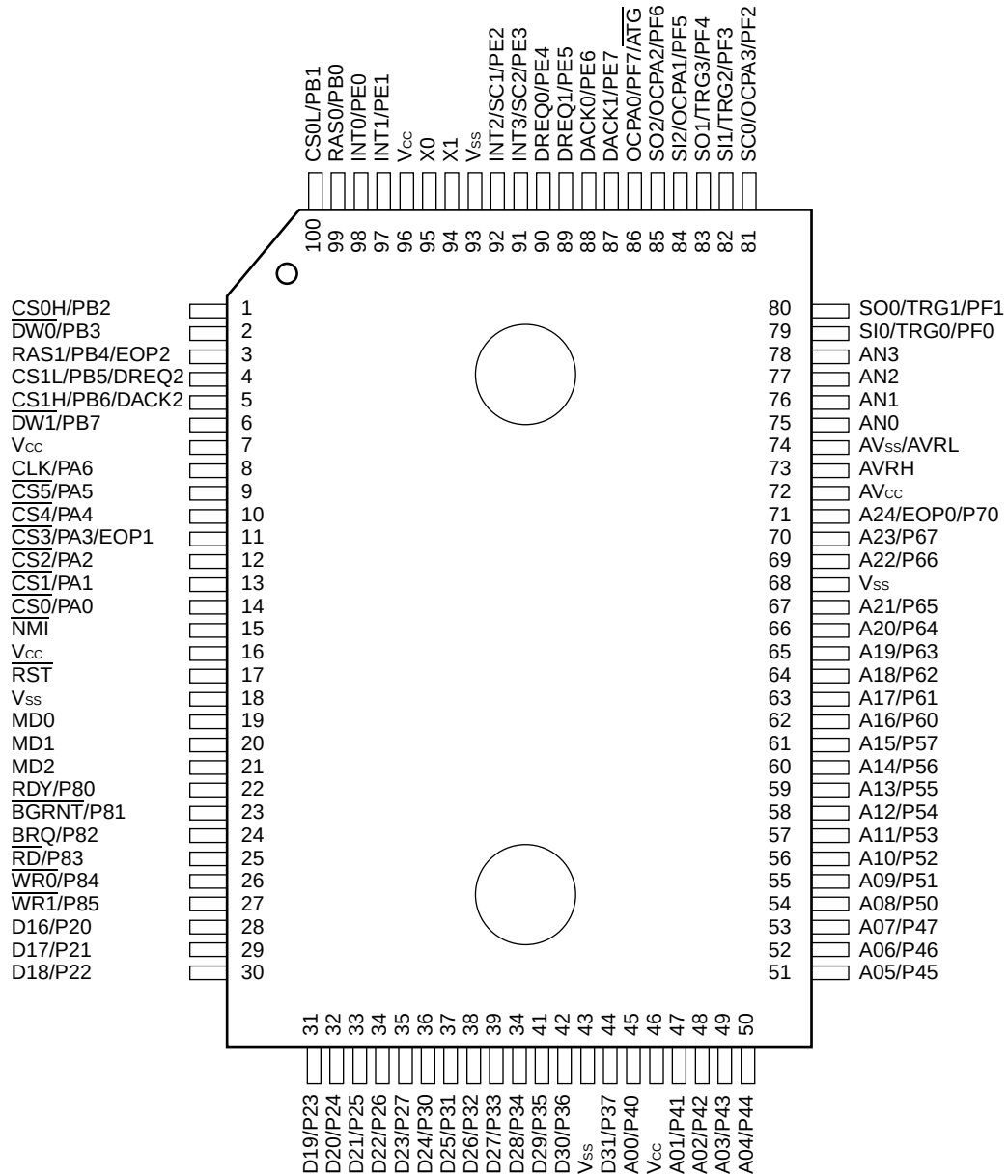
PIN ASSIGNMENTS



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(Top view)



(FPT-100P-M06)

MB91F109

■ PIN DESCRIPTION

Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2			
25 to 32	28 to 35	D16 to D23	C	Bit 16 to bit 23 of external data bus
		P20 to P27		Can be configured as general purpose I/O port when external data bus width is set to 8-bit or in single chip mode.
33 to 39, 41	36 to 42, 44	D24 to D30, D31	C	Bit 24 to bit 31 of external data bus
		P30 to P36, P37		Can be configured as general purpose I/O ports when not used as address bus.
42, 44 to 50, 51 to 58	45, 47 to 53, 54 to 61	A00, A01 to A07, A08 to A15	E	Bit 00 to bit 15 of external address bus
		P40, P41 to P47, P50 to P57		Can be configured as general purpose I/O ports when not used as address bus.
59 to 64, 66, 67	62 to 67, 69, 70	A16 to A21, A22, A23	E	Bit 16 to bit 23 of external address bus
		P60 to P65, P66, P67		Can be configured as general purpose I/O ports when not used as address bus.
68	71	A24	E	Bit 24 of external address bus
		EOP0		Can be configured as DMAC EOP output (ch. 0) when DMAC EOP output is enabled.
		P70		Can be configured as general purpose I/O port when A24 and EOP0 are not used.
19	22	RDY	C	External ready input Inputs "0" when bus cycle is being executed and not completed.
		P80		Can be configured as general purpose I/O port when RDY is not used.
20	23	$\overline{\text{BGRNT}}$	E	External bus release acknowledge output Outputs "L" level when external bus is released.
		P81		Can be configured as general purpose I/O port when $\overline{\text{BGRNT}}$ is not used.
21	24	BRQ	C	External bus release request input Inputs "1" when release of external bus is required.
		P82		Can be configured as general purpose I/O port when BRQ is not used.
22	25	$\overline{\text{RD}}$	E	Read strobe output pin for external bus
		P83		Can be configured as general purpose I/O port when $\overline{\text{RD}}$ is not used.

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*1 : FPT-100P-M05

*2 : FPT-100P-M06

Pin no.		Pin name	Circuit type	Function												
LQFP*1	QFP*2															
23	26	P84	E	Can be configured as general purpose I/O port when $\overline{WR0}$ is not used.												
		$\overline{WR0}$		Write strobe output pin for external bus												
24	27	$\overline{WR1}$	E	Relation between control signals and effective byte locations is as follows: <table><tr><th></th><th>16-bit bus width</th><th>8-bit bus width</th><th>Single chip mode</th></tr><tr><td>D31 to D24</td><td>$\overline{WR0}$</td><td>$\overline{WR0}$</td><td>(I/O port enabled)</td></tr><tr><td>D23 to D16</td><td>$\overline{WR1}$</td><td>(I/O port enabled)</td><td>(I/O port enabled)</td></tr></table>		16-bit bus width	8-bit bus width	Single chip mode	D31 to D24	$\overline{WR0}$	$\overline{WR0}$	(I/O port enabled)	D23 to D16	$\overline{WR1}$	(I/O port enabled)	(I/O port enabled)
					16-bit bus width	8-bit bus width	Single chip mode									
				D31 to D24	$\overline{WR0}$	$\overline{WR0}$	(I/O port enabled)									
		D23 to D16		$\overline{WR1}$	(I/O port enabled)	(I/O port enabled)										
P85	Can be configured as general purpose I/O port when $\overline{WR1}$ is not used.															
11	14	$\overline{CS0}$	E	Chip select 0 output ("L" active)												
		PA0		Can be configured as general purpose I/O port when $\overline{CS0}$ is not used.												
10	13	$\overline{CS1}$	E	Chip select 1 output ("L" active)												
		PA1		Can be configured as general purpose I/O port when $\overline{CS1}$ is not used.												
9	12	$\overline{CS2}$	E	Chip select 2 output ("L" active)												
		PA2		Can be configured as a port when $\overline{CS2}$ is not used.												
8	11	$\overline{CS3}$	E	Chip select 3 output ("L" active)												
		PA3		Can be configured as a port when $\overline{CS3}$ and EOP1 are not used.												
		EOP1		EOP output pin for DMAC (ch. 1) This function is available when EOP output for DMAC is enabled.												
7	10	$\overline{CS4}$	E	Chip select 4 output ("L" active)												
		PA4		Can be configured as general purpose I/O port when $\overline{CS4}$ is not used.												
6	9	$\overline{CS5}$	E	Chip select 5 output ("L" active)												
		PA5		Can be configured as general purpose I/O port when $\overline{CS5}$ is not used.												
5	8	CLK	E	System clock output Outputs clock signal of external bus operating frequency.												
		PA6		Can be configured as general purpose I/O port when CLK is not used.												

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*1:FPT-100P-M05

*2:FPT-100P-M06

MB91F109

Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2			
96	99	RAS0	E	RAS output for DRAM bank 0
		PB0		Can be configured as general purpose I/O port when RAS0 is not used.
97	100	CS0L	E	CASL output for DRAM bank 0
		PB1		Can be configured as general purpose I/O port when CS0L is not used.
98	1	CS0H	E	CASH output for DRAM bank 0
		PB2		Can be configured as general purpose I/O port when CS0H is not used.
99	2	$\overline{DW0}$	E	$\overline{WE}$ output for DRAM bank 0 ("L" active)
		PB3		Can be configured as general purpose I/O port when $\overline{DW0}$ is not used.
100	3	RAS1	E	RAS output for DRAM bank 1
		PB4		Can be configured as general purpose I/O port when RAS1 and EOP2 are not used.
		EOP2		DMAC EOP output (ch. 2) This function is available when DMAC EOP output is enabled.
1	4	CS1L	E	CASL output for DRAM bank 1
		PB5		Can be configured as general purpose I/O port when CS1L and DREQ are not used.
		DREQ2		External transfer request input pin for DMA This pin is used for input when external trigger is selected to cause DMAC operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
2	5	CS1H	E	CASH output for DRAM bank 1
		PB6		Can be configured as general purpose I/O port when CS1H and DACK2 are not used.
		DACK2		External transfer request accept output pin for DMAC (ch. 2) This function is available when transfer request output for DMAC is enabled.
3	6	$\overline{DW1}$	E	$\overline{WE}$ output for DRAM bank 1 ("L" active)
		PB7		Can be configured as general purpose I/O port when $\overline{DW1}$ is not used.
16 to 18	19 to 21	MD0 to MD2	F	Mode pins 0 to 2 MCU basic operation mode is set by these pins. Directly connect these pins with V_{CC} or V_{SS} for use.
92	95	X0	A	Clock (oscillator) input
91	94	X1	A	Clock (oscillator) output
14	17	$\overline{RST}$	B	External reset input
12	15	$\overline{NMI}$	G	NMI (non-maskable interrupt pin) input ("L" active)

(Continued)

*1 : FPT-100P-M05

*2 : FPT-100P-M06

Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2			
95, 94	98, 97	INT0, INT1	E	External interrupt request input pins These pins are used for input during corresponding interrupt is enabled, and it is necessary to disable output for other functions from these pins unless such output is made intentionally.
		PE0, PE1		Can be configured as general purpose I/O ports when INT0 and INT1 are not used.
89	92	INT2	E	External interrupt request input pin This pin is used for input during corresponding interrupt is enabled, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		SC1		Clock I/O pin for UART1 Clock output is available when clock output of UART1 is enabled.
		PE2		Can be configured as general purpose I/O port when INT2 and SC1 are not used. This function is available when UART1 clock output is disabled.
88	91	INT3	E	External interrupt request input pin This pin is used for input during corresponding interrupt is enabled, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		SC2		UART2 clock I/O pin Clock output is available when UART2 clock output is enabled.
		PE3		Can be configured as general purpose I/O port when INT3 and SC2 are not used. This function is available when UART2 clock output is disabled.
87, 86	90, 89	DREQ0, DREQ1	E	External transfer request input pins for DMA These pins are used for input when external trigger is selected to cause DMAC operation, and it is necessary to disable output for other functions from these pins unless such output is made intentionally.
		PE4, PE5		Can be configured as general purpose I/O ports when DREQ0 and DREQ1 are not used.
85	88	DACK0	E	External transfer request acknowledge output pin for DMAC (ch. 0) This function is available when transfer request output for DMAC is enabled.
		PE6		Can be configured as general purpose I/O port when DACK0 is not used. This function is available when transfer request acknowledge output for DMAC or DACK0 output is disabled.

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*1 : FPT-100P-M05

*2 : FPT-100P-M06

MB91F109

Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2			
84	87	DACK1	E	External transfer request acknowledge output pin for DMAC (ch. 1) This function is available when transfer request output for DMAC is enabled.
		PE7		Can be configured as general purpose I/O port when DACK1 is not used. This function is available when transfer request output for DMAC or DACK1 output is disabled.
76	79	SI0	E	UART0 data input pin This pin is used for input during UART0 is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		TRG0		PWM timer external trigger input pin (ch.0) This pin is used for input during PWM timer external trigger is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		PF0		Can be configured as general purpose I/O port when SI0 and TRG0 are not used.
77	80	SO0	E	UART0 data output pin This function is available when UART0 data output is enabled.
		TRG1		PWM timer external trigger input pin This function is available when serial data output of PF1, UART0 are disabled.
		PF1		Can be configured as general purpose I/O port when SO0 and TRG1 are not used. This function is available when serial data output of UART0 is disabled.
78	81	SC0	E	UART0 clock I/O pin Clock output is available when UART0 clock output is enabled.
		OCPA3		PWM timer output pin This function is available when PWM timer output is enabled.
		PF2		Can be configured as general purpose I/O port when SC0 and OCPA3 are not used. This function is available when UART0 clock output is disabled.
79	82	SI1	E	UART1 data input pin This pin is used for input during UART1 is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		TRG2		PWM timer external trigger input pin This pin is used for input during PWM timer external trigger is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		PF3		Can be configured as general purpose I/O port when SI1 and TRG2 are not used.

*1 : FPT-100P-M05

*2 : FPT-100P-M06

(Continued)

Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2			
80	83	SO1	E	UART1 data output pin This function is available when UART1 data output is enabled.
		TRG3		PWM timer external trigger input pin This function is available when PF4, UART1 data outputs are disabled.
		PF4		Can be configured as general purpose I/O port when SO1 and TRG3 are not used. This function is available when UART1 data output is disabled.
81	84	SI2	E	UART2 data input pin This pin is used for input during UART2 is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		OCPA1		PWM timer output pin This function is available when PWM timer output is enabled.
		PF5		Can be configured as general purpose I/O port when SI2 and OCPA2 are not used.
82	85	SO2	E	UART2 data output pin This function is available when UART2 data output is enabled.
		OCPA2		PWM timer output pin This function is available when PWM timer output is enabled.
		PF6		Can be configured as general purpose I/O port when SO2 and OCPA2 are not used. This function is available when UART2 data output is disabled.
83	86	OCPA0	E	PWM timer output pin This function is available when PWM timer output is enabled.
		PF7		Can be configured as a port when OCPA0 and $\overline{ATG}$ are not used. This function is available when PWM timer output is disabled.
		$\overline{ATG}$		External trigger input pin for A/D converter This pin is used for input when external trigger is selected to cause A/D converter operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
72 to 75	75 to 78	AN0 to AN3	D	Analog input pins of A/D converter
69	72	AV _{CC}	—	Power supply pin (V _{CC}) for A/D converter
70	73	AVRH	—	Reference voltage input (high) for A/D converter Make sure to turn on and off this pin with potential of AVRH or more applied to V _{CC} .
71	74	AV _{SS} , AVRL	—	Power supply pin (V _{SS}) for A/D converter and reference voltage input pin (low)

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*1 : FPT-100P-M05

*2 : FPT-100P-M06

MB91F109

(Continued)

Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2			
4, 13, 43, 93	7, 16, 46, 96	V _{CC}	—	Power supply pin (V _{CC}) for digital circuit Always power supply pin (V _{CC}) must be connected to the power supply
15, 40, 65, 90	18, 43, 68, 93	V _{SS}	—	Earth level (V _{SS}) for digital circuit

*1 : FPT-100P-M05

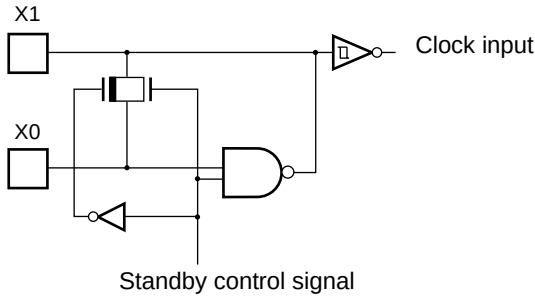
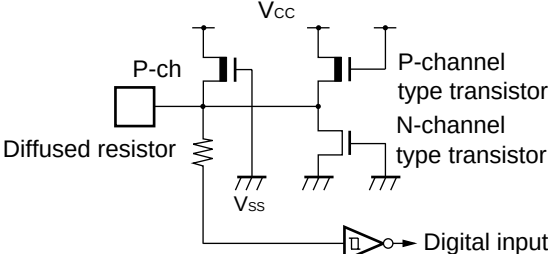
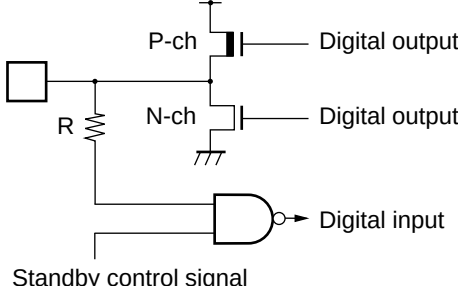
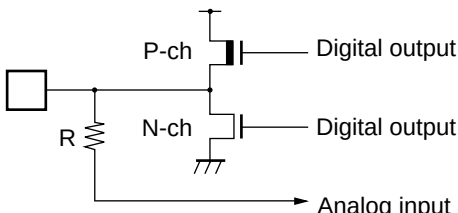
*2 : FPT-100P-M06

Note : In most of the above pins, I/O port and resource I/O are multiplexed e.g. xxx/Pxxx. In case of conflict between output of I/O port and resource I/O, priority is always given to the output of resource I/O.

■ DRAM CONTROL PIN

Pin name	Data bus 16-bit mode		Data bus 8-bit mode	Remarks
	2CAS/1WR mode	1CAS/2WR mode		
RAS0	Area 4 RAS	Area 4 RAS	Area 4 RAS	Correspondence of "L" "H" to lower address 1 bit (A0) in data bus 16- bit mode "L": "0" "H": "1" CASL: CAS which A0 corresponds to "0" area CASH: CAS which A0 corresponds to "1" area WEL: $\overline{WE}$ which A0 corresponds to "0" area WEH: $\overline{WE}$ which A0 corresponds to "1" area
RAS1	Area 5 RAS	Area 5 RAS	Area 5 RAS	
CS0L	Area 4 CASL	Area 4 CAS	Area 4 CAS	
CS0H	Area 4 CASH	Area 4 $\overline{WEL}$	Area 4 CAS	
CS1L	Area 5 CASL	Area 5 CAS	Area 5 CAS	
CS1H	Area 5 CASH	Area 5 $\overline{WEL}$	Area 5 CAS	
$\overline{DW0}$	Area 4 $\overline{WE}$	Area 4 $\overline{WEH}$	Area 4 $\overline{WE}$	
$\overline{DW1}$	Area 5 $\overline{WE}$	Area 5 $\overline{WEH}$	Area 5 $\overline{WE}$	

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A	 Standby control signal	- Oscillation feedback resistance 1 MΩ approx. - With standby control
B	 Digital input	- CMOS level hysteresis input - Without standby control - With pull-up resistance
C	 Digital output Digital output Digital input Standby control signal	- CMOS level I/O - With standby control
D	 Digital output Digital output Analog input	Analog input

(Continued)

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Type	Circuit	Remarks
E		• CMOS level output • CMOS level hysteresis input - With standby control
F		• CMOS level input - Without standby control
G		• CMOS level hysteresis input - Without standby control

■ HANDLING DEVICES

1. Preventing Latchup

In CMOS ICs, applying voltage higher than V_{CC} or lower than V_{SS} to input/output pin or applying voltage over rating across V_{CC} and V_{SS} may cause latchup.

This phenomenon rapidly increases the power supply current, which may result in thermal breakdown of the device. Make sure to prevent the voltage from exceeding the maximum rating.

Take care that the analog power supply (AV_{CC} , $AVRH$) and the analog input do not exceed the digital power supply (V_{CC}) when the analog power supply turned on or off.

2. Treatment of Unused Pins

Unused pins left open may cause malfunctions. Make sure to connect them to pull-up or pull-down resistors.

3. External Reset Input

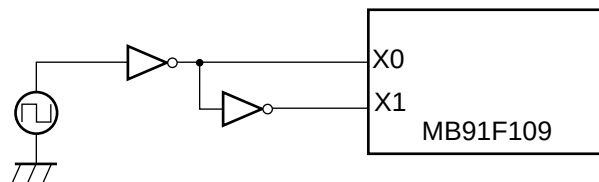
It takes at least 5 machine cycle to input "L" level to the $\overline{RST}$ pin and to ensure inner reset operation properly.

4. Remarks for External Clock Operation

When external clock is selected, supply it to X0 pin generally, and simultaneously the opposite phase clock to X0 must be supplied to X1 pin. However, in this case the stop mode must not be used (because X1 pin stops at "H" output in stop mode).

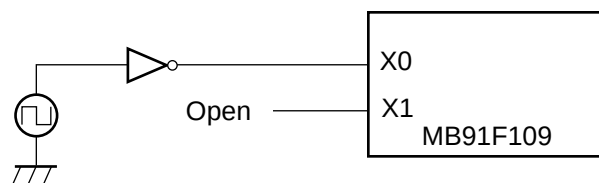
And can be used to supply only to X0 pin with 5 V power supply at 12.5 MHz and less than.

• Using an external clock



Using an external clock (normal)

Note: Can not be used stop mode (oscillation stop mode).



Using an external clock (can be used at 12.5 MHz and less than.)
(3.3 V power supply only)

5. Power Supply Pins

When there are several V_{CC} and V_{SS} pins, each of them is equipotentially connected to its counterpart inside of the device, minimizing the risk of malfunctions such as latch up. To further reduce the risk of malfunctions, to prevent EMI radiation, to prevent strobe signal malfunction resulting from creeping-up of ground level and to observe the total output current standard, connect all V_{CC} and V_{SS} pins to the power supply or GND.

It is preferred to connect V_{CC} and V_{SS} of MB91F109 to power supply with minimal impedance possible.

It is also recommended to connect a ceramic capacitor as a bypass capacitor of about 0.1 μF between V_{CC} and V_{SS} at a position as close as possible to MB91F109.

6. Crystal Oscillator Circuit

Noises around X0 and X1 pins may cause malfunctions of MB91F109. In designing the PC board, layout X0, X1 and crystal oscillator (or ceramic oscillator) and bypass capacitor for grounding as close as possible.

It is strongly recommended to design PC board so that X1 and X0 pins are surrounded by grounding area for stable operation.

7. Turning-on Sequence of A/D Converter Power Supply and Analog Input

Make sure to turn on the digital power supply (V_{CC}) before turning on the A/D converter (AV_{CC} , AV_{RH}) and applying voltage to analog input ($AN0$ to $AN3$).

Make sure to turn off digital power supply after power supply to A/D converters and analog inputs have been switched off. (There are no such limitations in turning on power supplies. Analog and digital power supplies may be turned on simultaneously.) Make sure that AV_{RH} never exceeds AV_{CC} when turning on/off power supplies.

8. Treatment of N.C. Pins

Make sure to leave N.C. pins open.

9. Fluctuation of Power Supply Voltage

Warranty range for normal operation against fluctuation of power supply voltage V_{CC} is as given in rating. However, sudden fluctuation of power supply voltage within the warranty range may cause malfunctions. It is recommended to make every effort to stabilize the power supply voltage to IC. It is also recommended that by controlling power supply as a reference of stabilizing, V_{CC} ripple fluctuation (P-P value) at the commercial frequency (50 Hz to 60 Hz) should be less than 10% of the standard V_{CC} value and the transient regulation should be less than 0.1 V/ms at instantaneous deviation like turning off the power supply.

10. Mode Setting Pins (MD0 to MD2)

Connect mode setting pins (MD0 to MD2) directly to V_{CC} or V_{SS} .

Arrange each mode setting pin and V_{CC} or V_{SS} patterns on the printed circuit board as close as possible and make the impedance between them minimal to prevent mistaken entrance to the test mode caused by noises.

11. Turning on the Power Supply

When turning on the power supply, never fail to start from setting the $\overline{\text{RST}}$ pin to "L" level. And after the power supply voltage goes to V_{CC} level, at least after ensuring the time for 5 machine cycle, then set to "H" level.

12. Pin Condition at Turning on the Power Supply

The pin condition at turning on the power supply is unstable. The circuit starts being initialized after turning on the power supply and then starting oscillation and then the operation of the internal regulator becomes stable. So it takes about 42 ms for the pin to be initialized from the oscillation starting at the source oscillation 12.5 MHz. Take care that the pin condition may be output condition at initial unstable condition.

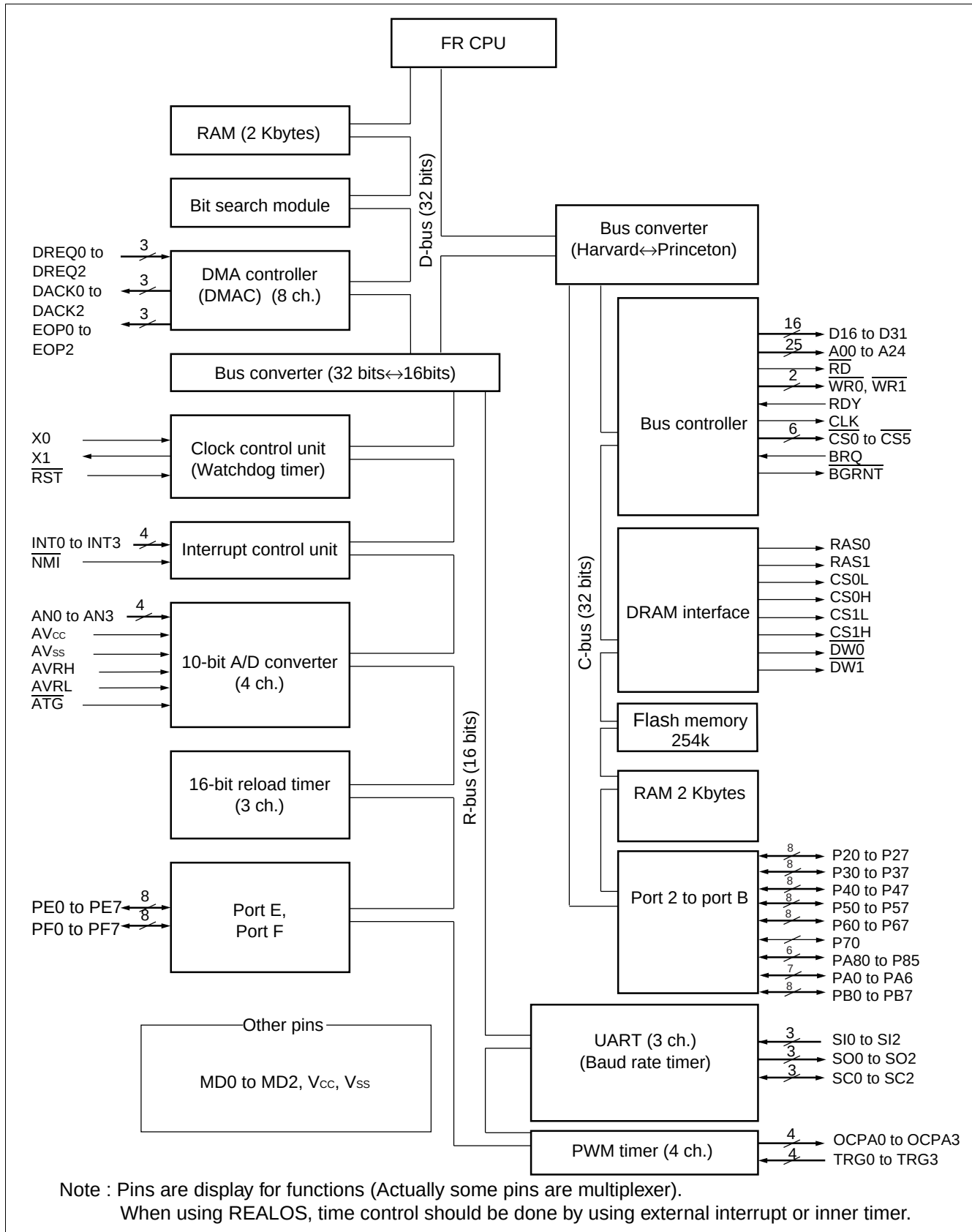
13. Source Oscillation Input at Turning on the Power Supply

At turning on the power supply, never fail to input the clock before cancellation of the oscillation stabilizing waiting.

14. Initialization

Some internal resistors initialized only via power on reset are embedded in the device. To initialize these resistors, run power on reset by returning on the power supply or to set $\overline{\text{RST}}$ pin to "H" level.

■ BLOCK DIAGRAM



■ CPU CORE

1. Memory Space

The FR family has a logical address space of 4 Gbytes (2^{32} bytes) and the CPU linearly accesses the memory space.

• Memory space

• Memory Space

Address	Single chip mode	Internal ROM/ external bus mode	External ROM/ external bus mode	
0000 0000H	I/O Area	I/O Area	I/O Area	Direct addressing area*
0000 0400H	I/O Area	I/O Area	I/O Area	
0000 0800H	Access inhibited	Access inhibited	Access inhibited	See "■ I/O MAP"
0000 1000H	RAM 2 Kbytes	RAM 2 Kbytes	RAM 2 Kbytes	
0000 1800H	Access inhibited	Access inhibited	Access inhibited	
0001 0000H	Access inhibited	External area	External area	
0008 0000H	Access inhibited	Access inhibited		
000C 0000H	RAM 2 Kbytes	RAM 2 Kbytes		
000C 0800H	FLASH ROM 254 Kbytes	FLASH ROM 254 Kbytes		
0010 0000H	Access inhibited	External area		
FFFF FFFFH				

*: Direct addressing area

The following areas on the memory space are assigned to direct addressing area for I/O. In these areas, an address can be specified in a direct operand of a code.

Direct areas consists of the following areas dependent on accessible data sizes.

Byte data access : 000H to 0FFH

Half word data access: 000H to 1FFH

Word data access : 000H to 3FFH

Notes: Access to the external area can be execute in the single chip mode.
To access to the external area, select internal ROM external bus mode via mode resistor.
Never execute data access to the instruction ROM area.

2. Registers

The FR family has two types of registers; dedicated registers embedded on the CPU and general-purpose registers on memory.

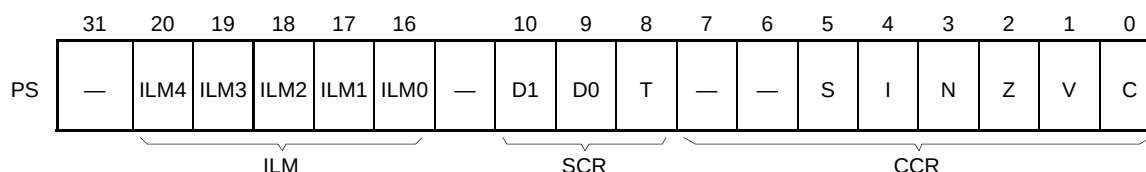
• Dedicated registers

- Program counter (PC) : 32-bit length, indicates the location of the instruction to be executed.
- Program status (PS) : 32-bit length, register for storing register pointer or condition codes
- Table base register (TBR) : Holds top address of vector table used in EIT (Exceptional/Interrupt/Trap) processing.
- Return pointer (RP) : Holds address to resume operation after returning from a subroutine.
- System stack pointer (SSP) : Indicates system stack space.
- User's stack pointer (USP) : Indicates user's stack space.
- Multiplication/division result register (MDH/MDL) : 32-bit length, register for multiplication/division

← 32 bits →			Initial value	
PC	Program counter	XXXX XXXX _H	Indeterminate	
PS	Program status			
TBR	Table base register	000F FC00 _H		
RP	Return pointer	XXXX XXXX _H	Indeterminate	
SSP	System stack pointer	0000 0000 _H		
USP	User's stack pointer	XXXX XXXX _H	Indeterminate	
MDH	Multiplication/division result register	XXXX XXXX _H	Indeterminate	
MDL		XXXX XXXX _H	Indeterminate	

• Program status (PS)

The PS register is for holding program status and consists of a condition code register (CCR), a system condition code register (SCR) and a interrupt level mask register (ILM).



- **Condition code register (CCR)**

- S-flag: Specifies a stack pointer used as R15.
- I-flag: Controls user interrupt request enable/disable.
- N-flag: Indicates sign bit when division result is assumed to be in the 2's complement format.
- Z-flag: Indicates whether or not the result of division was "0".
- V-flag: Assumes the operand used in calculation in the 2's complement format and indicates whether or not overflow has occurred.
- C-flag: Indicates if a carry or borrow from the MSB has occurred.

- **System condition code register (SCR)**

- T-flag: Specifies whether or not to enable step trace trap.

- **Interrupt level mask register (ILM)**

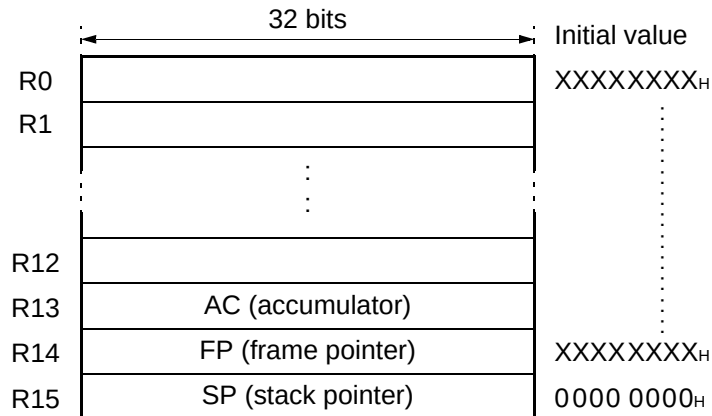
- ILM4 to ILM0: Register for holding interrupt level mask value. The value held by this register is used as a level mask. When an interrupt request issued to the CPU is higher than the level held by ILM, the interrupt request is accepted.

ILM4	ILM3	ILM2	ILM1	ILM0	Interrupt level	High-low
0	0	0	0	0	0	High ↑ ↓ Low
⋮					⋮	
0	1	0	0	0	15	
⋮					⋮	
1	1	1	1	1	31	

■ GENERAL-PURPOSE REGISTERS

R0 to R15 are general-purpose registers embedded on the CPU. These registers functions as an accumulator and a memory access pointer (field for indicating address).

• Register bank structure



Of the above 16 registers, following registers have special functions. To support the special functions, part of the instruction set has been sophisticated to have enhanced functions.

- R13: Virtual accumulator (AC)
- R14: Frame pointer (FP)
- R15: Stack pointer (SP)

Upon reset, values in R0 to R14 are not fixed. Value in R15 is initialized to be 0000 0000_H (SSP value).

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■ SETTING MODE

1. Pin

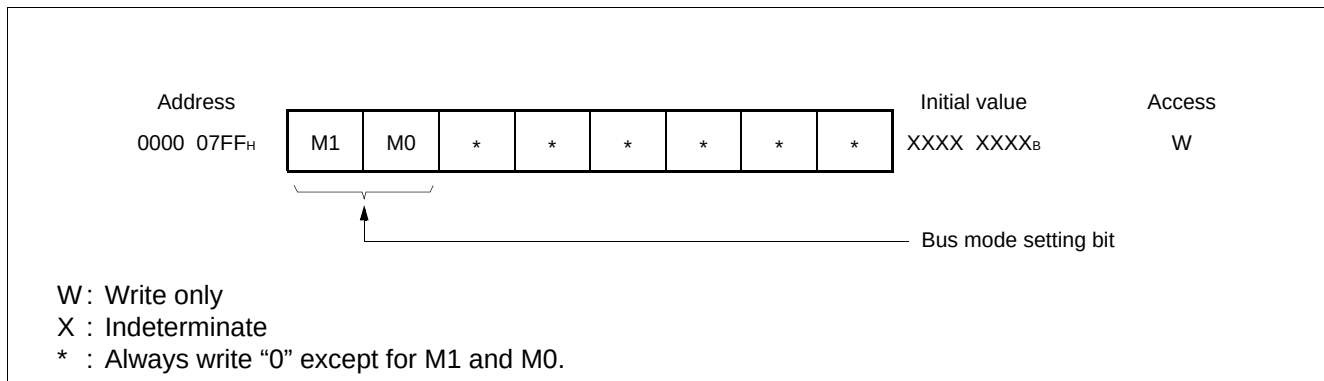
• Mode setting pins and modes

Mode setting pins			Mode name	Reset vector access area	External data bus width	Bus mode
MD2	MD1	MD0				
0	0	0	External vector mode 0	External	8 bits	External ROM/external bus mode
0	0	1	External vector mode 1	External	16 bits	
0	1	0	—	—	—	Inhibited
0	1	1	Internal vector mode	Internal	(Mode register)	Single-chip mode*
1	—	—	—	—	—	Not use

*: MB91F109 support single-chip mode.

2. Registers

• Mode setting registers (MODR) and modes



• Bus mode setting bits and functions

M1	M0	Functions	Note
0	0	Single-chip mode	
0	1	Internal ROM/external bus mode	
1	0	External ROM/external bus mode	
1	1	—	Inhibited

■ I/O MAP

Address	Register name (abbreviated)	Register name	Read/write	Resources name	Initial value
000000 _H	PDR3	Port 3 data register	R/W	Port 3	XXXXXXXX _B
000001 _H	PDR2	Port 2 data register	R/W	Port 2	XXXXXXXX _B
000002 _H	(Vacancy)				
000003 _H					
000004 _H	PDR7	Port 7 data register	R/W	Port 7	-----X _B
000005 _H	PDR6	Port 6 data register	R/W	Port 6	XXXXXXXX _B
000006 _H	PDR5	Port 5 data register	R/W	Port 5	XXXXXXXX _B
000007 _H	PDR4	Port 4 data register	R/W	Port 4	XXXXXXXX _B
000008 _H	PDRB	Port B data register	R/W	Port B	XXXXXXXX _B
000009 _H	PDRA	Port A data register	R/W	Port A	-XXXXXXXX _B
00000A _H	(Vacancy)				
00000B _H	PDR8	Port 8 data register	R/W	Port 8	--XXXXXX _B
00000C _H to 000011 _H	(Vacancy)				
000012 _H	PDRE	Port E data register	R/W	Port E	XXXXXXXX _B
000013 _H	PDRF	Port F data register	R/W	Port F	XXXXXXXX _B
000014 _H to 00001B _H	(Vacancy)				
00001C _H	SSR0	Serial status register 0	R/W	UART0	00001-00 _B
00001D _H	SIDR0/SODR0	Serial input data register 0/serial output data register 0	R/W		XXXXXXXX _B
00001E _H	SCR0	Serial control register 0	R/W		00000100 _B
00001F _H	SMR0	Serial mode register 0	R/W		00--0-00 _B
000020 _H	SSR1	Serial status register 1	R/W	UART1	00001-00 _B
000021 _H	SIDR1/SODR1	Serial input data register 1/serial output data register 1	R/W		XXXXXXXX _B
000022 _H	SCR1	Serial control register 1	R/W		00000100 _B
000023 _H	SMR1	Serial mode register 1	R/W		00--0-00 _B
000024 _H	SSR2	Serial status register 2	R/W	UART2	00001-00 _B
000025 _H	SIDR2/SODR2	Serial input data register 2/serial output data register 2	R/W		XXXXXXXX _B
000026 _H	SCR2	Serial control register 2	R/W		00000100 _B
000027 _H	SMR2	Serial mode register 2	R/W		00--0-00 _B

(Continued)

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Address	Register name (abbreviated)	Register name	Read/write	Resources name	Initial value
000028 _H	TMRLR0	16-bit reload register 0	W	16-bitreload timer 0	XXXXXXXX _B
000029 _H					XXXXXXXX _B
00002A _H	TMR0	16-bit timer register 0	R		XXXXXXXX _B
00002B _H					XXXXXXXX _B
00002C _H	(Vacancy)				
00002D _H					
00002E _H	TMCSR0	16-bit reload timer control status register 0	R/W	16-bitreload timer 0	----0000 _B
00002F _H					00000000 _B
000030 _H	TMRLR1	16-bit reload register 1	W	16-bitreload timer 1	XXXXXXXX _B
000031 _H					XXXXXXXX _B
000032 _H	TMR1	16-bit timer register 1	R		XXXXXXXX _B
000033 _H					XXXXXXXX _B
000034 _H	(Vacancy)				
000035 _H					
000036 _H	TMCSR1	16-bit reload timer control status register 1	R/W	16-bitreload timer 1	----0000 _B
000037 _H					00000000 _B
000038 _H	ADCR	A/D converter data register	R	10-bit A/D converter	000000XX _B
000039 _H					XXXXXXXX _B
00003A _H	ADCS	A/D converter control status register	R/W		00000000 _B
00003B _H					00000000 _B
00003C _H	TMRLR2	16-bit reload register 2	W	16-bitreload timer 2	XXXXXXXX _B
00003D _H					XXXXXXXX _B
00003E _H	TMR2	16-bit timer register 2	R		XXXXXXXX _B
00003F _H					XXXXXXXX _B
000040 _H	(Vacancy)				
000041 _H					
000042 _H	TMCSR2	16-bit reload timer control status register 2	R/W	16-bitreload timer 2	----0000 _B
000043 _H					00000000 _B
000044 _H to 000077 _H	(Vacancy)				

(Continued)

Address	Register name (abbreviated)	Register name	Read/write	Resources name	Initial value
000078 _H	UTIM0/UTIMR0	U-TIMER register ch. 0 /U-TIMER reload register ch. 0	R/W	U-TIMER 0	00000000 _B
000079 _H					00000000 _B
00007A _H	(Vacancy)				
00007B _H	UTIMC0	U-TIMER control register ch. 0	R/W	U-TIMER 0	0--00001 _B
00007C _H	UTIM1/UTIMR1	U-TIMER register ch. 1/reload register ch. 1	R/W	U-TIMER 1	00000000 _B
00007D _H					00000000 _B
00007E _H	(Vacancy)				
00007F _H	UTIMC1	U-TIMER control register ch. 1	R/W	U-TIMER 1	0--00001 _B
000080 _H	UTIM2/UTIMR2	U-TIMER register ch. 2/U-TIMER reload register ch. 2	R/W	U-TIMER 2	00000000 _B
000081 _H					00000000 _B
000082 _H	(Vacancy)				
000083 _H	UTIMC2	U-TIMER control register ch. 2	R/W	U-TIMER 2	0--00001 _B
000084 _H to 000093 _H	(Vacancy)				
000094 _H	EIRR	External interrupt cause register	R/W	External in- terrupt/NMI	00000000 _B
000095 _H	ENIR	Interrupt enable register	R/W		00000000 _B
000096 _H to 000098 _H	(Vacancy)				
000099 _H	ELVR	External interrupt request level setting register	R/W	External in- terrupt/NMI	00000000 _B
00009A _H to 0000D1 _H	(Vacancy)				
0000D2 _H	DDRE	Port E data direction register	W	Port E	00000000 _B
0000D3 _H	DDRF	Port F data direction register	W	Port F	00000000 _B
0000D4 _H to 0000DB _H	(Vacancy)				
0000DC _H	GCN1	General control register 1	R/W	PWM timer 1	00110010 _B
0000DD _H					00010000 _B
0000DE _H	(Vacancy)				
0000DF _H	GCN2	General control register 2	R/W	PWM timer 2	00000000 _B

(Continued)

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Address	Register name (abbreviated)	Register name	Read/ write	Resources name	Initial value
0000E0 _H	PTMR0	PWM timer register 0	R	PWM timer 0	1 1 1 1 1 1 1 1 _B
0000E1 _H					1 1 1 1 1 1 1 1 _B
0000E2 _H	PCSR0	PWM cycle setting register 0	W		XXXXXXXX _B
0000E3 _H					XXXXXXXX _B
0000E4 _H	PDUT0	PWM duty setting register 0	W		XXXXXXXX _B
0000E5 _H					XXXXXXXX _B
0000E6 _H	PCNH0	Control status register H 0	R/W		0 0 0 0 0 0 0 — _B
0000E7 _H	PCNL0	Control status register L 0	R/W		0 0 0 0 0 0 0 0 _B
0000E8 _H	PTMR1	PWM timer register 1	R	PWM timer 1	1 1 1 1 1 1 1 1 _B
0000E9 _H					1 1 1 1 1 1 1 1 _B
0000EA _H	PCSR1	PWM cycle setting register 1	W		XXXXXXXX _B
0000EB _H					XXXXXXXX _B
0000EC _H	PDUT1	PWM duty setting register 1	W		XXXXXXXX _B
0000ED _H					XXXXXXXX _B
0000EE _H	PCNH1	Control status register H 1	R/W		0 0 0 0 0 0 0 — _B
0000EF _H	PCNL1	Control status register L 1	R/W		0 0 0 0 0 0 0 0 _B
0000F0 _H	PTMR2	PWM timer register 2	R	PWM timer 2	1 1 1 1 1 1 1 1 _B
0000F1 _H					1 1 1 1 1 1 1 1 _B
0000F2 _H	PCSR2	PWM cycle setting register 2	W		XXXXXXXX _B
0000F3 _H					XXXXXXXX _B
0000F4 _H	PDUT2	PWM duty setting register 2	W		XXXXXXXX _B
0000F5 _H					XXXXXXXX _B
0000F6 _H	PCNH2	Control status register H 2	R/W		0 0 0 0 0 0 0 — _B
0000F7 _H	PCNL2	Control status register L 2	R/W		0 0 0 0 0 0 0 0 _B
0000F8 _H	PTMR3	PWM timer register 3	R	PWM timer 3	1 1 1 1 1 1 1 1 _B
0000F9 _H					1 1 1 1 1 1 1 1 _B
0000FA _H	PCSR3	PWM cycle setting register 3	W		XXXXXXXX _B
0000FB _H					XXXXXXXX _B
0000FC _H	PDUT3	PWM duty setting register 3	W		XXXXXXXX _B
0000FD _H					XXXXXXXX _B
0000FE _H	PCNH3	Control status register H 3	R/W		0 0 0 0 0 0 0 — _B
0000FF _H	PCNL3	Control status register L 3	R/W		0 0 0 0 0 0 0 0 _B

(Continued)

Address	Register name (abbreviated)	Register name	Read/ write	Resources name	Initial value
000100 _H to 0001FF _H	(Vacancy)				
000200 _H	DPDP	DMAC parameter descriptor pointer	R/W	DMA controller (DMAC)	XXXXXXXX _B
000201 _H					XXXXXXXX _B
000202 _H					XXXXXXXX _B
000203 _H					X0000000 _B
000204 _H	DACSR	DMAC control status register	R/W		00000000 _B
000205 _H					00000000 _B
000206 _H					00000000 _B
000207 _H					00000000 _B
000208 _H	DATCR	DMAC pin control register	R/W		XXXXXXXX _B
000209 _H					XX000000 _B
00020A _H					XX000000 _B
00020B _H					XX000000 _B
00020C _H to 0003EF _H	(Vacancy)				
0003F0 _H	BSD0	Bit search module 0-detection data register	R/W	Bit search module	XXXXXXXX _B
0003F1 _H					XXXXXXXX _B
0003F2 _H					XXXXXXXX _B
0003F3 _H					XXXXXXXX _B
0003F4 _H	BSD1	Bit search module 1-detection data register	R/W		XXXXXXXX _B
0003F5 _H					XXXXXXXX _B
0003F6 _H					XXXXXXXX _B
0003F7 _H					XXXXXXXX _B
0003F8 _H	BSDC	Bit search module transition-detection data register	W		XXXXXXXX _B
0003F9 _H					XXXXXXXX _B
0003FA _H					XXXXXXXX _B
0003FB _H					XXXXXXXX _B
0003FC _H	BSRR	Bit search module detection result register	R		XXXXXXXX _B
0003FD _H					XXXXXXXX _B
0003FE _H					XXXXXXXX _B
0003FF _H					XXXXXXXX _B

(Continued)

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Address	Register name (abbreviated)	Register name	Read/write	Resources name	Initial value
000400 _H	ICR00	Interrupt control register 0	R/W	Interrupt controller	---11111 _B
000401 _H	ICR01	Interrupt control register 1	R/W		---11111 _B
000402 _H	ICR02	Interrupt control register 2	R/W		---11111 _B
000403 _H	ICR03	Interrupt control register 3	R/W		---11111 _B
000404 _H	ICR04	Interrupt control register 4	R/W		---11111 _B
000405 _H	ICR05	Interrupt control register 5	R/W		---11111 _B
000406 _H	ICR06	Interrupt control register 6	R/W		---11111 _B
000407 _H	ICR07	Interrupt control register 7	R/W		---11111 _B
000408 _H	ICR08	Interrupt control register 8	R/W		---11111 _B
000409 _H	ICR09	Interrupt control register 9	R/W		---11111 _B
00040A _H	ICR10	Interrupt control register 10	R/W		---11111 _B
00040B _H	ICR11	Interrupt control register 11	R/W		---11111 _B
00040C _H	ICR12	Interrupt control register 12	R/W		---11111 _B
00040D _H	ICR13	Interrupt control register 13	R/W		---11111 _B
00040E _H	ICR14	Interrupt control register 14	R/W		---11111 _B
00040F _H	ICR15	Interrupt control register 15	R/W		---11111 _B
000410 _H	ICR16	Interrupt control register 16	R/W		---11111 _B
000411 _H	ICR17	Interrupt control register 17	R/W		---11111 _B
000412 _H	ICR18	Interrupt control register 18	R/W		---11111 _B
000413 _H	ICR19	Interrupt control register 19	R/W		---11111 _B
000414 _H	ICR20	Interrupt control register 20	R/W		---11111 _B
000415 _H	ICR21	Interrupt control register 21	R/W		---11111 _B
000416 _H	ICR22	Interrupt control register 22	R/W		---11111 _B
000417 _H	ICR23	Interrupt control register 23	R/W		---11111 _B
000418 _H	ICR24	Interrupt control register 24	R/W		---11111 _B
000419 _H	ICR25	Interrupt control register 25	R/W		---11111 _B
00041A _H	ICR26	Interrupt control register 26	R/W		---11111 _B
00041B _H	ICR27	Interrupt control register 27	R/W		---11111 _B
00041C _H	ICR28	Interrupt control register 28	R/W		---11111 _B
00041D _H	ICR29	Interrupt control register 29	R/W		---11111 _B
00041E _H	ICR30	Interrupt control register 30	R/W		---11111 _B
00041F _H	ICR31	Interrupt control register 31	R/W		---11111 _B

(Continued)

Address	Register name (abbreviated)	Register name	Read/write	Resources name	Initial value
000420 _H to 00042E _H	(Vacancy)				
00042F _H	ICR47	Interrupt control register 47	R/W	Interrupt controller	---11111 _B
000430 _H	DICR	Delayed interrupt control register	R/W		-----0 _B
000431 _H	HRCL	Hold request cancel request level setting register	R/W		---11111 _B
000432 _H to 00047F _H	(Vacancy)				
000480 _H	RSRR/WTCR	Reset cause register/ watchdog cycle control register	R/W	Clock generator	1XXXX-00 _B
000481 _H	STCR	Standby control register	R/W		000111-- _B
000482 _H	PDRR	DMA controller request squelch register	R/W		----0000 _B
000483 _H	CTBR	Timebase timer clear register	W		XXXXXXXX _B
000484 _H	GCR	Gear control register	R/W		110011-1 _B
000485 _H	WPR	Watchdog reset occurrence postpone register	W		XXXXXXXX _B
000486 _H 000487 _H	(Vacancy)				
000488 _H	PCTR	PLL control register	R/W	PLL control	00--0--- _B
000489 _H to 0005FF _H	(Vacancy)				
000600 _H	DDR3	Port 3 data direction register	W	Port 3	00000000 _B
000601 _H	DDR2	Port 2 data direction register	W	Port 2	00000000 _B
000602 _H 000603 _H	(Vacancy)				
000604 _H	DDR7	Port 7 data direction register	W	Port 7	-----0 _B
000605 _H	DDR6	Port 6 data direction register	W	Port 6	00000000 _B
000606 _H	DDR5	Port 5 data direction register	W	Port 5	00000000 _B
000607 _H	DDR4	Port 4 data direction register	W	Port 4	00000000 _B
000608 _H	DDRB	Port B data direction register	W	Port B	00000000 _B
000609 _H	DDRA	Port A data direction register	W	Port A	-0000000 _B
00060A _H	(Vacancy)				
00060B _H	DDR8	Port 8 data direction register	W	Port 8	--000000 _B

(Continued)

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Address	Register name (abbreviated)	Register name	Read/ write	Resources name	Initial value
00060C _H	ASR1	Area select register 1	W	External bus interface	00000000 _B
00060D _H					00000001 _B
00060E _H	AMR1	Area mask register 1	W		00000000 _B
00060F _H					00000000 _B
000610 _H	ASR2	Area select register 2	W		00000000 _B
000611 _H					00000010 _B
000612 _H	AMR2	Area mask register 2	W		00000000 _B
000613 _H					00000000 _B
000614 _H	ASR3	Area select register 3	W		00000000 _B
000615 _H					00000011 _B
000616 _H	AMR3	Area mask register 3	W		00000000 _B
000617 _H					00000000 _B
000618 _H	ASR4	Area select register 4	W		00000000 _B
000619 _H					00000100 _B
00061A _H	AMR4	Area mask register 4	W		00000000 _B
00061B _H					00000000 _B
00061C _H	ASR5	Area select register 5	W		00000000 _B
00061D _H					00000101 _B
00061E _H	AMR5	Area mask register 5	W		00000000 _B
00061F _H					00000000 _B
000620 _H	AMD0	Area mode register 0	R/W		---00111 _B
000621 _H	AMD1	Area mode register 1	R/W		0--00000 _B
000622 _H	AMD32	Area mode register 32	R/W		00000000 _B
000623 _H	AMD4	Area mode register 4	R/W		0--00000 _B
000624 _H	AMD5	Area mode register 5	R/W		0--00000 _B
000625 _H	DSCR	DRAM signal control register	W		00000000 _B
000626 _H	RFCR	Refresh control register	R/W		--XXXXXX _B
000627 _H					00---000 _B
000628 _H	EPCR0	External pin control register 0	W		----1100 _B
000629 _H					-1111111 _B
00062A _H	EPCR1	External pin control register 1	W		-----1 _B
00062B _H					11111111 _B
00062C _H	DMCR4	DRAM control register 4	R/W		00000000 _B
00062D _H					0000000- _B
00062E _H	DMCR5	DRAM control register 5	R/W		00000000 _B
00062F _H					0000000- _B

(Continued)

(Continued)

Address	Register name (abbreviated)	Register name	Read/write	Resources name	Initial value
000630 _H to 0007BF _H	(Vacancy)				
0007C0 _H	FSTR	FLASH memory status register	R/W	FLASH memory	000XXXX0 _B
0007C1 _H to 0007FD _H	(Vacancy)				
0007FE _H	LER	Little endian register	W	External bus interface	-----000 _B
0007FF _H	MODR	Mode register	W		XXXXXXXX _B

About Programming

R/W: Readable and writable

R: Read only

W: Write only

Explanation of initial values

0: The initial value of this bit is "0".

1: The initial value of this bit is "1".

X: The initial value of this bit is undefined.

–: This bit is not used. The initial value of this bit is undefined.

RMW system instructions (RMW: Read Modify Write)

AND	Rj, @ Ri	OR	Rj, @ Ri	EOR	Rj, @ Ri
ANDH	Rj, @ Ri	ORH	Rj, @ Ri	EORH	Rj, @ Ri
ANDB	Rj, @ Ri	ORB	Rj, @ Ri	EORB	Rj, @ Ri
BANDL	#μ4, @ Ri	BORL	#μ4, @ Ri	BEORL	#μ4, @ Ri
BANDH	#μ4, @ Ri	BORH	#μ4, @ Ri	BEORH	#μ4, @ Ri

Notes : • Never execute a RMW system instruction to the resistor has a write only bit.

- The area "vacancy" on the I/O map is reserved area. Access to this area are deal with to an internal area. No access signals to the external area would be generated.

■ INTERRUPT CAUSES, INTERRUPT VECTORS AND INTERRUPT CONTROL REGISTER ALLOCATIONS

Interrupt causes	Interrupt number		Interrupt level		TBR default address
	Decimal	Hexadecimal	Register	Offset	
Reset	0	00	—	3FC _H	000FFFFC _H
Reserved for system	1	01	—	3F8 _H	000FFFF8 _H
Reserved for system	2	02	—	3F4 _H	000FFFF4 _H
Reserved for system	3	03	—	3F0 _H	000FFFF0 _H
Reserved for system	4	04	—	3EC _H	000FFFE _C
Reserved for system	5	05	—	3E8 _H	000FFFE8 _H
Reserved for system	6	06	—	3E4 _H	000FFFE4 _H
Reserved for system	7	07	—	3E0 _H	000FFFE0 _H
Reserved for system	8	08	—	3DC _H	000FFFD _C
Reserved for system	9	09	—	3D8 _H	000FFFD8 _H
Reserved for system	10	0A	—	3D4 _H	000FFFD4 _H
Reserved for system	11	0B	—	3D0 _H	000FFFD0 _H
Reserved for system	12	0C	—	3CC _H	000FFFDC _H
Reserved for system	13	0D	—	3C8 _H	000FFFDC _H
Exception for undefined instruction	14	0E	—	3C4 _H	000FFFDC _H
NMI request	15	0F	F _H fixed	3C0 _H	000FFFDC _H
External interrupt 0	16	10	ICR00	3BC _H	000FFFBC _H
External interrupt 1	17	11	ICR01	3B8 _H	000FFFBC _H
External interrupt 2	18	12	ICR02	3B4 _H	000FFFBC _H
External interrupt 3	19	13	ICR03	3B0 _H	000FFFBC _H
UART0 receive complete	20	14	ICR04	3AC _H	000FFFAC _H
UART1 receive complete	21	15	ICR05	3A8 _H	000FFFAC _H
UART2 receive complete	22	16	ICR06	3A4 _H	000FFFAC _H
UART0 transmit complete	23	17	ICR07	3A0 _H	000FFFAC _H
UART1 transmit complete	24	18	ICR08	39C _H	000FFF9C _H
UART2 transmit complete	25	19	ICR09	398 _H	000FFF98 _H
DMAC0 (complete, error)	26	1A	ICR10	394 _H	000FFF94 _H
DMAC1 (complete, error)	27	1B	ICR11	390 _H	000FFF90 _H
DMAC2 (complete, error)	28	1C	ICR12	38C _H	000FFF8C _H
DMAC3 (complete, error)	29	1D	ICR13	388 _H	000FFF88 _H
DMAC4 (complete, error)	30	1E	ICR14	384 _H	000FFF84 _H
DMAC5 (complete, error)	31	1F	ICR15	380 _H	000FFF80 _H

(Continued)

Interrupt causes	Interrupt number		Interrupt level		TBR default address
	Decimal	Hexadecimal	Register	Offset	
DMAC6 (complete, error)	32	20	ICR16	37C _H	000FFF7C _H
DMAC7 (complete, error)	33	21	ICR17	378 _H	000FFF78 _H
A/D converter (successive approximation conversion type)	34	22	ICR18	374 _H	000FFF74 _H
16-bit reload timer 0	35	23	ICR19	370 _H	000FFF70 _H
16-bit reload timer 1	36	24	ICR20	36C _H	000FFF6C _H
16-bit reload timer 2	37	25	ICR21	368 _H	000FFF68 _H
PWM 0	38	26	ICR22	364 _H	000FFF64 _H
PWM 1	39	27	ICR23	360 _H	000FFF60 _H
PWM 2	40	28	ICR24	35C _H	000FFF5C _H
PWM 3	41	29	ICR25	358 _H	000FFF58 _H
U-TIMER 0	42	2A	ICR26	354 _H	000FFF54 _H
U-TIMER 1	43	2B	ICR27	350 _H	000FFF50 _H
U-TIMER 2	44	2C	ICR28	34C _H	000FFF4C _H
FLASH memory	45	2D	ICR29	348 _H	000FFF48 _H
Reserved for system	46	2E	ICR30	344 _H	000FFF44 _H
Reserved for system	47	2F	ICR31	340 _H	000FFF40 _H
Reserved for system	48	30	—	33C _H	000FFF3C _H
Reserved for system	49	31	—	338 _H	000FFF38 _H
Reserved for system	50	32	—	334 _H	000FFF34 _H
Reserved for system	51	33	—	330 _H	000FFF30 _H
Reserved for system	52	34	—	32C _H	000FFF2C _H
Reserved for system	53	35	—	328 _H	000FFF28 _H
Reserved for system	54	36	—	324 _H	000FFF24 _H
Reserved for system	55	37	—	320 _H	000FFF20 _H
Reserved for system	56	38	—	31C _H	000FFF1C _H
Reserved for system	57	39	—	318 _H	000FFF18 _H
Reserved for system	58	3A	—	314 _H	000FFF14 _H
Reserved for system	59	3B	—	310 _H	000FFF10 _H
Reserved for system	60	3C	—	30C _H	000FFF0C _H
Reserved for system	61	3D	—	308 _H	000FFF08 _H
Reserved for system	62	3E	—	304 _H	000FFF04 _H
Delayed interrupt cause bit	63	3F	ICR47	300 _H	000FFF00 _H

(Continued)

MB91F109

(Continued)

Interrupt causes	Interrupt number		Interrupt level		TBR default address
	Decimal	Hexadecimal	Register	Offset	
Reserved for system (used in REALOS*)	64	40	—	2FC _H	000FFEFC _H
Reserved for system (used in REALOS*)	65	41	—	2F8 _H	000FFE8 _H
Used in INT instructions	66 to 255	42 to FF	—	2F4 _H to 000 _H	000FFE4 _H to 000FFD00 _H

*: When using in REALOS/FR, interrupt 0x40, 0x41 for system code.

■ PERIPHERAL RESOURCES

1. I/O Ports

There are 2 types of I/O port register structure; port data register (PDR0 to PDRF) and data direction register (DDR0 to DDRF), where bits PDR0 to PDRF and bits DDR0 to DDRF corresponds respectively. Each bit on the register corresponds to an external pin. In port registers input/output register of the port configures input/output function of the port, while corresponding bit (pin) configures input/output function in data direction registers. Bit “0” specifies input and “1” specifies output.

- For input (DDR = “0”) setting;
PDR reading operation: reads level of corresponding external pin.
PDR writing operation: writes set value to PDR.
- For output (DDR = “1”) setting;
PDR reading operation: reads PDR value.
PDR writing operation: outputs PDR value to corresponding external pin.

(1) Register configuration

• Port data register

Address	bit 7	bit 0	Initial value	
000001 _H	PDR2		XXXXXXXX _B	(R/W)
000000 _H	PDR3		XXXXXXXX _B	(R/W)
000007 _H	PDR4		XXXXXXXX _B	(R/W)
000006 _H	PDR5		XXXXXXXX _B	(R/W)
000005 _H	PDR6		XXXXXXXX _B	(R/W)
000004 _H	PDR7		- - - - - X _B	(R/W)
00000B _H	PDR8		- - XXXXXX _B	(R/W)
000009 _H	PDRA		- XXXXXX _B	(R/W)
000008 _H	PDRB		XXXXXXXX _B	(R/W)
000012 _H	PDRE		XXXXXXXX _B	(R/W)
000013 _H	PDRF		XXXXXXXX _B	(R/W)

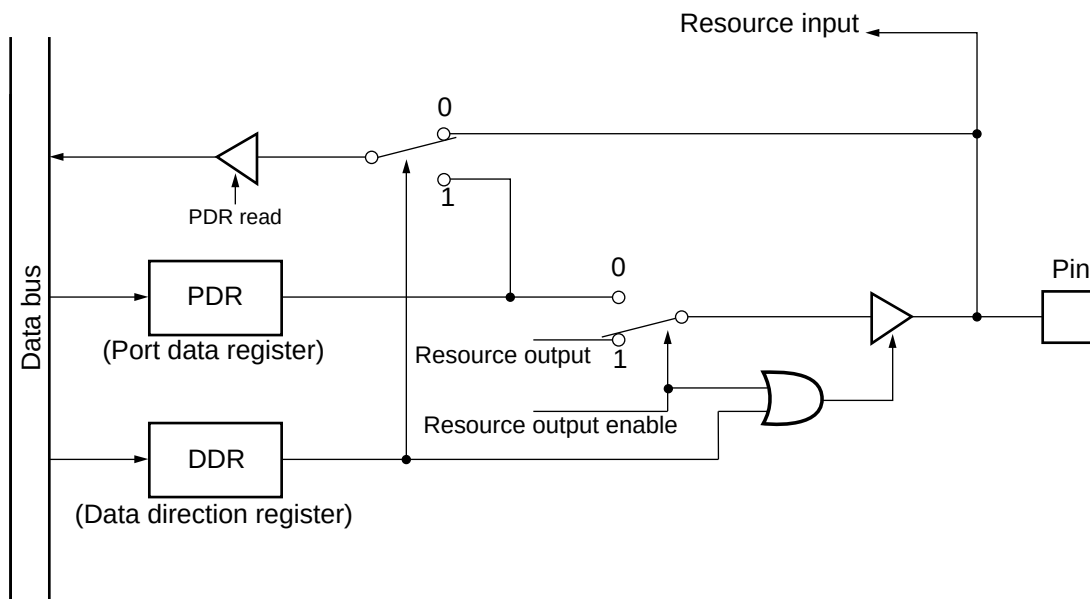
() :Access
R/W :Readable and writable
X :Indeterminate

• Data direction register

Address	bit 7	bit 0	Initial value	
000601 _H	DDR2		00000000 _B	(W)
000600 _H	DDR3		00000000 _B	(W)
000607 _H	DDR4		00000000 _B	(W)
000606 _H	DDR5		00000000 _B	(W)
000605 _H	DDR6		00000000 _B	(W)
000604 _H	DDR7		- - - - - 0 _B	(W)
00060B _H	DDR8		- - 000000 _B	(W)
000609 _H	DDRA		- 0000000 _B	(W)
000608 _H	DDRB		00000000 _B	(W)
0000D2 _H	DDRE		00000000 _B	(W)
0000D3 _H	DDRF		00000000 _B	(W)

() : Access
W : Write only
- : Unused

(2) Block diagram



2. DMA Controller (DMAC)

The DMA controller is a module embedded in FR family devices, and performs DMA (direct memory access) transfer.

DMA transfer performed by the DMA controller transfers data without intervention of CPU, contributing to enhanced performance of the system.

- 8 channels
- Mode : single/block transfer, burst transfer and continuous transfer: 3 kinds of transfer
- Transfer all through the area
- Max 65536 of transfer cycles
- Interrupt function right after the transfer
- Selectable for address transfer increase/decrease by the software
- External transfer request input pin, external transfer request accept output pin, external transfer complete output pin three pins for each

(1) Registers configuration

• DMAC internal registers

- DMAC parameter descriptor pointer

Address	bit 31	bit 0	Initial value	
00000200 _H	DPDP		XXXXXXXX _B	(R/W)
			XXXXXXXX _B	
			XXXXXXXX _B	
			X0000000 _B	

- DMAC control status register

Address	bit 31	bit 0	Initial value	
00000204 _H	DACSR		00000000 _B	(R/W)
			00000000 _B	
			00000000 _B	
			00000000 _B	

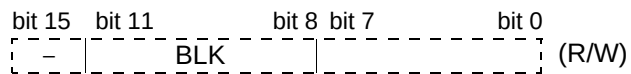
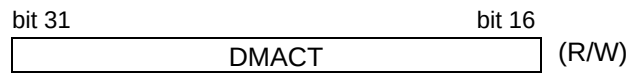
- DMAC pin control register

Address	bit 31	bit 0	Initial value	
00000208 _H	DATCR		XXXXXXXX _B	(R/W)
			XX000000 _B	
			XX000000 _B	
			XX000000 _B	

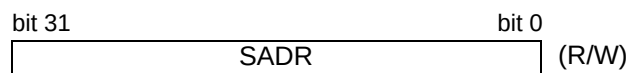
() :Access
 R/W :Readable and writable
 X :Indeterminate

- **DMAC descriptor**

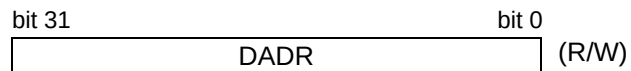
- The first word of descriptor



- The second word of descriptor

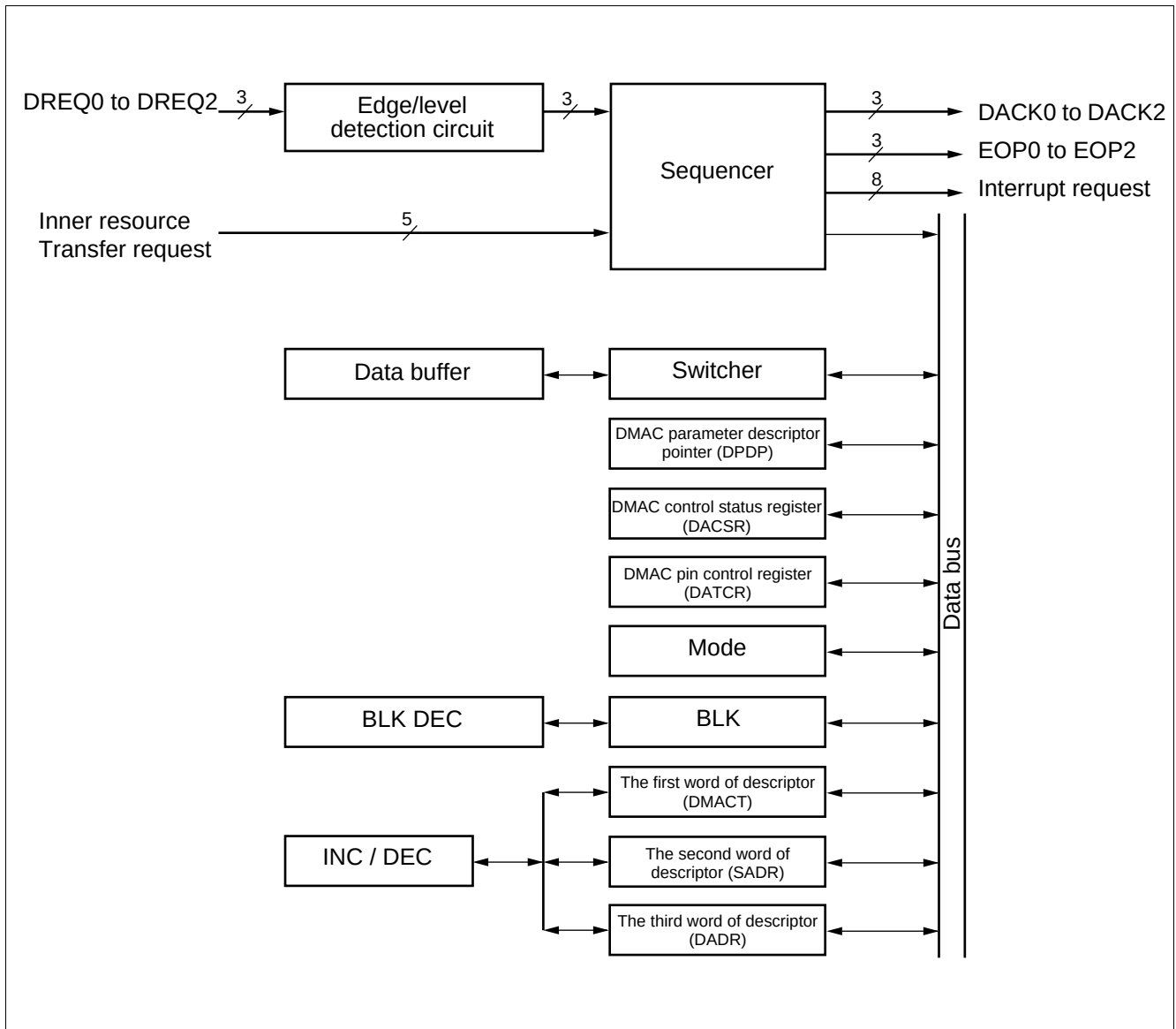


- The third word of descriptor



R/W: Readable and writable

(2) Block diagram



3. UART

The UART is a serial I/O port for supporting asynchronous (start-stop system) communication or CLK synchronous communication, and it has the following features.

The MB91F109 consists of 3 channels of UART.

- Full double double buffer
- Both a synchronous (start-stop system) communication and CLK synchronous communication are available.
- Supporting multi-processor mode
- Perfect programmable baud rate
 - Any baud rate can be set by internal timer (refer to section "4. U-TIMER").
- Any baud rate can be set by external clock.
- Error checking function (parity, framing and overrun)
- Transfer signal: NRZ code
- Enable DMA transfer/start by interrupt.

(1) Register configuration

- Serial control register 0 to 2

Address	bit 15	bit 8	bit 7	bit 0	Initial value
SCR0 : 00001E _H	SCR0 to SCR2				0 0 0 0 1 0 0 _B (R/W)
SCR1 : 000022 _H					
SCR2 : 000026 _H					

- Serial model register 0 to 2

Address	bit 15	bit 8	bit 7	bit 0	Initial value
SMR0 : 00001F _H	(SCR)				0 0 - - 0 - 0 0 _B (R/W)
SMR1 : 000023 _H					
SMR2 : 000027 _H					

- Serial status register 0 to 2

Address	bit 15	bit 8	bit 7	bit 0	Initial value
SSR0 : 00001C _H	SSR0 to SSR2				0 0 0 1 - 0 0 _B (R/W)
SSR1 : 000020 _H					
SSR2 : 000024 _H					

- Serial input data register 0 to 2

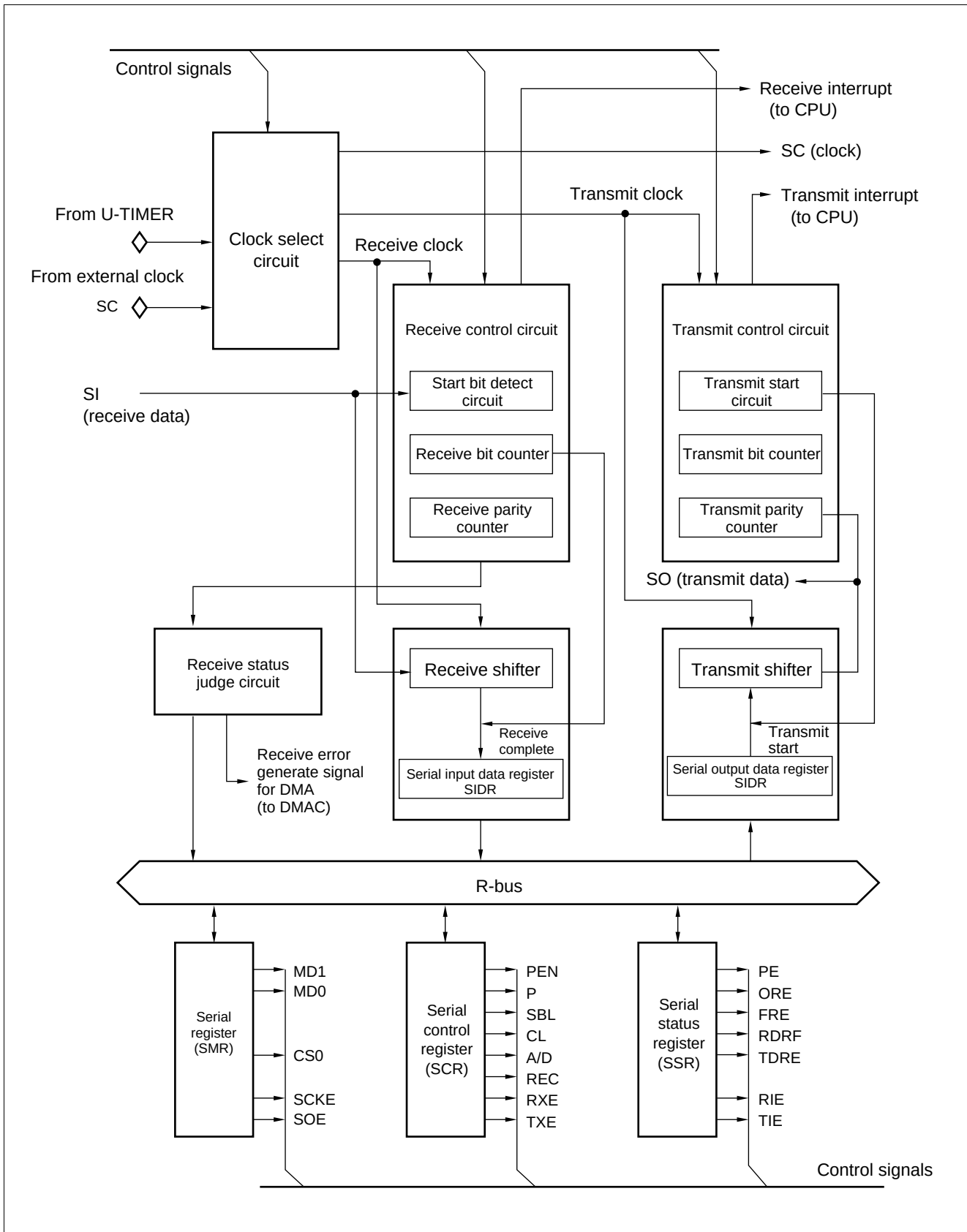
Address	bit 15	bit 8	bit 7	bit 0	Initial value
SIDR0 : 00001D _H	(SSR)				X X X X X X X _B (R)
SIDR1 : 000021 _H					
SIDR2 : 000025 _H					

- Serial output data register 0 to 2

Address	bit 15	bit 8	bit 7	bit 0	Initial value
SODR0 : 00001D _H	(SSR)				X X X X X X X _B (W)
SODR1 : 000021 _H					
SODR2 : 000025 _H					

() :Access
 R/W :Readable and writable
 - :Unused
 X :Indeterminate

(2) Block diagram



4. U-TIMER (16-bit Timer for UART Baud Rate Generation)

The U-TIMER is a 16-bit timer for generating UART baud rate. Combination of chip operating frequency and reload value of U-TIMER allows flexible setting of baud rate.

The U-TIMER operates as an interval timer by using interrupt issued on counter underflow.

The MB91F109 has 3 channel U-TIMER embedded on the chip. When used as an interval timer, two couple of U-TIMER (ch0, ch1) can be cascaded and an interval of up to $2^{32} \times \phi$ can be counted.

(1) Register configuration

- U-TIMER register ch.0 to ch.2

Address	bit 15	bit 0	Initial value
UTIM0 : 00000078 _H	UTIM0 to UTIM2		0 0 0 0 0 0 0 0 _B (R)
UTIM1 : 0000007C _H			0 0 0 0 0 0 0 0 _B
UTIM2 : 00000080 _H			

- U-TIMER reload register ch.0 to ch.2

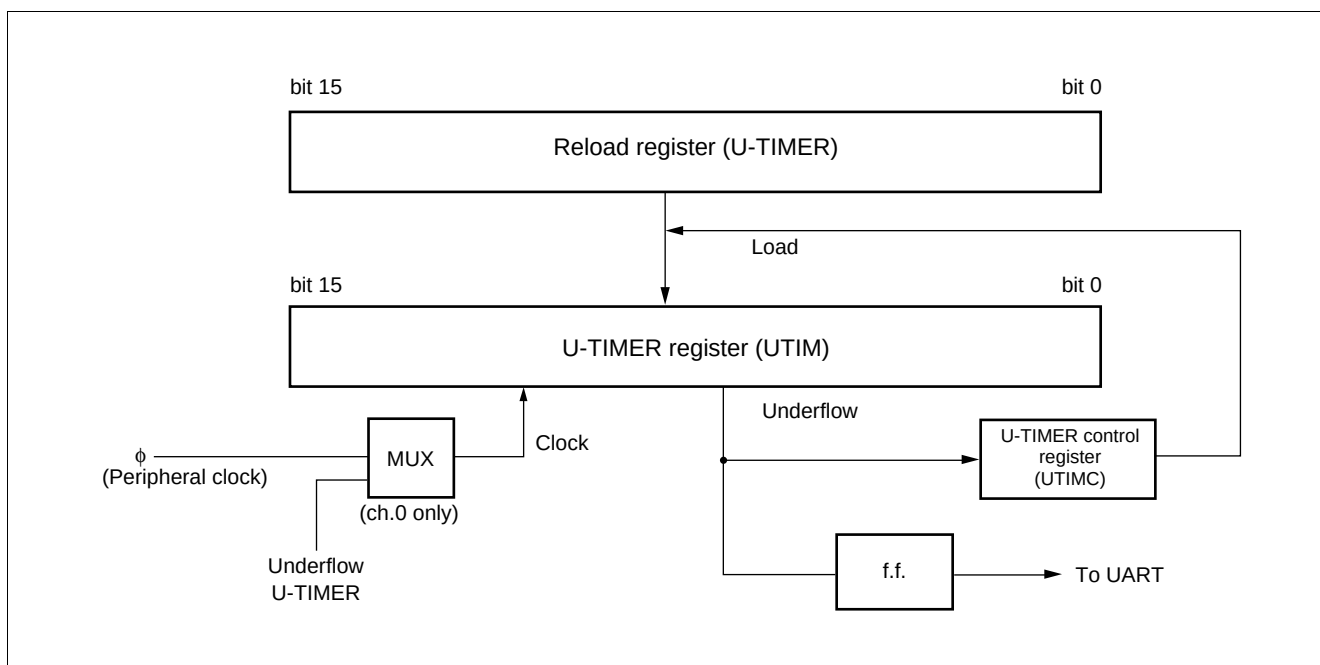
Address	bit 15	bit 0	Initial value
UTIMR0 : 00000078 _H	UTIMR0 to UTIMR2		0 0 0 0 0 0 0 0 _B (W)
UTIMR1 : 0000007C _H			0 0 0 0 0 0 0 0 _B
UTIMR2 : 00000080 _H			

- U-TIMER control register ch.0 to ch.2

Address	bit 15	bit 8	bit 7	bit 0	Initial value
UTIMC0 : 0000007B _H	(Vacancy) UTIMC0 to UTIMC2				0 - - 0 0 0 0 1 _B (R/W)
UTIMC1 : 0000007F _H					
UTIMC2 : 00000083 _H					

() :Access
R/W :Readable and writable
- :Unused

(2) Block diagram



5. PWM Timer

The PWM timer can output high accurate PWM waves efficiently.

MB91F109 has inner 4-channel PWM timers, and has the following features.

- Each channel consists of a 16-bit down counter, a 16-bit data register with a buffer for cycle setting, a 16-bit compare register with a buffer for duty setting, and a pin controller.
- The count clock of a 16-bit down counter can be selected from the following four inner clocks.
Inner clock ϕ , $\phi/4$, $\phi/16$, $\phi/64$
- The counter value can be initialized “FFFF_H” by the resetting or the counter borrow.
- PWM output (each channel)

(1) Register configuration

- Control status register H0 to 3

Address	bit 15	bit 8	bit 7	bit 0	Initial value
PCNH0 : 0000E6 _H	PCNH0 to PCNH3 (PCNL)				0 0 0 0 0 0 0 - _B (R/W)
PCNH1 : 0000EE _H					
PCNH2 : 0000F6 _H					
PCNH3 : 0000FE _H					

- Control status register L0 to 3

Address	bit 15	bit 0	Initial value
PCNL0 : 0000E7 _H	(PCNH) PCNL0 to PCNL3	0 0 0 0 0 0 0 0 _B (R/W)	
PCNL1 : 0000EF _H			
PCNL2 : 0000F7 _H			
PCNL3 : 0000FF _H			

- PWM cycle setting register 0 to 3

Address	bit 15	bit 0	Initial value
PCSR0 : 0000E2 _H	PCSR0 to PCSR3		X X X X X X X _B X X X X X X X _B (W)
PCSR1 : 0000EA _H			
PCSR2 : 0000F2 _H			
PCSR3 : 0000FA _H			

- PWM duty setting register 0 to 3

Address	bit 15	bit 0	Initial value
PDUT0 : 0000E4 _H	PDUT0 to PDUT3		X X X X X X X _B X X X X X X X _B (W)
PDUT1 : 0000EC _H			
PDUT2 : 0000F4 _H			
PDUT3 : 0000FC _H			

- PWM timer register 0 to 3

Address	bit 15	bit 0	Initial value
PTMR0 : 0000E0 _H	PTMR0 to PTMR3		1 1 1 1 1 1 1 _B (R) 1 1 1 1 1 1 1 _B
PTMR1 : 0000E8 _H			
PTMR2 : 0000F0 _H			
PTMR3 : 0000F8 _H			

- General control register 1, 2

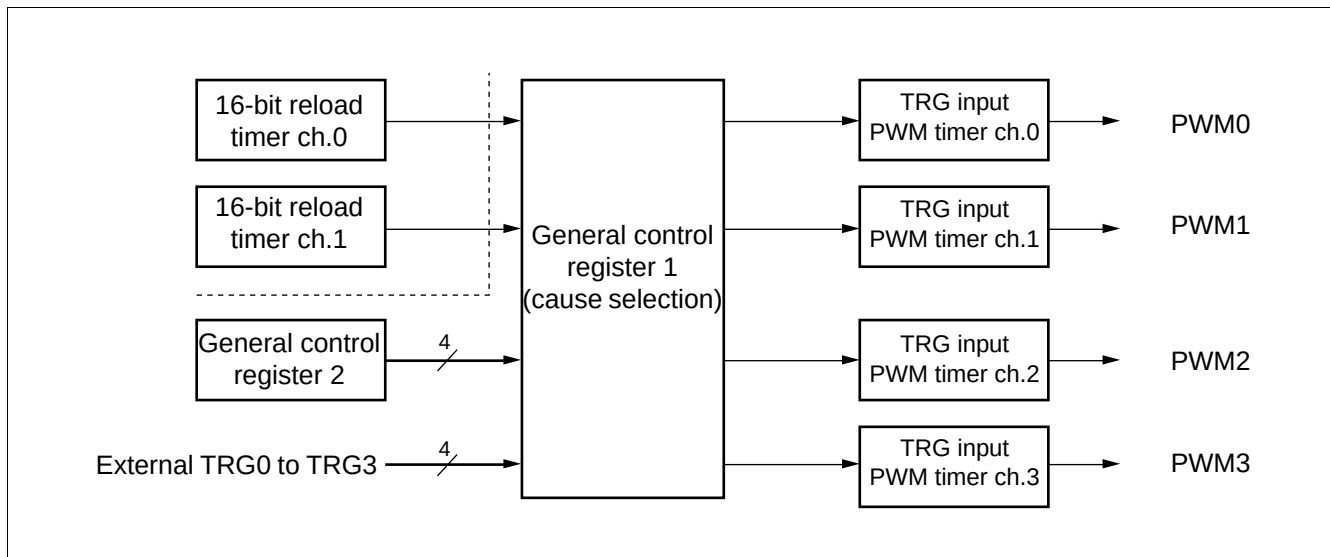
Address	bit 15	bit 0	Initial value
GCN1 : 0000DC _H	GCN1		0 0 1 1 0 0 1 0 _B 0 0 0 1 0 0 0 0 _B (R/W)

Address	bit 15	bit 8	bit 7	bit 0	Initial value
GCN1 : 0000DF _H	(Vacancy) GCN2				0 0 0 0 0 0 0 0 _B (R/W)

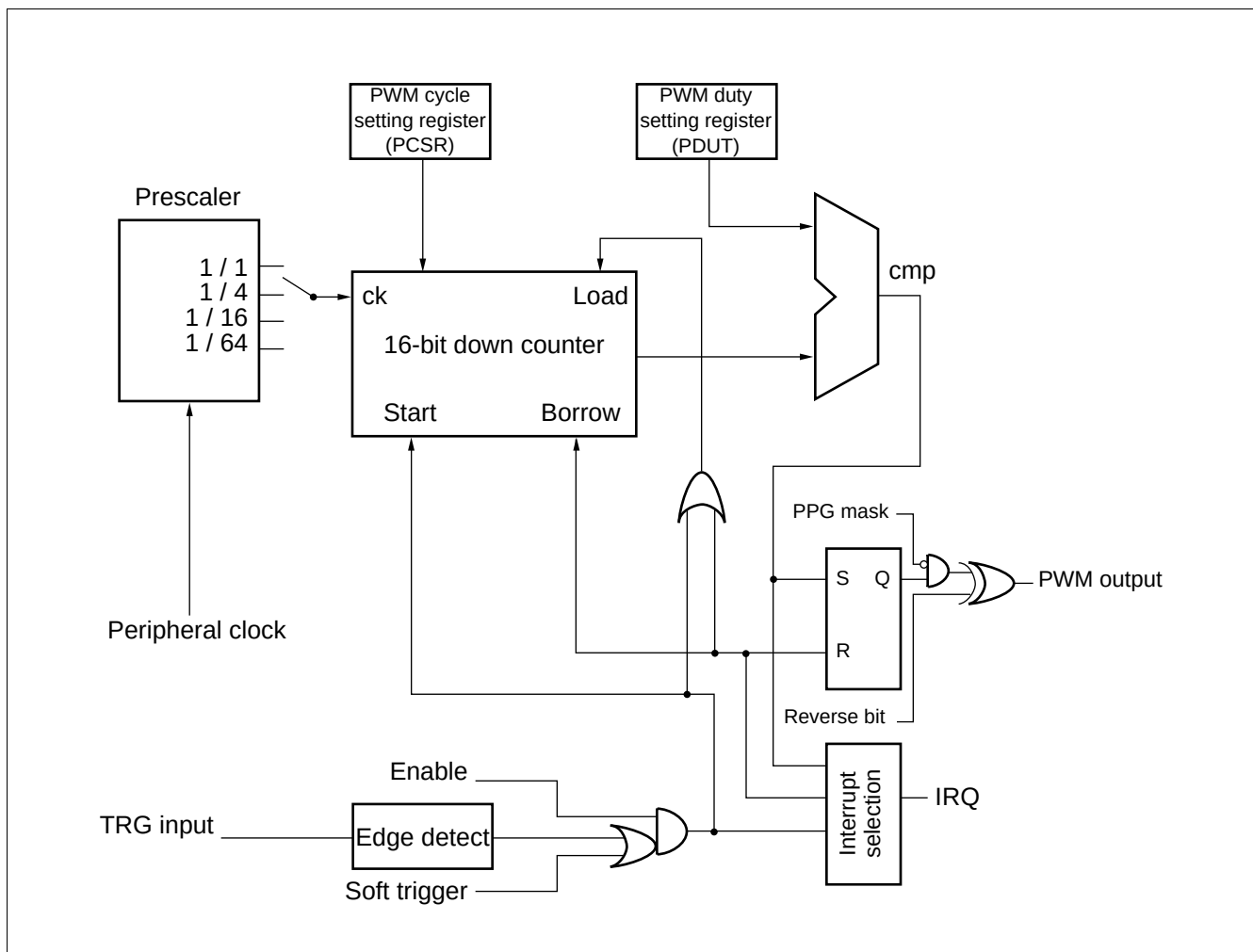
() : Access
 R/W : Readable and writable
 R : Read only
 W : Write only
 - : Unused
 X : Indeterminate

(2) Block diagram

• Block diagram (general construction)



• Block diagram (for one channel)



6. 16-bit Reload Timer

The 16-bit reload timer consists of a 16-bit down counter, a 16-bit reload timer, a prescaler for generating internal count clock and control registers.

Internal clock can be selected from 3 types of internal clocks (divided by 2/8/32 of machine clock).

The DMA transfer can be started by the interruption.

The MB91F109 consists of 3 channels of the 16-bit reload timer.

(1) Register configuration

- 16-bit reload timer control status register 0 to 2

Address	bit 15	bit 0	Initial value
TMCSR0 : 00002EH	TMCSR0 to TMCSR2		- - - 0 0 0 0 _B (R/W)
TMCSR1 : 000036H			0 0 0 0 0 0 0 0 _B
TMCSR2 : 000042H			

- 16-bit timer register 0 to 2

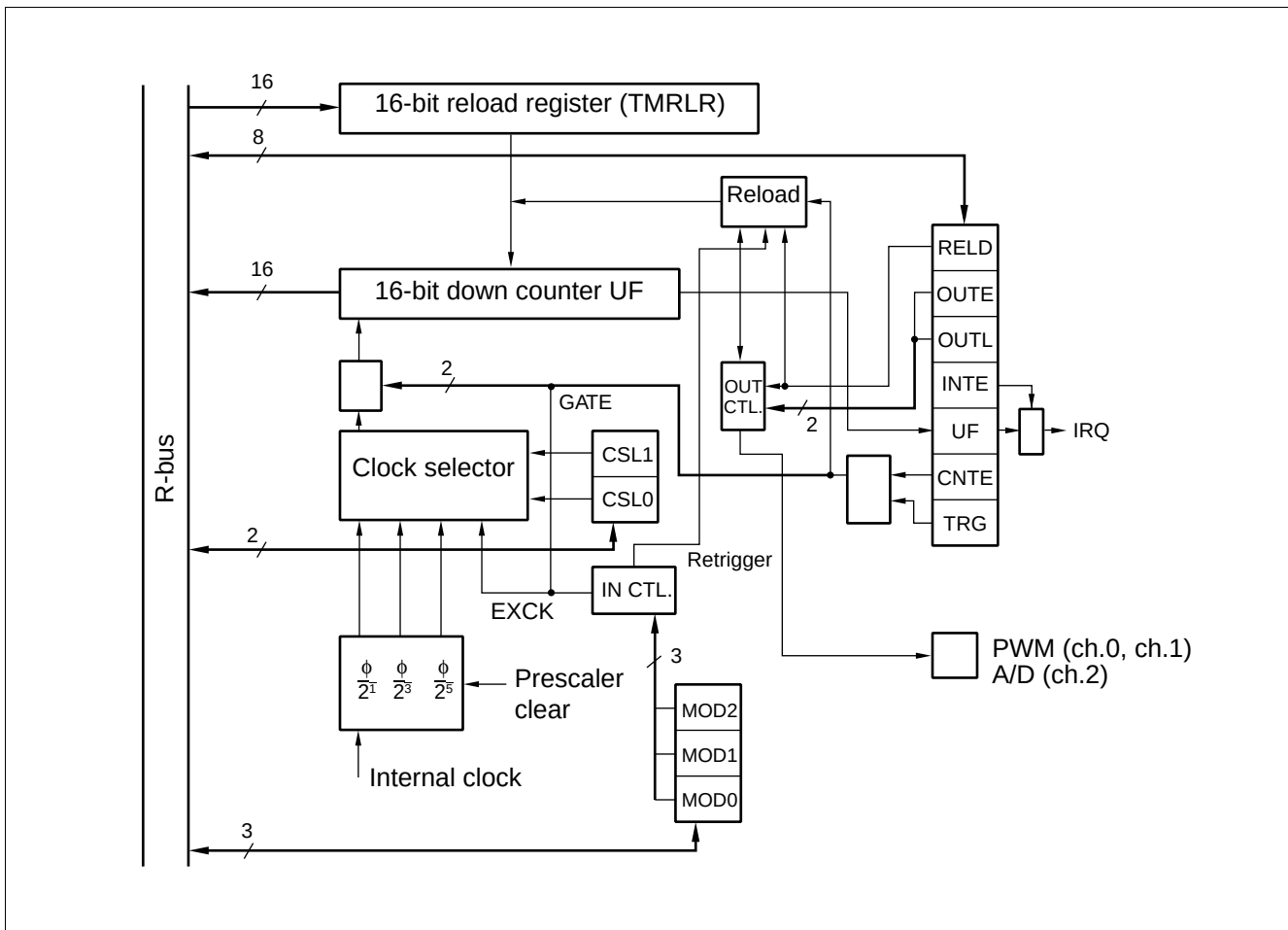
Address	bit 15	bit 0	Initial value
TMR0 : 00002AH	TMR0 to TMR2		X X X X X X X X _B (R)
TMR1 : 000032H			X X X X X X X X _B
TMR2 : 00003EH			

- 16-bit reload register 0 to 2

Address	bit 15	bit 0	Initial value
TMRLR0 : 000028H	TMRLR0 to TMRLR2		X X X X X X X X _B (W)
TMRLR1 : 000030H			X X X X X X X X _B
TMRLR2 : 00003CH			

() :Access
 R/W :Readable and writable
 R :Read Only
 W :Write Only
 - :Unused
 X :Indeterminate

(2) Block diagram



7. Bit Search Module

The bit search module detects transitions of data (0 to 1/1 to 0) on the data written on the input registers and returns locations of the transitions.

(1) Register configuration

- Bit search module 0, 1-detection data register

Address	bit 31	bit 0	Initial value
BSD0 : 000003F0 _H	BSD0, BSD1		X X X X X X X X _B
BSD1 : 000003F4 _H			X X X X X X X X _B
			X X X X X X X X _B
			X X X X X X X X _B
			(R/W)

- Bit search module transition-detection data register

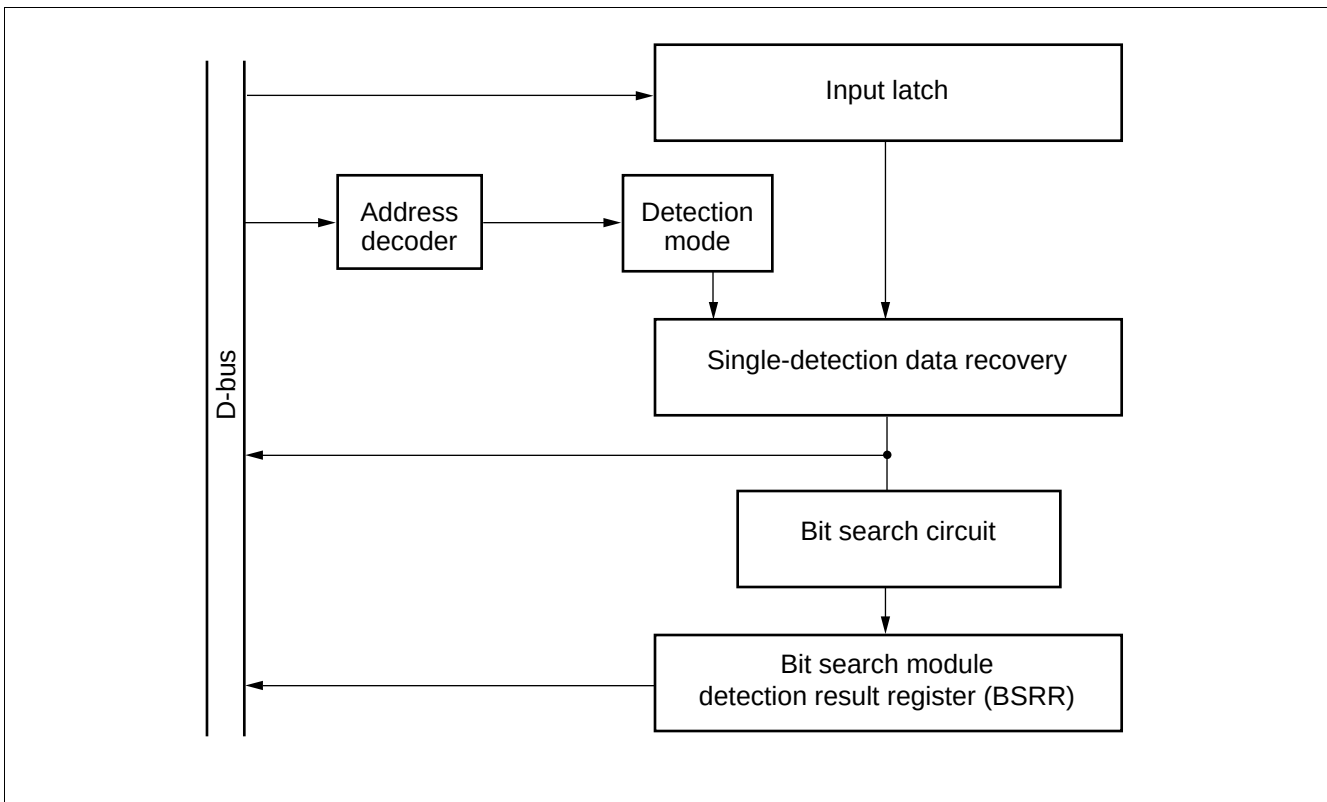
Address	bit 31	bit 0	Initial value
000003F8 _H	BSDC		X X X X X X X X _B
			X X X X X X X X _B
			X X X X X X X X _B
			X X X X X X X X _B
			(W)

- Bit search module detection result register

Address	bit 31	bit 0	Initial value
000003FC _H	BSRR		X X X X X X X X _B
			X X X X X X X X _B
			X X X X X X X X _B
			X X X X X X X X _B
			(R)

() : Access
 R/W : Readable and writable
 R : Read only
 W : Write only
 X : Indeterminate

(2) Block diagram



8. 10-bit A/D Converter (Successive Approximation Conversion Type)

The A/D converter is the module which converts an analog input voltage to a digital value, and it has following features.

- Minimum converting time: 5.6 μs/ch. (system clock: 25 MHz)
- Inner sample and hold circuit
- Resolution: 10 bits
- Analog input can be selected from 4 channels by program.
Single convert mode: 1 channel is selected and converted.
Scan convert mode: Converting continuous channels. Maximum 4 channels are programmable.
Continuous convert mode: Converting the specified channel repeatedly.
Stop convert mode: After converting one channel then stop and wait till next activation synchronizing at the beginning of conversion can be performed.
- DMA transfer operation is available by interruption.
- Operating factor can be selected from the software, the external trigger (falling edge), and 16-bit reload timer (rising edge).

(1) Register configuration

- A/D converter control status register

Address

bit 15

bit 0

0000003A_H

ADCS

Initial value

0 0 0 0 0 0 0 0_B (R/W)

0 0 0 0 0 0 0 0_B
- A/D converter data register

Address

bit 15

bit 0

00000038_H

ADCR

Initial value

0 0 0 0 0 0 X X_B (R)

X X X X X X X X_B

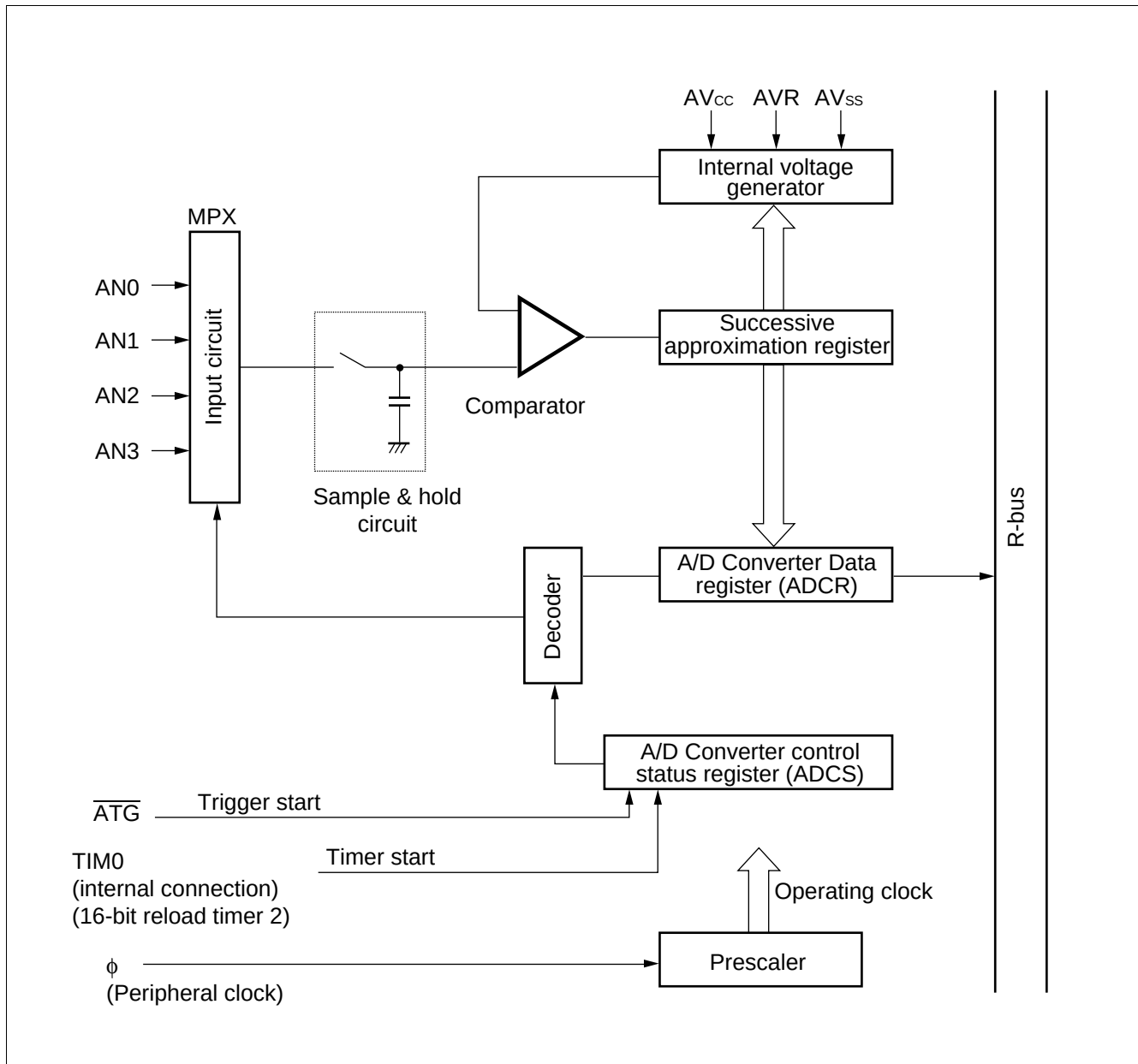
() : Access

R/W : Readable and writable

R : Read only

X : Indeterminate

(2) Block diagram



9. Interrupt Controller

The interrupt controller processes interrupt acknowledgments and arbitration between interrupts.

- Hardware Configuration

Interrupt controller is configured by ICR resistor, interrupt priority decision circuit, interrupt level, vector generation and HLDREQ cancel request, and has the following functions.

- Main Functions

NMI request/Interrupt request detection

Priority (judgement) decision (via level and vector)

Transfer of judged interrupt level to CPU

Transfer of judged interrupt vector to CPU

Return instruction from the stop mode via NMI/interrupt

Generation of HOLD request cancel request to the bus timer

(1) Register configuration

- Interrupt control register 0 to 31, 47

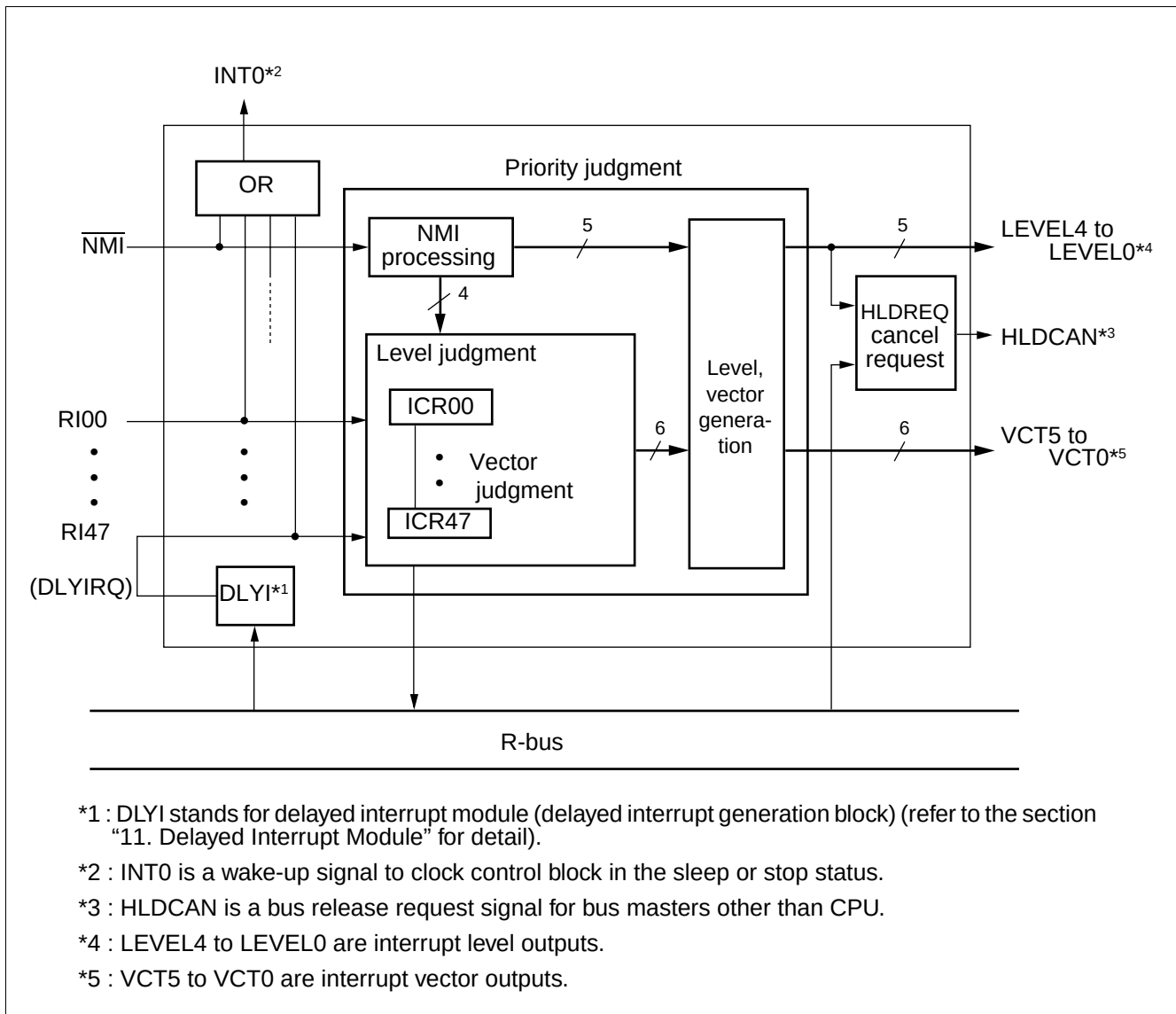
Address	bit 7	bit 0	Initial value	Address	bit 7	bit 0	Initial value
00000400 _H		ICR00	--- 11111 _B (R/W)	00000411 _H		ICR17	--- 11111 _B (R/W)
00000401 _H		ICR01	--- 11111 _B (R/W)	00000412 _H		ICR18	--- 11111 _B (R/W)
00000402 _H		ICR02	--- 11111 _B (R/W)	00000413 _H		ICR19	--- 11111 _B (R/W)
00000403 _H		ICR03	--- 11111 _B (R/W)	00000414 _H		ICR20	--- 11111 _B (R/W)
00000404 _H		ICR04	--- 11111 _B (R/W)	00000415 _H		ICR21	--- 11111 _B (R/W)
00000405 _H		ICR05	--- 11111 _B (R/W)	00000416 _H		ICR22	--- 11111 _B (R/W)
00000406 _H		ICR06	--- 11111 _B (R/W)	00000417 _H		ICR23	--- 11111 _B (R/W)
00000407 _H		ICR07	--- 11111 _B (R/W)	00000418 _H		ICR24	--- 11111 _B (R/W)
00000408 _H		ICR08	--- 11111 _B (R/W)	00000419 _H		ICR25	--- 11111 _B (R/W)
00000409 _H		ICR09	--- 11111 _B (R/W)	0000041A _H		ICR26	--- 11111 _B (R/W)
0000040A _H		ICR10	--- 11111 _B (R/W)	0000041B _H		ICR27	--- 11111 _B (R/W)
0000040B _H		ICR11	--- 11111 _B (R/W)	0000041C _H		ICR28	--- 11111 _B (R/W)
0000040C _H		ICR12	--- 11111 _B (R/W)	0000041D _H		ICR29	--- 11111 _B (R/W)
0000040D _H		ICR13	--- 11111 _B (R/W)	0000041E _H		ICR30	--- 11111 _B (R/W)
0000040E _H		ICR14	--- 11111 _B (R/W)	0000041F _H		ICR31	--- 11111 _B (R/W)
0000040F _H		ICR15	--- 11111 _B (R/W)	0000042F _H		ICR47	--- 11111 _B (R/W)
00000410 _H		ICR16	--- 11111 _B (R/W)				

- Hold request cancel request level setting register

Address	bit 7	bit 0	Initial value
00000431 _H		HRCL	- - - 1 1 1 1 1 _B (R/W)

() :Access
 R/W :Readable and writable
 — :Unused

(2) Block diagram



10. External Interrupt/NMI Control Block

The external interrupt/NMI control block controls external interrupt request signals input to $\overline{\text{NMI}}$ pin and INT0 to INT3 pins.

Detecting levels can be selected from "H", "L", rising edge and falling edge (not for $\overline{\text{NMI}}$ pin).

(1) Register configuration

- Interrupt enable register

Address	bit 15	bit 7	bit 0	Initial value
00000095 _H	(EIRR) ENIR			0 0 0 0 0 0 0 0 _B (R/W)

- External interrupt cause register

Address	bit 15	bit 8	bit 0	Initial value
00000094 _H	EIRR (ENIR)			0 0 0 0 0 0 0 0 _B (R/W)

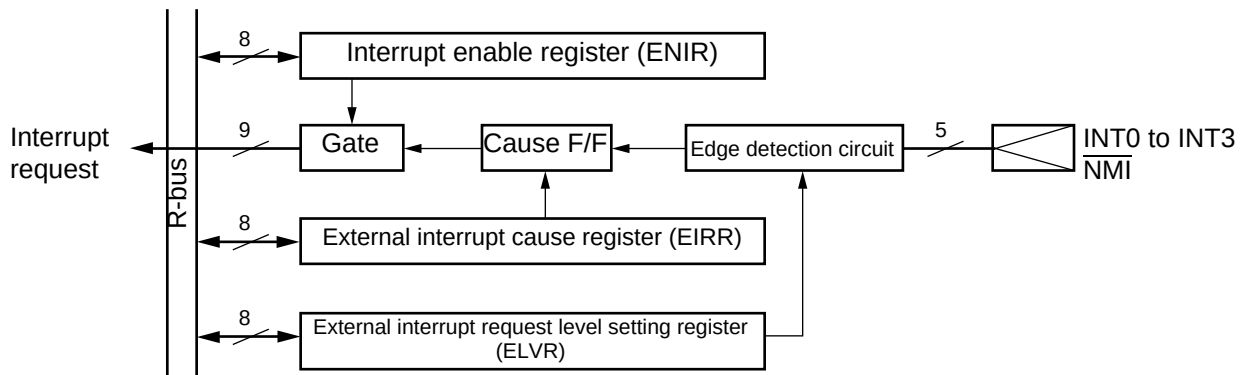
- External interrupt request level setting register

Address	bit 15	bit 0	Initial value
00000099 _H	ELVR		0 0 0 0 0 0 0 0 _B (R/W)

() :Access

R/W :Readable and writable

(2) Block diagram



11. Delayed Interrupt Module

Delayed interrupt module is a module which generates a interrupt for changing a task. By using this delayed interrupt module, an interrupt request to CPU can be generated/cancelled by the software.

Refer to the section “9. Interrupt Controller” for delayed interrupt module block diagram.

• Register configuration

- Delayed interrupt control register

Address	bit 7	bit 0	Initial value
00000430 _H	DICR		- - - - - 0 _B (R/W)
()	:Access		
R/W	:Readable and writable		
-	:Unused		

12. Clock Generation (Low-power consumption mechanism)

The clock control block is a module which undertakes the following functions.

- CPU clock generation (including gear function)
- Peripheral clock generation (including gear function)
- Reset generation and cause hold
- Standby function
- DMA request prohibit
- PLL (multiplier circuit) embedded

(1) Register configuration

- Reset cause register/watchdog cycle control register

Address	bit 15	bit 10	bit 9	bit 8	bit 0	Initial value
00000480 _H	RSRR			WTCR	(STCR)	1 X X X X - 0 0 _B (R/W)

- Standby control register

Address	bit 15	bit 7	bit 0	Initial value
00000481 _H	(RSRR/WTCR)		STCR	0 0 0 1 1 1 - - _B (R/W)

- DMA controller request squelch register

Address	bit 15	bit 8	bit 0	Initial value
00000482 _H	PDRR		(CTBR)	- - - - 0 0 0 0 _B (R/W)

- Timebase timer clear register

Address	bit 15	bit 7	bit 0	Initial value
00000483 _H	(PDRR)		CTBR	X X X X X X X X _B (W)

- Gear control register

Address	bit 15	bit 8	bit 0	Initial value
00000484 _H	GCR (WPR)			1 1 0 0 1 1 - 1 _B (R/W)

- Watchdog reset occurrence postpone register

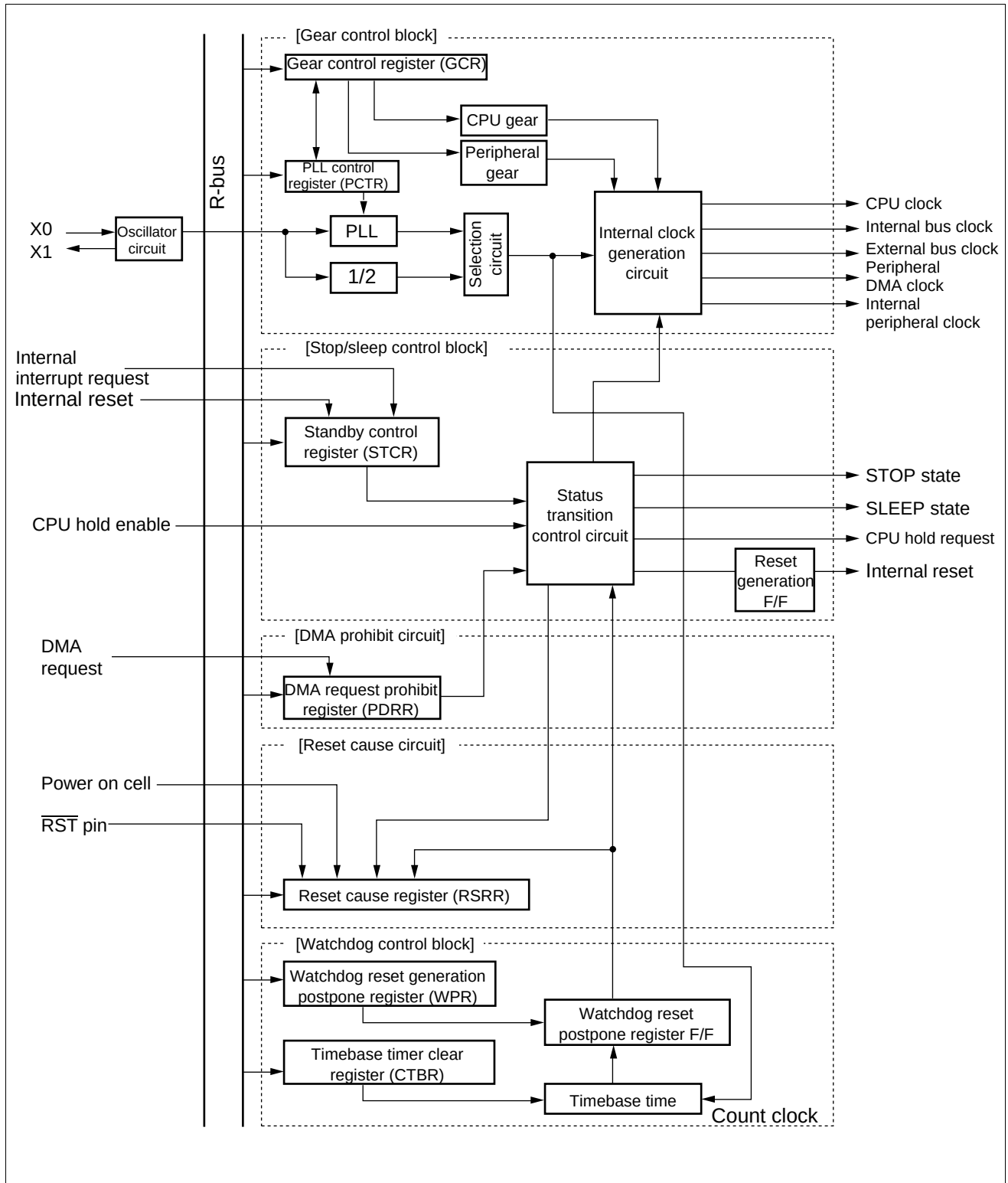
Address	bit 15	bit 7	bit 0	Initial value
00000485 _H	(GCR)		WPR	X X X X X X X X _B (W)

- PLL control register

Address	bit 15	bit 8	bit 0	Initial value
00000488 _H	PCTR (Vacancy)			0 0 - - 0 - - - _B (R/W)

() :Access
R/W :Readable and writable
R :Read Only
W :Write Only
- :Unused
X :Indeterminate

(2) Block diagram



13. External Bus Interface

The external bus interface controls the interface between the device and the external memory and also the external I/O, and has the following features.

- 25-bit (32 Mbytes) address output
- 6 independent banks owing to the chip select function.
Can be set to anywhere on the logical address space for minimum unit 64 Kbytes.
Total 32 Mbytes × 6 area setting is available by the address pin and the chip select pin.
- 8/16-bit bus width setting are available for every chip select area.
- Programmable automatic memory wait (Max for 7 cycles) can be inserted.
- DRAM interface support
Three kinds of DRAM interface: Double CAS DRAM (normally DRAM I/F)
Single CAS DRAM
Hyper DRAM
2 banks independent control (RAS, CAS, etc. control signals)
DRAM select is available from 2CAS/1WE and 1CAS/2WE.
Hi-speed page mode supported
CBR/self refresh supported
Programmable wave form
- Unused address/data pin can be used for I/O port.
- Little endian mode supported
- Without Clock doubler: Internal bus 25 MHz, external bus 25 MHz (at source oscillation 12.5 MHz)

(1) Register configuration

• Area select register 1 to 5

Address	bit 15	bit 0	Initial value
0000060C _H	ASR1		0 0 0 0 0 0 0 0 _B 0 0 0 0 0 0 0 1 _B
00000610 _H	ASR2		0 0 0 0 0 0 0 0 _B 0 0 0 0 0 0 1 0 _B
00000614 _H	ASR3		0 0 0 0 0 0 0 0 _B 0 0 0 0 0 0 1 1 _B (W)
00000618 _H	ASR4		0 0 0 0 0 0 0 0 _B 0 0 0 0 0 1 0 0 _B
0000061C _H	ASR5		0 0 0 0 0 0 0 0 _B 0 0 0 0 0 1 0 1 _B

• Area mask register 1 to 5

Address	bit 15	bit 0	Initial value
AMR1 : 0000060E _H AMR2 : 00000612 _H AMR3 : 00000616 _H AMR4 : 0000061A _H AMR5 : 0000061E _H	AMR1 to AMR5		0 0 0 0 0 0 0 0 _B (W) 0 0 0 0 0 0 0 0 _B

• Area mode register 0, 1, 32, 4, 5

Address	bit 15	bit 8	bit 7	bit 0	Initial value
AMD0 : 00000620 _H AMD1 : 00000621 _H	AMD0		AMD1		- - - 0 0 1 1 1 _B (R/W) 0 - - 0 0 0 0 0 _B
AMD32 : 00000622 _H AMD4 : 00000623 _H	AMD32		AMD4		0 0 0 0 0 0 0 0 _B 0 - - 0 0 0 0 0 _B (R/W)
AMD5 : 00000624 _H	AMD5		(DSCR)		0 - - 0 0 0 0 0 _B (R/W)

• DRAM single control register

Address	bit 15	bit 8	bit 7	bit 0	Initial value
00000625 _H	(AMD5)		DSCR		0 0 0 0 0 0 0 0 _B (W)

• Refresh control register

Address	bit 15	bit 0	Initial value
00000626 _H	RFCR		- - X X X X X _B (R/W) 0 0 - - - 0 0 _B

• External pin control register 0, 1

Address	bit 15	bit 0	Initial value
EPCR0: 00000628 _H	EPCR0		- - - - 1 1 0 0 _B (W) - 1 1 1 1 1 1 1 _B
EPCR1: 0000062A _H	EPCR1		- - - - - 1 _B (W) 1 1 1 1 1 1 1 1 _B

• DRAM control register 4, 5

Address	bit 15	bit 0	Initial value
DMCR4: 0000062C _H DMCR5: 0000062E _H	DMCR4, DMCR5		0 0 0 0 0 0 0 0 _B (R/W) 0 0 0 0 0 0 0 - _B

• Little endian register

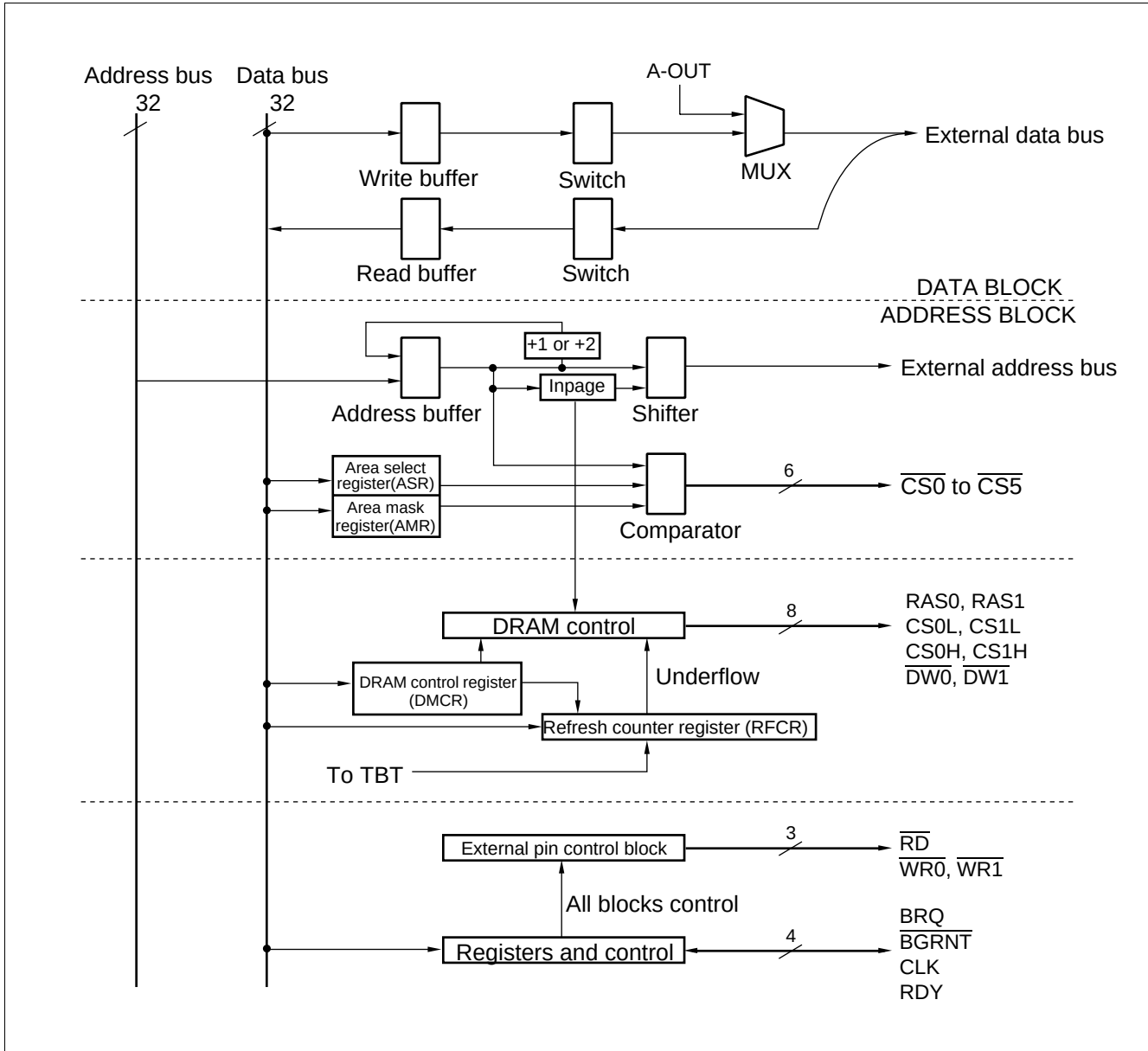
Address	bit 15	bit 8	bit 7	bit 0	Initial value
000007FE _H	LER		(MODR)		- - - - - 0 0 0 _B (W)

• Mode register

Address	bit 15	bit 8	bit 7	bit 0	Initial value
000007FF _H	(LER)		MODR		X X X X X X X _B (W)

() :Access
R/W :Readable and writable
W :Write only
- :Unused
X :Indeterminate

(2) Block diagram



■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

($V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	*1
Analog supply voltage	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	*2
Analog reference voltage	$AVRH$	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	*2
Analog pin input voltage	V_{IA}	$V_{SS} - 0.3$	$AV_{CC} + 0.3$	V	
Input voltage	V_I	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	
Output voltage	V_O	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	
"L" level maximum output current	I_{OL}	—	10	mA	*3
"L" level average output current	I_{OLAV}	—	8	mA	*4
"L" level maximum total output current	ΣI_{OL}	—	100	mA	
"L" level average total output current	ΣI_{OLAV}	—	50	mA	*5
"H" level maximum output current	I_{OH}	—	-10	mA	*3
"H" level average output current	I_{OHAV}	—	-4	mA	*4
"H" level maximum total output current	ΣI_{OH}	—	-50	mA	
"H" level average total output current	ΣI_{OHAV}	—	-20	mA	*5
Power consumption	P_D	—	500	mW	
Operating temperature	T_A	0	+70	°C	
Storage temperature	T_{stg}	-55	+150	°C	

*1 : V_{CC} must not be less than $V_{SS} - 0.3\text{ V}$.

*2 : Care must be taken that AV_{CC} and $AVRH$ do not exceed $V_{CC} + 0.3\text{ V}$, such as when turning on the device.
Also, care must be taken that $AVRH$ do not exceed AV_{CC} .

*3 : Maximum output current is a peak current value measured at a corresponding pin.

*4 : Average output current is an average current for a 100 ms period at a corresponding pin.

*5 : Average total output current is an average current for a 100 ms period for all corresponding pins.

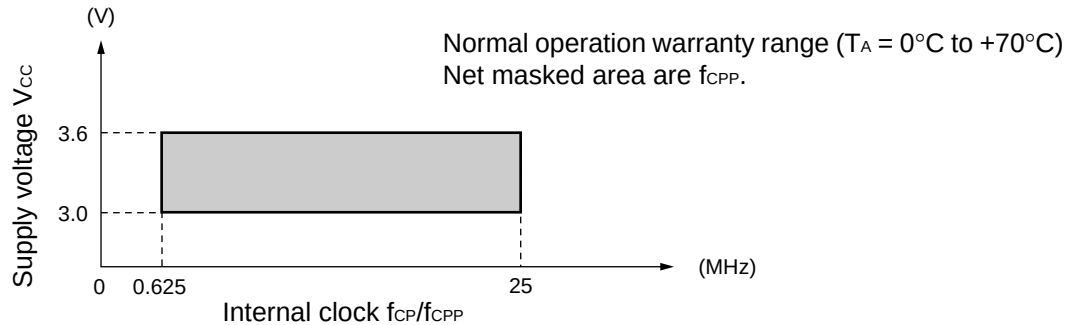
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

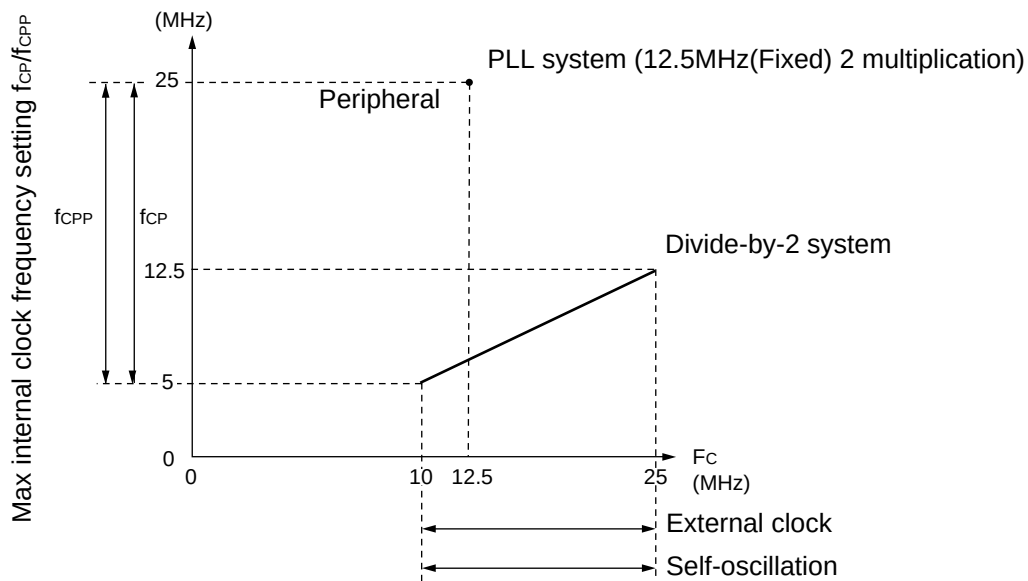
($V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	3.15	3.6	V	Normal operation
	V_{CC}	3.15	3.6	V	Retaining the RAM state in stop mode
Analog supply voltage	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 3.6$	V	
Analog reference voltage	AV_{RH}	AV_{SS}	AV_{CC}	V	
Operating temperature	T_A	0	+70	°C	

• Normal operation warranty range



• External/Internal clock setting rage



- Notes :
- When using PLL, the external clock must be used need 12.5 MHz.
 - PLL oscillation stabilizing period $> 100 \mu\text{s}$
 - The setting of internal clock must be within above ranges.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

($V_{CC} = 3.15 \text{ V to } 3.6 \text{ V}$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
“H” level input voltage	V_{IH}	Input pin except for hysteresis input	—	$0.65 \times V_{CC}$	—	$V_{CC} + 0.3$	V	
	V_{IHS}	$\overline{NMI}$, $\overline{RST}$, P40 to P47, P50 to P57, P60 to P67, P70, P81, P83 to P85, PA0 to PA6, PB0 to PB7, PE0 to PE7, PF0 to PF7	—	$0.8 \times V_{CC}$	—	$V_{CC} + 0.3$	V	Hysteresis input
“L” level input voltage	V_{IL}	Input other than following symbols	—	$V_{SS} - 0.3$	—	$0.25 \times V_{CC}$	V	
	V_{ILS}	$\overline{NMI}$, $\overline{RST}$, P40 to P47, P50 to P57, P60 to P67, P70, P81, P83 to P85, PA0 to PA6, PB0 to PB7, PE0 to PE7, PF0 to PF7	—	$V_{SS} - 0.3$	—	$0.2 \times V_{CC}$	V	Hysteresis input
“H” level output voltage	V_{OH}	P20 to P27 P30 to P37 P40 to P47 P50 to P57	$V_{CC} = 3.15 \text{ V}$ $I_{OH} = -4.0 \text{ mA}$	$V_{CC} - 0.5$	—	—	V	
“L” level output voltage	V_{OL}	P60 to P67 P70 P80 to P85	$V_{CC} = 3.15 \text{ V}$ $I_{OL} = 4.0 \text{ mA}$	—	—	0.4	V	
Input leakage current (Hi-Z output leakage current)	I_{LI}	PA0 to PA6 PB0 to PB7 PE0 to PE7 PF0 to PF7	$V_{CC} = 3.6 \text{ V}$ $0.45 \text{ V} < V_I < V_{CC}$	-5	—	+5	μA	
Pull-up resistance	R_{PULL}	$\overline{RST}$	$V_{CC} = 3.6 \text{ V}$ $V_I = 0.45 \text{ V}$	25	50	100	k Ω	
Power supply current	I_{CC}	V_{CC}	$F_C = 12.5 \text{ MHz}$ $V_{CC} = 3.3 \text{ V}$	—	75	100	mA	(2 multiplication) Operation at 25 MHz
	I_{CCS}	V_{CC}	$F_C = 12.5 \text{ MHz}$ $V_{CC} = 3.3 \text{ V}$	—	35	50	mA	Sleep mode
	I_{CCH}	V_{CC}	$T_A = +25^\circ\text{C}$ $V_{CC} = 3.3 \text{ V}$	—	1.4	150	μA	Stop mode
Input capacitance	C_{IN}	Except for V_{CC} , AV_{CC} , AV_{SS} , V_{SS}	—	—	10	—	pF	

4. FLASH Memory Programming/Erasing Characteristics

($V_{CC} = 3.15 \text{ V to } 3.6 \text{ V}$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$)

Parameter	Condition	Value			Unit	Remarks
		Min	Typ	Max		
Sector erasing time	$T_A = +25^\circ\text{C}$ $V_{CC} = 3.3 \text{ V}$	—	1.5	13.5	s	Except for the write time before internal erase operation
Chip erasing time		—	—	27.0	s	Except for the write time before internal erase operation
Byte programming time		—	16	—	μs	Except for the over head time of the system
Chip programming time		—	2.1	—	s	Except for the over head time of the system
Erase/Program cycle	—	100	—	—	cycle	

Note: The internal automatic algorithm continues operations for up to 48 ms, for each 1-byte writing operation.

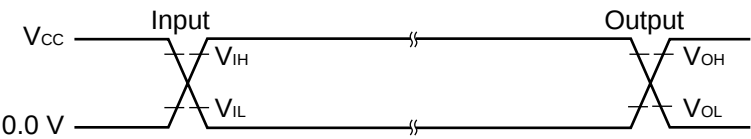
5. AC Characteristics

(1) Measurement Conditions

(V_{CC} = 3.15 V to 3.6 V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
"H" level input voltage	V _{IH}	—	1/2* × V _{CC}	—	V	
"L" level input voltage	V _{IL}	—	1/2* × V _{CC}	—	V	
"H" level output voltage	V _{OH}	—	1/2* × V _{CC}	—	V	
"L" level output voltage	V _{OL}	—	1/2* × V _{CC}	—	V	

*: Input rise/fall time is 10 ns. and less.

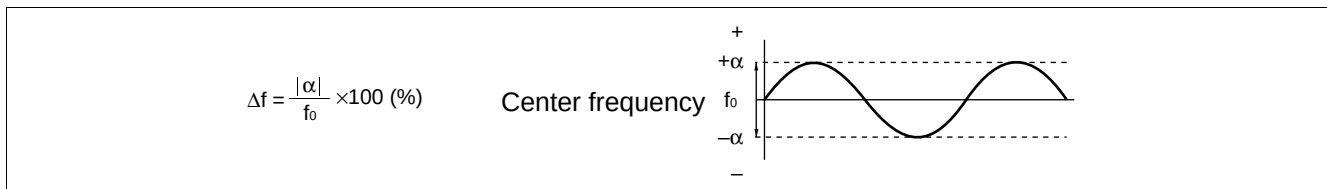


(2) Clock Timing Rating

(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

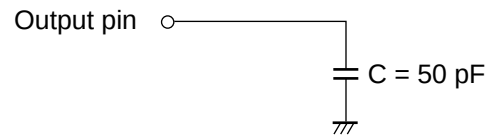
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Clock frequency	F _C	X0, X1	Self-oscillation at 12.5 MHz Internal operation at 25 MHz (Via PLL, double)	12.5	12.5	MHz	
	F _C	X0, X1	Self-oscillation (divide-by-2 input)	10	25	MHz	
	F _C	X0, X1	External clock (divide-by-2 input)	10	25	MHz	
Clock cycle time	t _c	X0, X1	Self-oscillation at 12.5 MHz Internal operation at 25 MHz (Via PLL, double)	—	80	ns	
	t _c	X0, X1	—	40	100	ns	
Frequency shift ratio (when locked)	Δf	—	Self-oscillation at 12.5 MHz Internal operation at 25 MHz (Via PLL, double)	—	5	%	*1
Input clock pulse width	P _{WH} , P _{WL}	X0, X1	12.5 MHz to 25.0 MHz	18.5	—	ns	Input clock pulse to X0 and X1
	P _{WH}	X0	12.5 MHz and less	25	—	ns	Input clock pulse to X0 only
Input clock rising/falling time	t _{CR} , t _{CF}	X0, X1	—	—	8	ns	(t _{CR} + t _{CF})
Internal operating clock frequency	f _{CP}	—	CPU system	0.625*2	25	MHz	
	f _{CPP}	—	Peripheral system	0.625*2	25	MHz	
Internal operating clock cycle time	t _{CP}	—	CPU system	40	1600*2	ns	
	t _{CPP}	—	Peripheral system	40	1600*2	ns	

*1 : Frequency shift ratio stands for deviation ratio of the operating clock from the center frequency in the clock multiplication system.

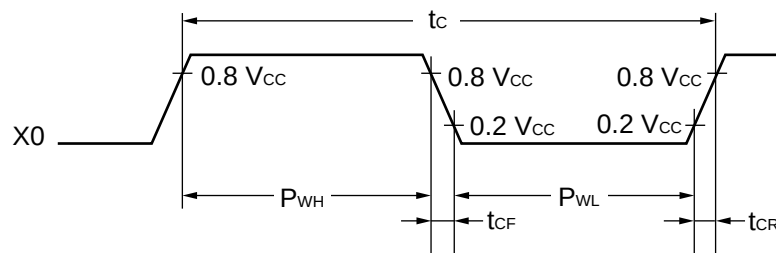


*2 : These values are for a minimum clock of 10 MHz input to X0, a divide-by-2 system of the source oscillation and a 1/8 gear.

- **Load conditions**



- **Clock timing rating measurement conditions**



(3) Clock Output Timing

($V_{CC} = 3.15 \text{ V to } 3.6 \text{ V}$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	t_{CP}^{*1}	—	ns	*2
CLK $\uparrow \rightarrow$ CLK $\downarrow$	t_{CHCL}	CLK	—	$1/2 \times t_{CYC} - 5$	$1/2 \times t_{CYC} + 5$	ns	*3
CLK $\downarrow \rightarrow$ CLK $\uparrow$	t_{CLCH}	CLK		$1/2 \times t_{CYC} - 5$	$1/2 \times t_{CYC} + 5$	ns	*4

*1 : For information on t_{CP} (internal operating clock cycle time), see “(2) Clock Timing Rating.”

*2 : t_{CYC} is a frequency for 1 clock cycle including a gear cycle.

*3 : Rating at a gear cycle of $\times 1$.

When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute “n” in the following equations with 1/2, 1/4, 1/8, respectively.

$$\text{Min} : (1 - n/2) \times t_{CYC} - 10$$

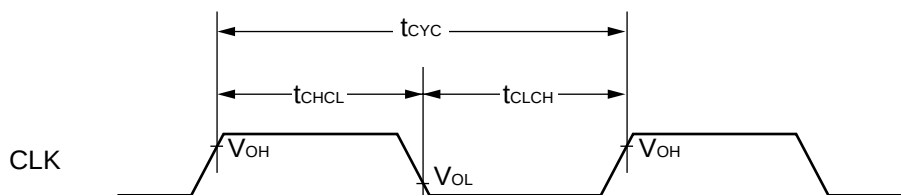
$$\text{Max} : (1 - n/2) \times t_{CYC} + 10$$

*4 : Rating at a gear cycle of $\times 1$.

When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute “n” in the following equations with 1/2, 1/4, 1/8, respectively.

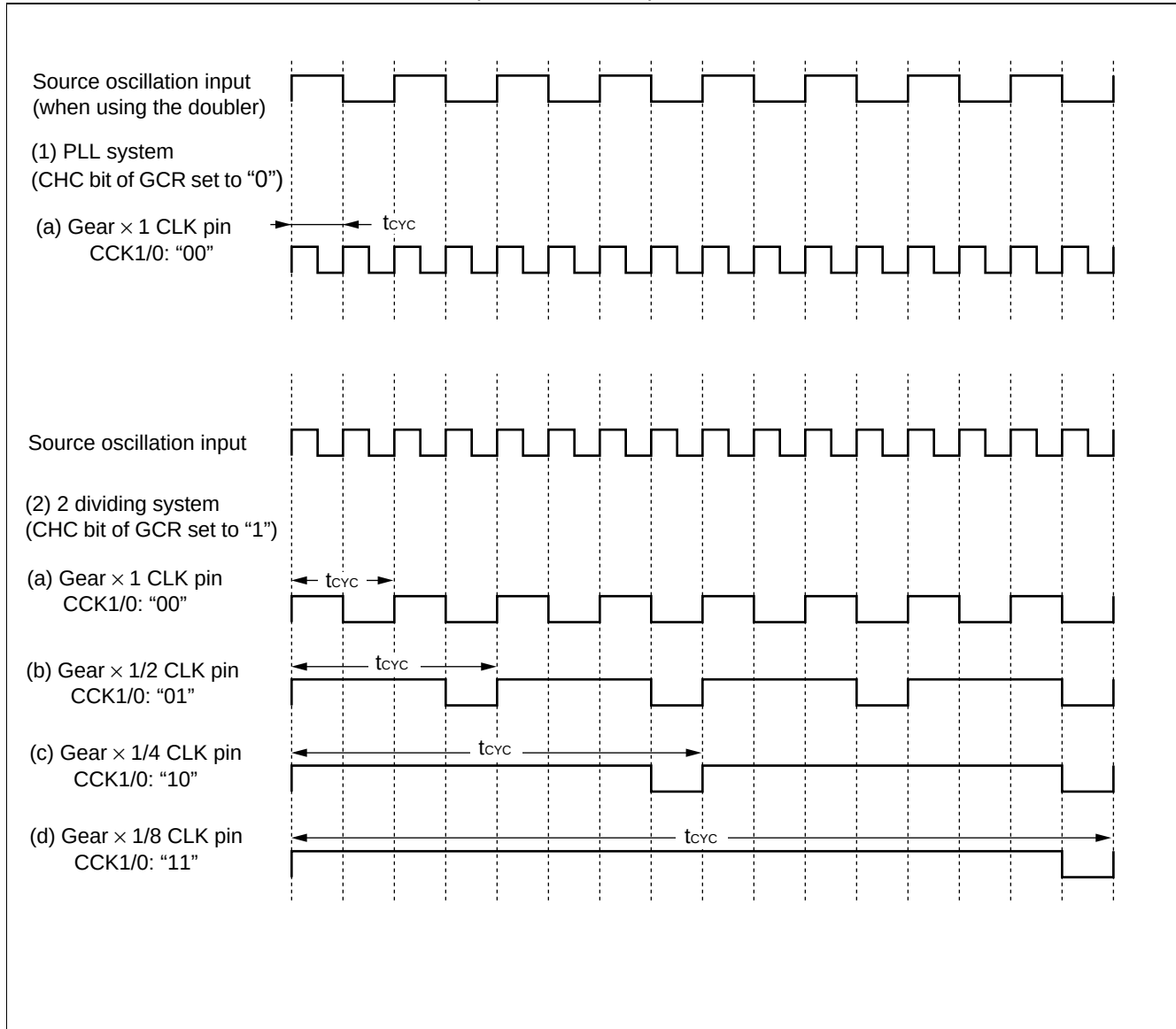
$$\text{Min} : n/2 \times t_{CYC} - 10$$

$$\text{Max} : n/2 \times t_{CYC} + 10$$



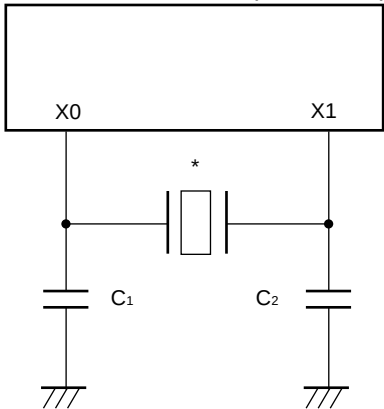
The relation between source oscillation input and CLK pin for configured by CHC/CCK1/CCK0 settings of GCR (gear control register) is as follows:

However, in this chart source oscillation input means X0 input clock.

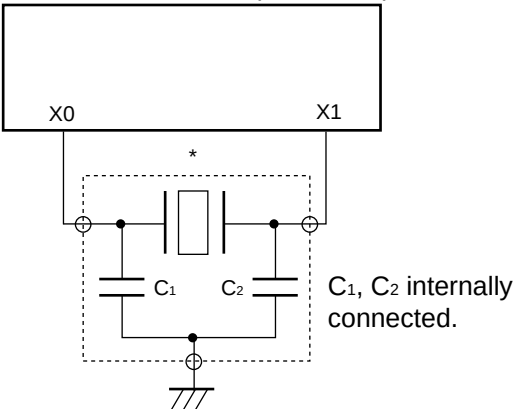


• Ceramic oscillator applications

Recommended circuit (2 contacts)



Recommended circuit (3 contacts)



*: Murata Mfg. Co., Ltd.

• Discreet type

Oscillation frequency [MHz]	Model	Load capacitance C ₁ = C ₂ [pF]	Power supply voltage V _{CC} [V]
5.00 to 6.30	CSA□□□MG	30	3.15 to 3.6
	CST□□□MGW	(30)	
	CSA□□□MG093	30	3.15 to 3.6
	CST□□□MGW093	(30)	
6.31 to 10.0	CSA□□□MTZ	30	3.15 to 3.6
	CST□□□MTW	(30)	
	CSA□□□MTZ093	30	3.15 to 3.6
	CST□□□MTW093	(30)	
10.1 to 13.0	CSA□□□MTZ	30	3.15 to 3.6
	CST□□□MTW	(30)	
	CSA□□□MTZ093	30	3.15 to 3.6
	CST□□□MTW093	(30)	
13.01 to 15.00	CSA□□□MXZ040	15	3.2 to 3.6
	CST□□□MXW0C3	(15)	

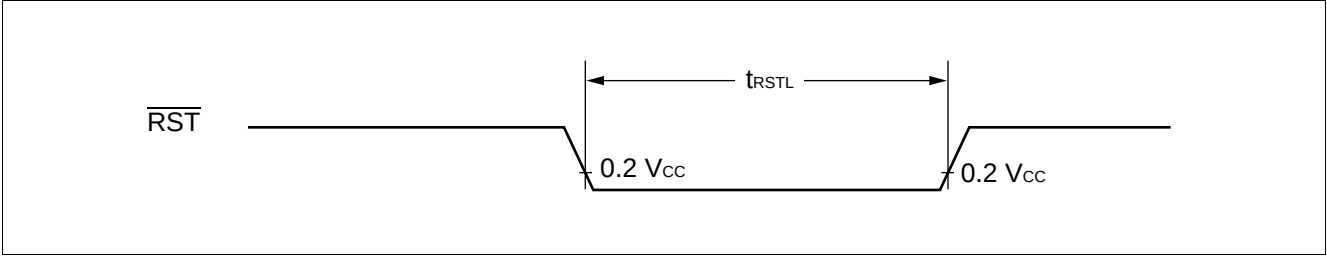
(): C₁ and C₂ internally connected 3 contacts type.

(4) Reset Input Ratings

(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Reset input time	t _{RSTL}	$\overline{\text{RST}}$	—	t _{CP} * × 5	—	ns	

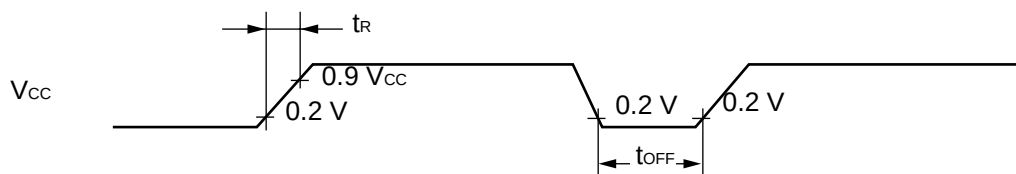
*: For information on t_{CP} (internal operating clock cycle time), see “(2) Clock Timing Rating.”



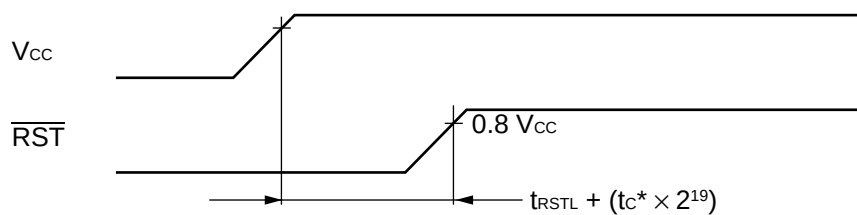
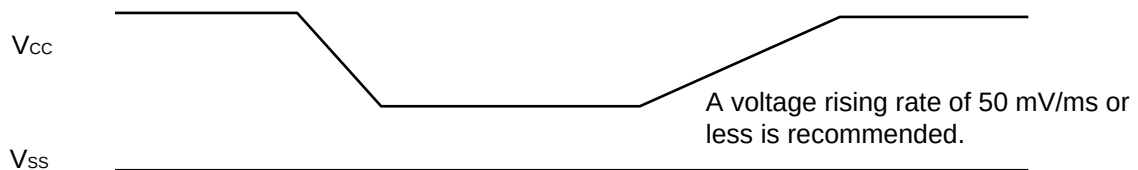
(5) Power on Supply Specifications (Power-on Reset)

($AV_{CC} = V_{CC} = 3.15 \text{ V to } 3.6 \text{ V}$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Power supply rising time	t_R	V_{CC}	$V_{CC} = 3.3 \text{ V}$	—	18	ms	$V_{CC} < 0.2 \text{ V}$ before the power supply rising
Power supply shut off time	t_{OFF}	V_{CC}	—	1	—	ms	Repeated operations



Note: Sudden change in supply voltage during operation may initiate a power-on sequence.
To change supply voltage during operation, it is recommended to smoothly raise the voltage to avoid rapid fluctuations in the supply voltage.



t_{RSTL} : Reset input time

*: For information on t_c (clock cycle time), see "(2) Clock Timing Rating."

- Notes :
- Set $\overline{RST}$ pin to "L" level when turning on the device, at least the described above duration after the supply voltage reaches V_{CC} is necessary before turning the $\overline{RST}$ to "H" level.
 - Some internal resistors which are initialized only via power on reset are embedded in the device. To initialize these resistors, run power on reset by returning on the power supply.

(6) Normal Bus Access Read/write Operation

($AV_{CC} = V_{CC} = 3.15 \text{ V to } 3.6 \text{ V}$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
$\overline{CS0}$ to $\overline{CS5}$ delay time	t_{CHCSL}	CLK, $\overline{CS0}$ to $\overline{CS5}$	—	—	15	ns	
	t_{CHCSH}	CLK, $\overline{CS0}$ to $\overline{CS5}$		—	15	ns	
Address delay time	t_{CHAV}	CLK, A24 to A00		—	15	ns	
Data delay time	t_{CHDV}	CLK, D31 to D16		—	15	ns	
$\overline{RD}$ delay time	t_{CLRL}	CLK, $\overline{RD}$		—	15	ns	
	t_{CLRH}	CLK, $\overline{RD}$		—	15	ns	
$\overline{WR0}$, $\overline{WR1}$ delay time	t_{CLWL}	CLK, $\overline{WR0}$, $\overline{WR1}$		—	15	ns	
	t_{CLWH}	CLK, $\overline{WR0}$, $\overline{WR1}$		—	15	ns	
Valid address → valid data input time	t_{AVDV}	A24 to A00, D31 to D16		—	$\frac{3}{2} \times t_{CYC}^{*1} - 25$	ns	*2 *3
$\overline{RD} \downarrow \rightarrow$ valid data input time	t_{RLDV}	$\overline{RD}$, D31 to D16		—	$t_{CYC}^{*1} - 10$	ns	*2
Data set up → $\overline{RD} \uparrow$ time	t_{DSRH}	$\overline{RD}$, D31 to D16		10	—	ns	
$\overline{RD} \uparrow \rightarrow$ data hold time	t_{RHDX}	$\overline{RD}$, D31 to D16		0	—	ns	

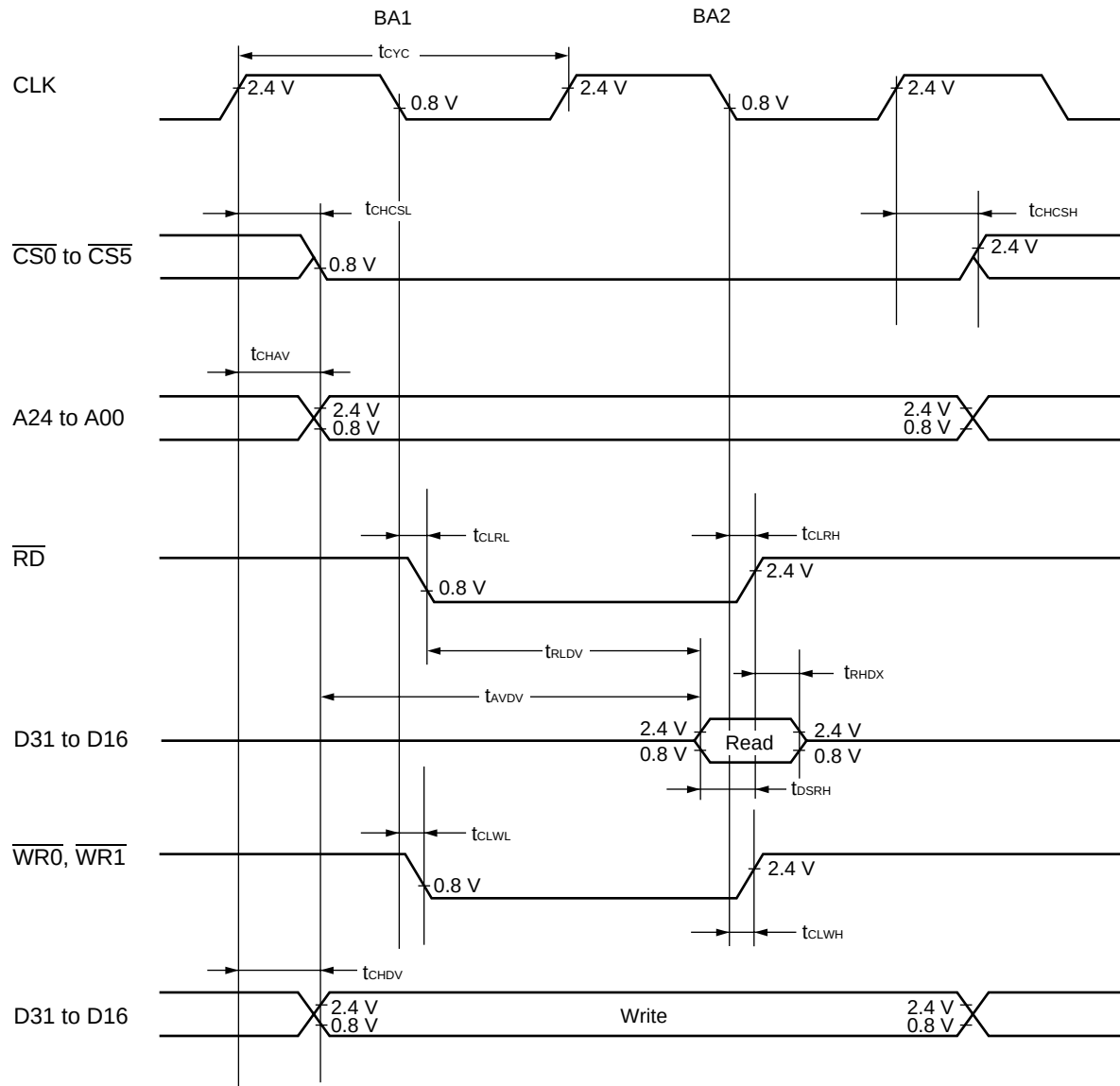
*1 : For information on t_{CYC} (a cycle time of peripheral system clock), see “(3) Clock Output Timing.”

*2 : When bus timing is delayed by automatic wait insertion or RDY input, add ($t_{CYC} \times$ extended cycle number for delay) to this rating.

*3 : Rating at a gear cycle of $\times 1$.

When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute “n” in the following equation with 1/2, 1/4, 1/8, respectively.

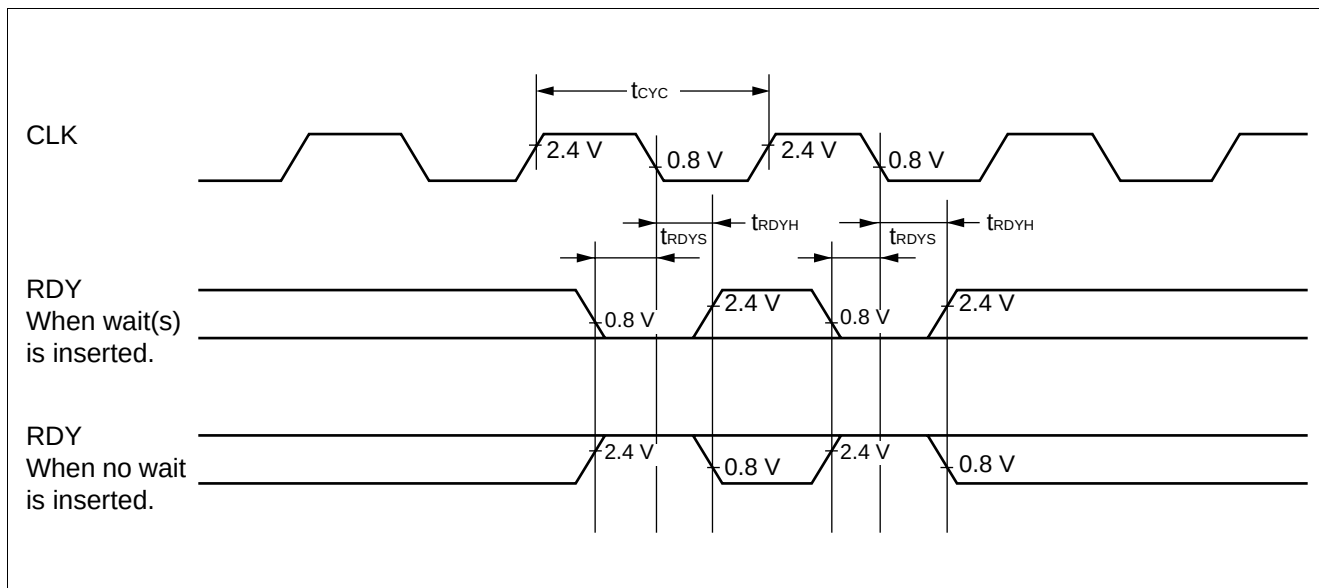
$$\text{Equation: } (2 - n/2) \times t_{CYC} - 25$$



(7) Ready Input Timing

($V_{CC} = 3.15 \text{ V to } 3.6 \text{ V}$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
RDY set up time $\rightarrow$ CLK $\downarrow$	t_{RDYS}	RDY, CLK	—	15	—	ns	
CLK $\downarrow \rightarrow$ RDY hold time	t_{RDYH}	CLK, RDY		0	—	ns	



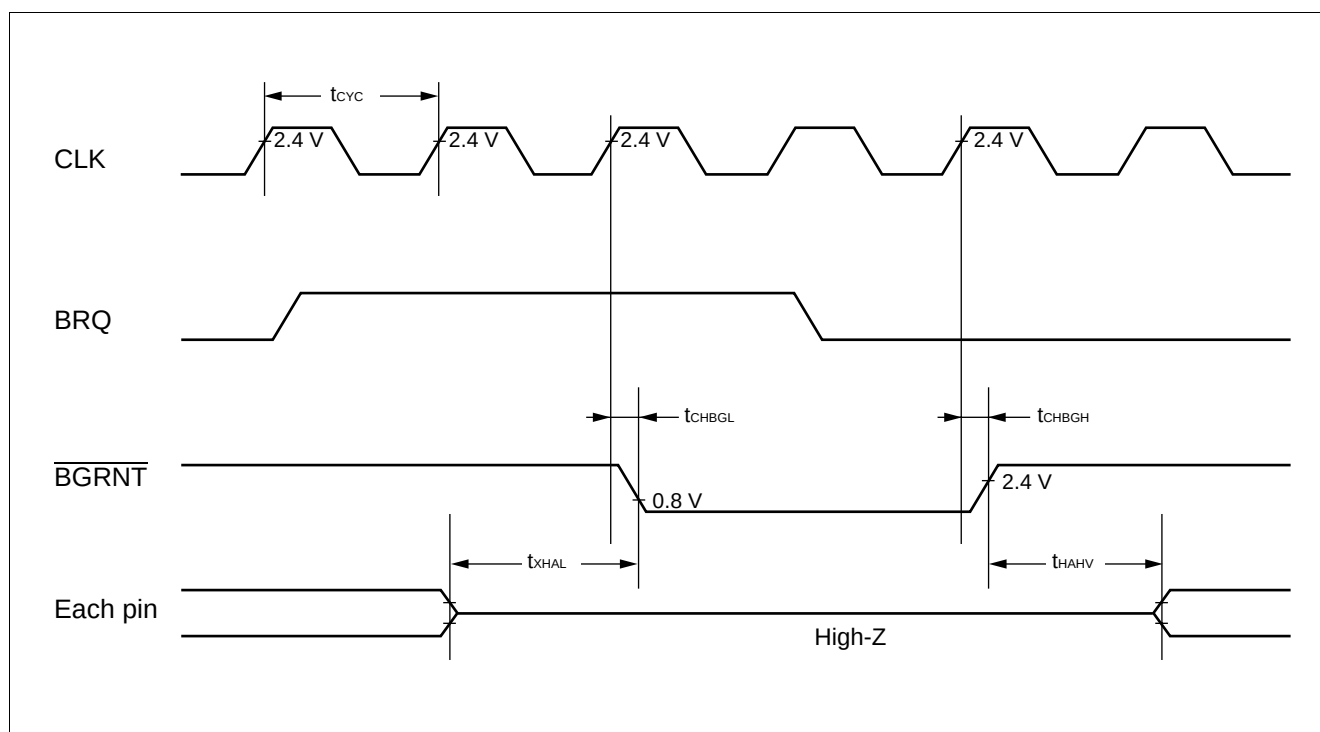
(8) Hold Timing

($V_{CC} = 3.15 \text{ V to } 3.6 \text{ V}$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
$\overline{\text{BGRNT}}$ delay time	t_{CHBGL}	$\frac{\text{CLK,}}{\overline{\text{BGRNT}}}$	—	—	6	ns	
	t_{CHBGH}	$\frac{\text{CLK,}}{\overline{\text{BGRNT}}}$		—	6	ns	
Pin floating $\rightarrow \overline{\text{BGRNT}} \downarrow$ time	t_{XHAL}	$\overline{\text{BGRNT}}$		$t_{\text{CYC}}^* - 10$	$t_{\text{CYC}}^* + 10$	ns	
$\overline{\text{BGRNT}} \uparrow \rightarrow$ pin valid time	t_{HAHV}	$\overline{\text{BGRNT}}$		$t_{\text{CYC}}^* - 10$	$t_{\text{CYC}}^* + 10$	ns	

*: For information on t_{CYC} (a cycle time of peripheral system clock), see “(3) Clock Output Timing.”

Note: There is a delay time of more than 1 cycle from BRQ input to $\overline{\text{BGRNT}}$ change.



(9) Normal DRAM Mode Read/Write Cycle

(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
RAS delay time	t _{CLRAH}	CLK, RAS	—	—	15	ns	
	t _{CHRAL}	CLK, RAS		—	15	ns	
CAS delay time	t _{CLCASL}	CLK, CS0H, CS1H, CS0L, CS1L		—	15	ns	
	t _{CLCASH}	CLK, CS0H, CS1H, CS0L, CS1L		—	15	ns	
ROW address delay time	t _{CHRAV}	CLK, A24 to A00		—	15	ns	
COLUMN address delay time	t _{CHCAV}	CLK, A24 to A00		—	15	ns	
$\overline{DW}$ delay time	t _{CHDWL}	CLK, $\overline{DW}^{*2}$		—	15	ns	
	t _{CHDWH}	CLK, $\overline{DW}^{*2}$		—	15	ns	
Output data delay time	t _{CHDV1}	CLK, D31 to D16		—	15	ns	
RAS ↓→ valid data input time	t _{RLDV}	RAS, D31 to D16		—	$\frac{5}{2} \times t_{CYC}^{*1} - 16$	ns	*3 *4
CAS ↓→ valid data input time	t _{CLDV}	CS0H, CS1H, CS0L, CS1L, D31 to D16		—	$t_{CYC}^{*1} - 17$	ns	*3
CAS ↑→ data hold time	t _{CADH}	CS0H, CS1H, CS0L, CS1L, D31 to D16		10	—	ns	

*1 : For information on t_{CYC} (a cycle time of peripheral system clock), see “(3) Clock Output Timing.”

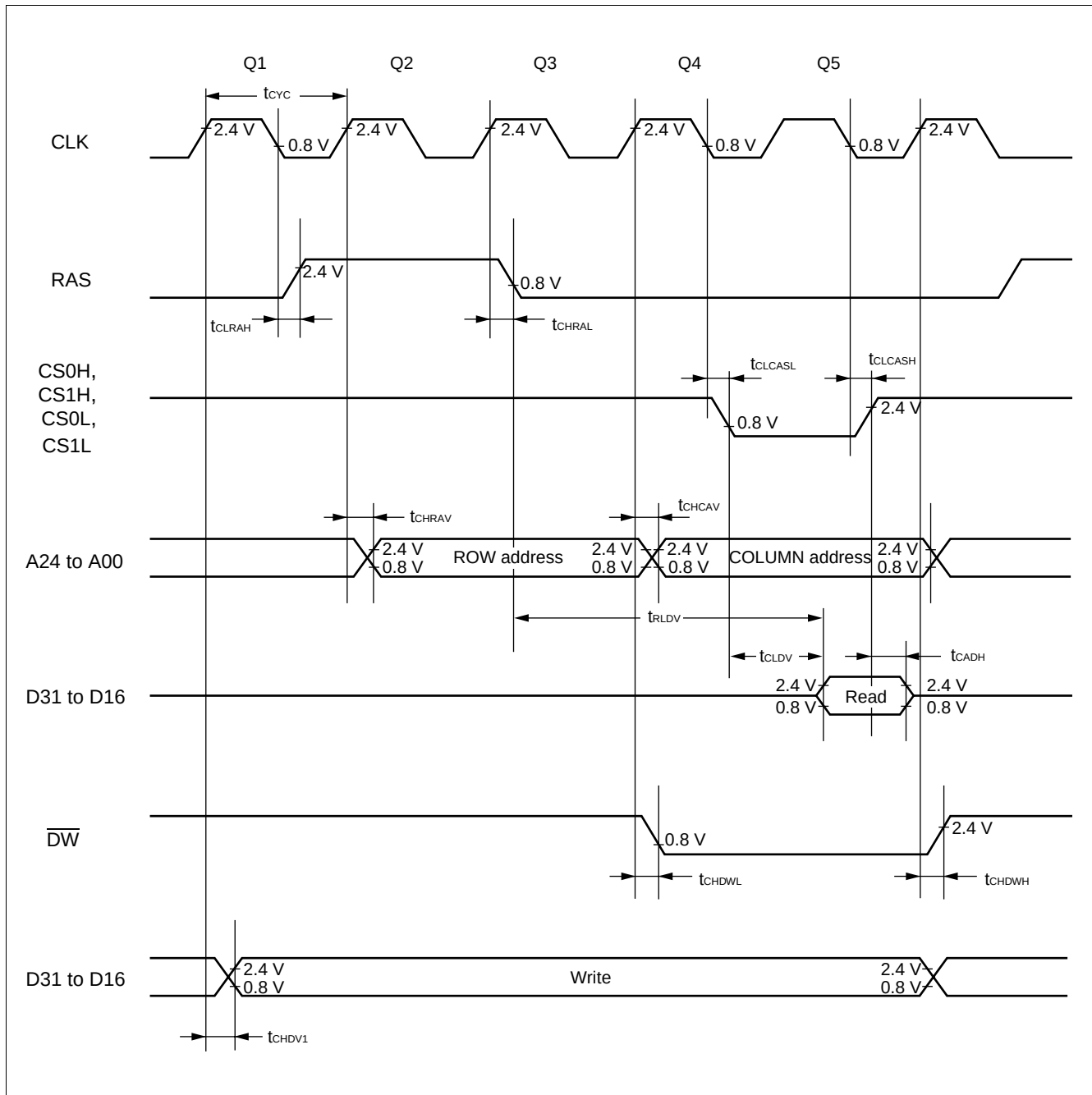
*2 : $\overline{DW}$ expresses that $\overline{DW0}$, $\overline{DW1}$ and CS0H, CS1H are used for $\overline{WE}$.

*3 : When Q1 cycle or Q4 cycle is extended for 1 cycle, add t_{CYC} time to this rating.

*4 : Rating at a gear cycle of × 1.

When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute “n” in the following equation with 1/2, 1/4, 1/8, respectively.

$$\text{Equation: } (3 - n/2) \times t_{CYC} - 16$$



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(10) Normal DRAM Mode Fast Page Read/Write Cycle

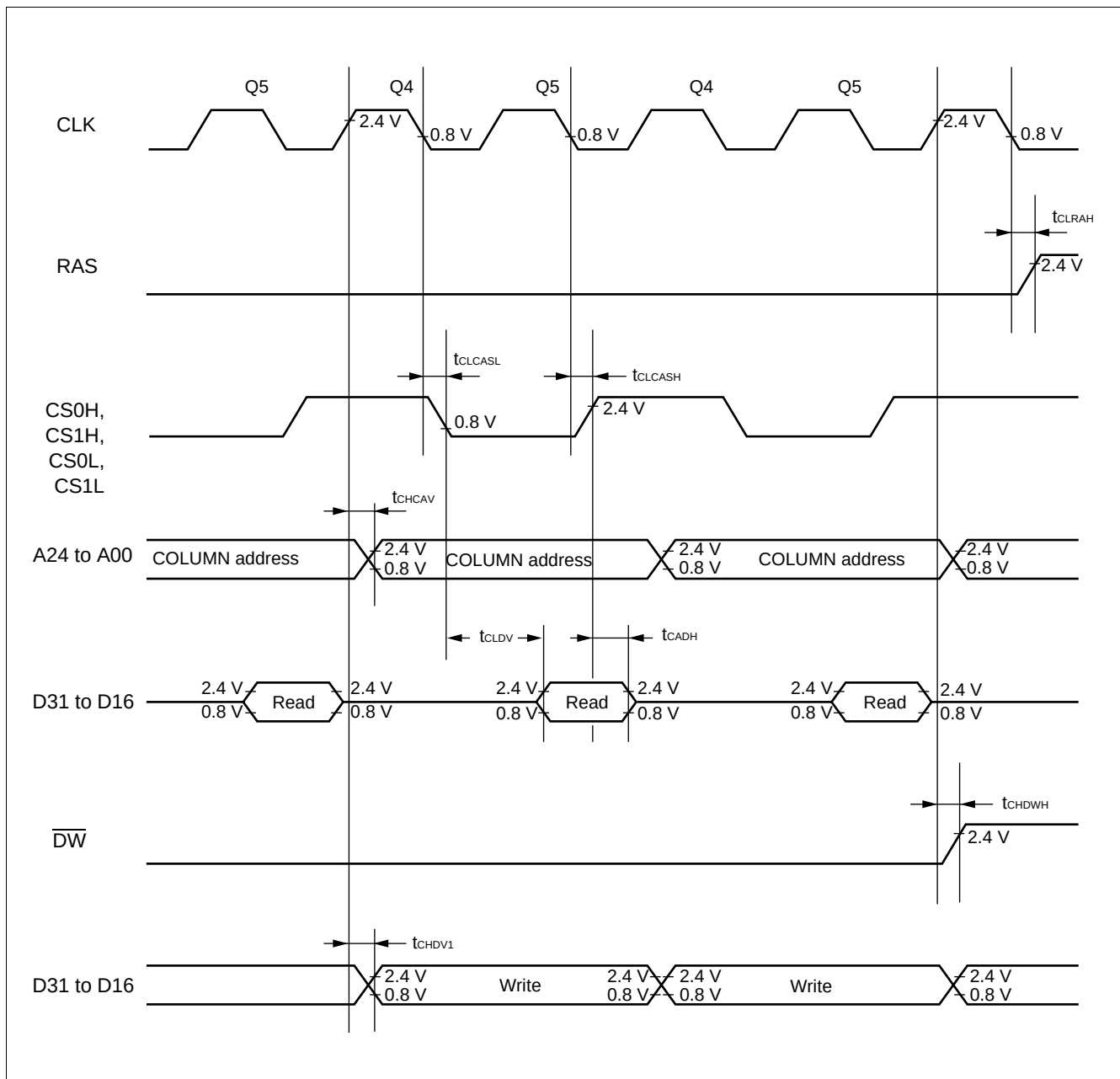
(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
RAS delay time	t _{CLRAH}	CLK, RAS	—	—	15	ns	
CAS delay time	t _{CLCASL}	CLK, CS0H, CS1H, CS0L, CS1L		—	15	ns	
	t _{CLCASH}	CLK, CS0H, CS1H, CS0L, CS1L		—	15	ns	
COLUMN address delay time	t _{CHCAV}	CLK, A24 to A00		—	15	ns	
$\overline{DW}$ delay time	t _{CHDWH}	CLK, $\overline{DW}$ *2		—	15	ns	
Output data delay time	t _{CHDV1}	CLK, D31 to D16		—	15	ns	
CAS ↓ → valid data input time	t _{CLDV}	CS0H, CS1H, CS0L, CS1L, D31 to D16		—	t _{CYC} *1 – 17	ns	*3
CAS ↑ → data hold time	t _{CADH}	CS0H, CS1H, CS0L, CS1L, D31 to D16		10	—	ns	

*1 : For information on t_{CYC} (a cycle time of peripheral system clock), see “(3) Clock Output Timing.”

*2 : $\overline{DW}$ expresses that $\overline{DW0}$, $\overline{DW1}$ and CS0H, CS1H are used for $\overline{WE}$.

*3 : When Q4 cycle is extended for 1 cycle, add t_{CYC} time to this rating.



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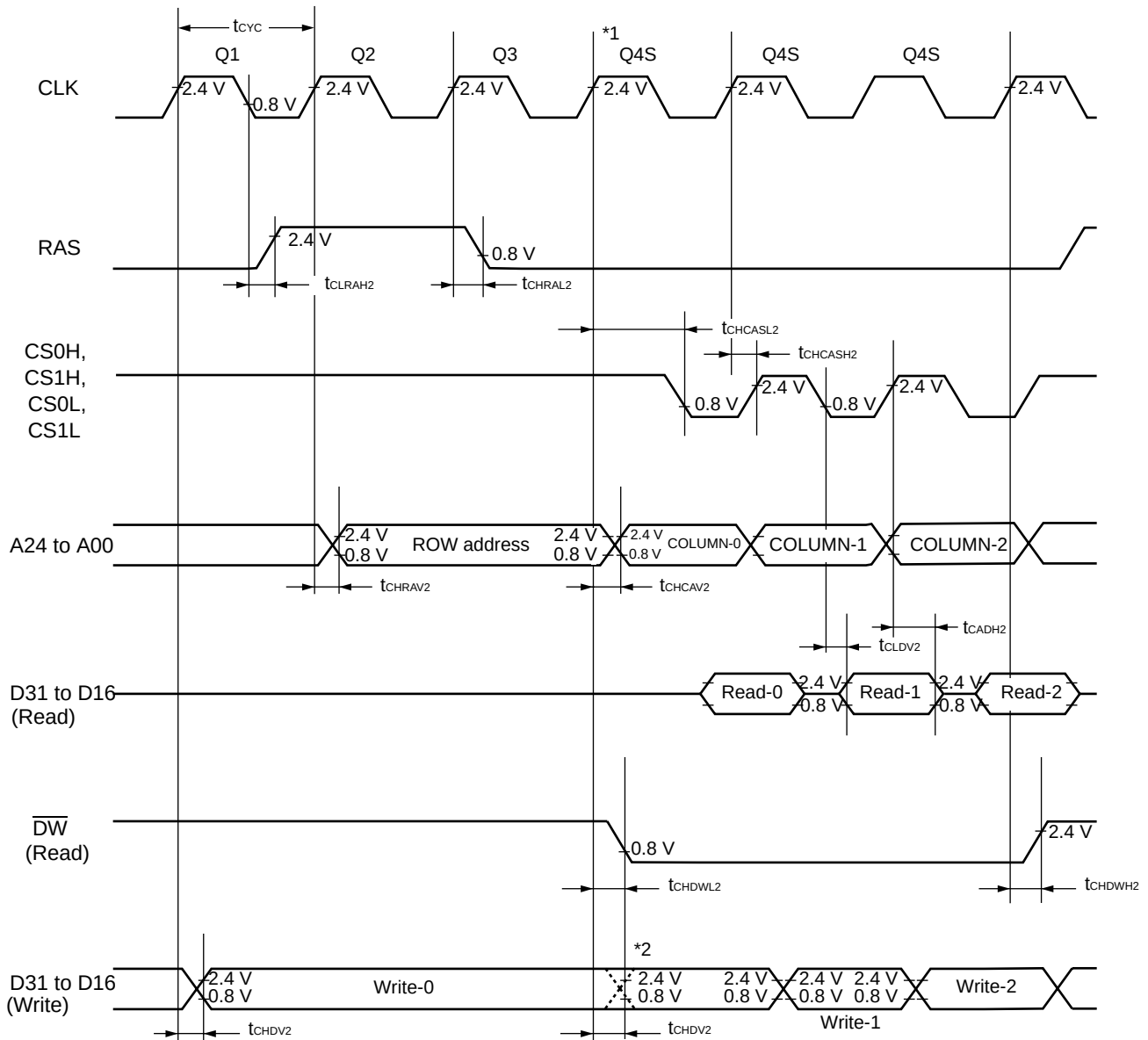
(11) Single DRAM Timing

($V_{CC} = 3.15 \text{ V to } 3.6 \text{ V}$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
RAS delay time	t_{CLRAH2}	CLK, RAS	—	—	15	ns	
	t_{CHRAL2}	CLK, RAS			15	ns	
CAS delay time	$t_{CHCASL2}$	CLK, CS0H, CS1H, CS0L, CS1L		—	$n/2 \times t_{CYC}^{*1}$	ns	
	$t_{CHCASH2}$	CLK, CS0H, CS1H, CS0L, CS1L		—	15	ns	
ROW address delay time	t_{CHRAV2}	CLK, A24 to A00		—	15	ns	
COLUMN address delay time	t_{CHCAV2}	CLK, A24 to A00		—	15	ns	
$\overline{DW}$ delay time	t_{CHDWL2}	CLK, $\overline{DW}^{*2}$		—	15	ns	
	t_{CHDWH2}	CLK, $\overline{DW}^{*2}$		—	15	ns	
Output data delay time	t_{CHDV2}	CLK, D31 to D16		—	15	ns	
CAS $\downarrow \rightarrow$ Valid data input time	t_{CLDV2}	CS0H, CS1H, CS0L, CS1L, D31 to D16		—	$(1 - n/2) \times t_{CYC}^{*1} - 17$	ns	
CAS $\uparrow \rightarrow$ data hold time	t_{CADH2}	CS0H, CS1H, CS0L, CS1L, D31 to D16		10	—	ns	

*1 : For information on t_{CYC} (a cycle time of peripheral system clock), see “(3) Clock Output Timing.”

*2 : $\overline{DW}$ expresses that $\overline{DW0}$, $\overline{DW1}$ and CS0H, CS1H are used for $\overline{WE}$.



*1 : Q4S indicates Q4SR (Read) of Single DRAM cycle or Q4SW (Write) cycle.

*2 : ----- indicates the timing when the bus cycle begins from the high speed page mode.

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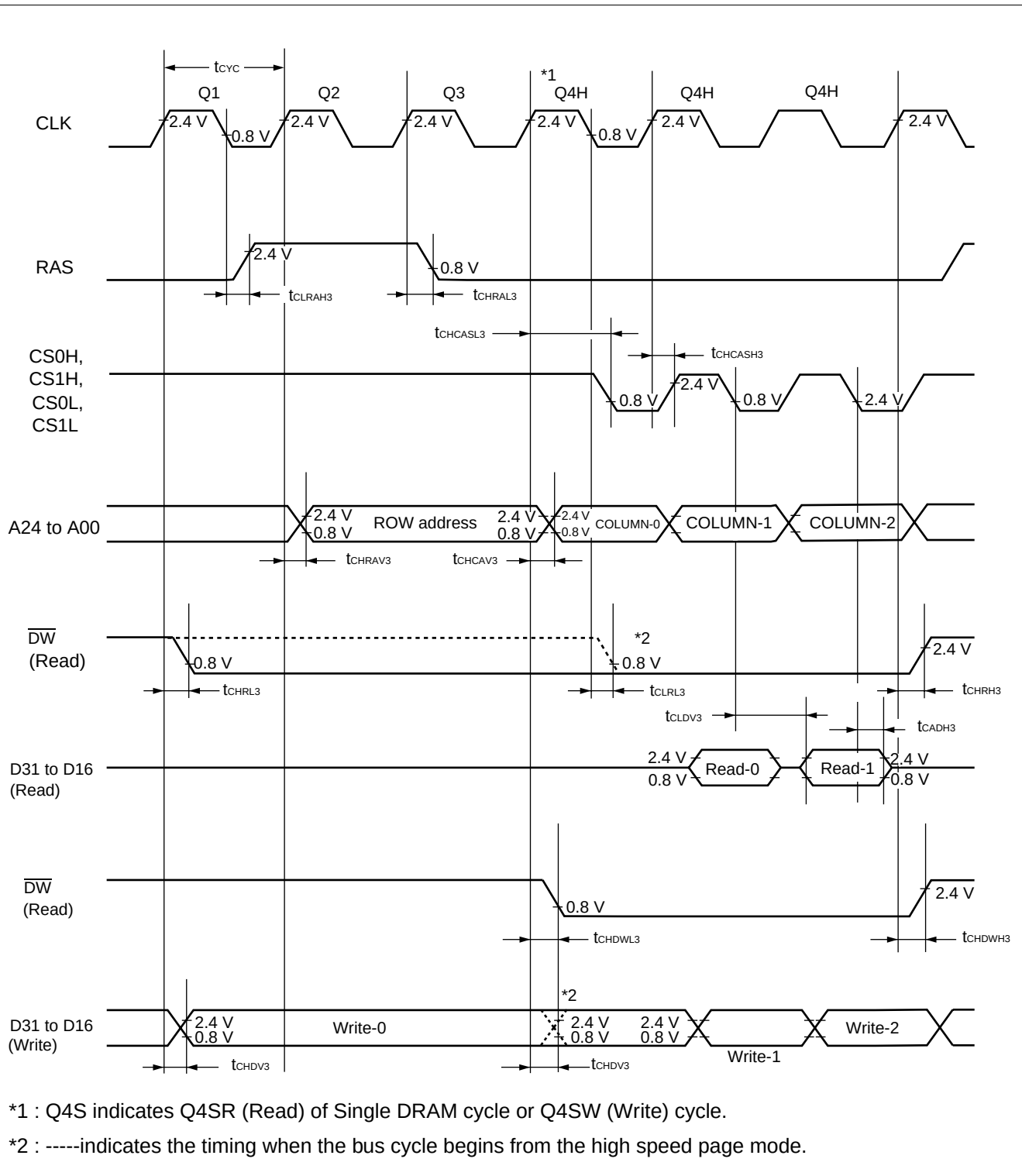
(12) Hyper DRAM Timing

($V_{CC} = 3.15 \text{ V to } 3.6 \text{ V}$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
RAS delay time	t_{CLRAH3}	CLK, RAS	—	—	15	ns	
	t_{CHRAL3}	CLK, RAS		—	15	ns	
CAS delay time	$t_{CHCASL3}$	CLK, CS0H, CS1H, CS0L, CS1L		—	$n/2 \times t_{CYC}^{*1}$	ns	
	$t_{CHCASH3}$	CLK, CS0H, CS1H, CS0L, CS1L		—	15	ns	
ROW address delay time	t_{CHRAV3}	CLK, A24 to A00		—	15	ns	
COLUMN address delay time	t_{CHCAV3}	CLK, A24 to A00		—	15	ns	
$\overline{\text{RD}}$ delay time	t_{CHRL3}	CLK, $\overline{\text{RD}}$		—	15	ns	
	t_{CHRH3}	CLK, $\overline{\text{RD}}$		—	15	ns	
	t_{CLRL3}	CLK, $\overline{\text{RD}}$		—	15	ns	
$\overline{\text{DW}}$ delay time	t_{CHDWL3}	CLK, $\overline{\text{DW}}^{*2}$		—	15	ns	
	t_{CHDWH3}	CLK, $\overline{\text{DW}}^{*2}$		—	15	ns	
Output data delay time	t_{CHDV3}	CLK, D31 to D16		—	15	ns	
CAS $\downarrow \rightarrow$ valid data input time	t_{CLDV3}	CS0H, CS1H, CS0L, CS1L, D31 to D16		—	$t_{CYC} - 17$	ns	
CAS $\downarrow \rightarrow$ data hold time	t_{CADH3}	CS0H, CS1H, CS0L, CS1L, D31 to D16		10	—	ns	

*1 : For information on t_{CYC} (a cycle time of peripheral system clock), see “(3) Clock Output Timing.”

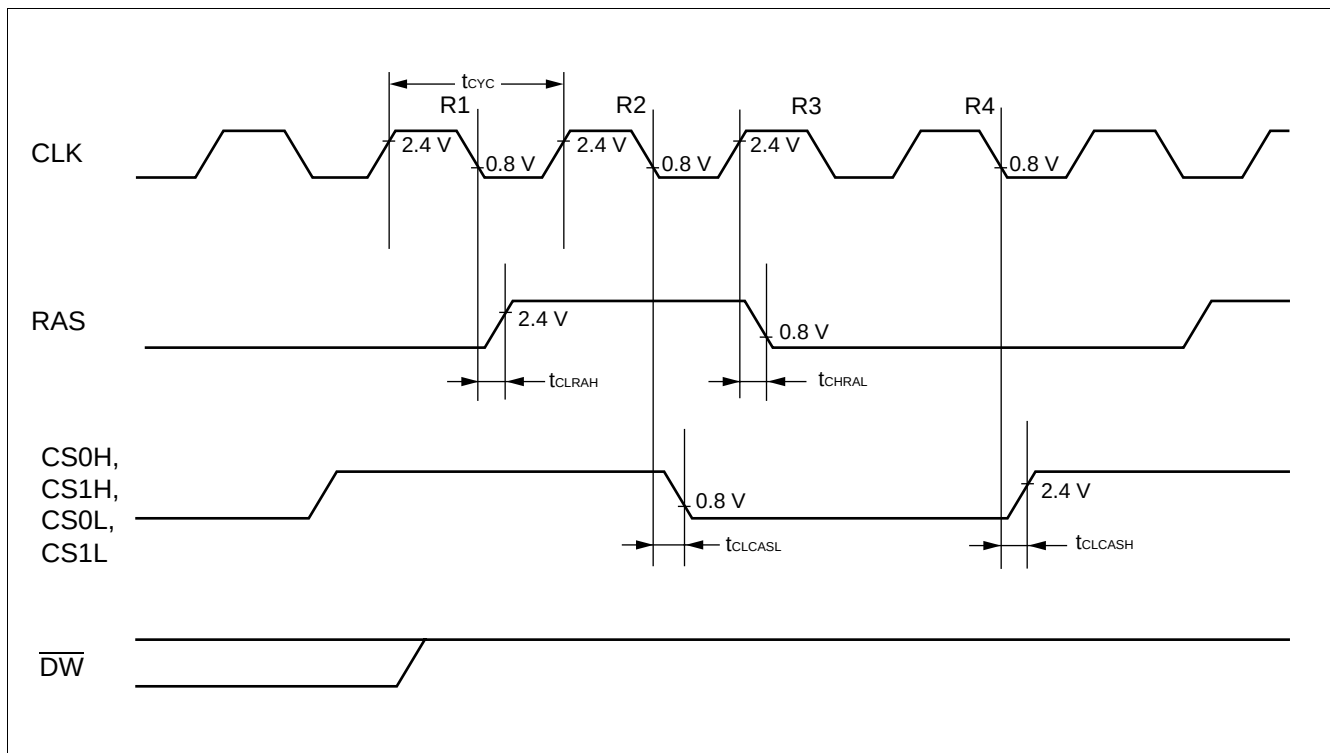
*2 : $\overline{\text{DW}}$ expresses that $\overline{\text{DW0}}$, $\overline{\text{DW1}}$ and CS0H, CS1H are used for $\overline{\text{WE}}$.



(13) CBR Refresh

($V_{CC} = 3.15 \text{ V}$ to 3.6 V , $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)

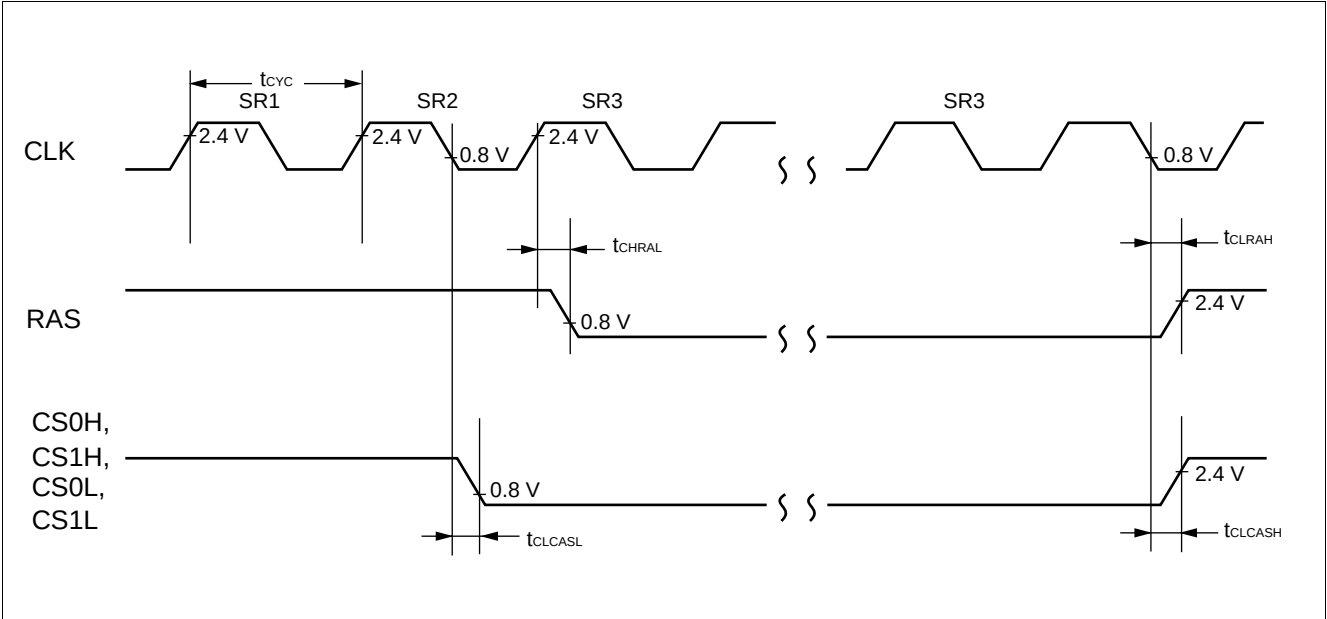
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
RAS delay time	t_{CLRAH}	CLK, RAS	—	—	15	ns	
	t_{CHRAL}	CLK, RAS		—	15	ns	
CAS delay time	t_{CLCASL}	CLK, CS0H, CS1H, CS0L, CS1L		—	15	ns	
	t_{CLCASH}	CLK, CS0H, CS1H, CS0L, CS1L		—	15	ns	



(14) Self Refresh

(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
RAS delay time	t _{CLRAH}	CLK, RAS	—	—	15	ns	
	t _{CHRAL}	CLK, RAS		—	15	ns	
CAS delay time	t _{CLCASL}	CLK, CS0H, CS1H, CS0L, CS1L		—	15	ns	
	t _{CLCASH}	CLK, CS0H, CS1H, CS0L, CS1L		—	15	ns	



(15) UART Timing

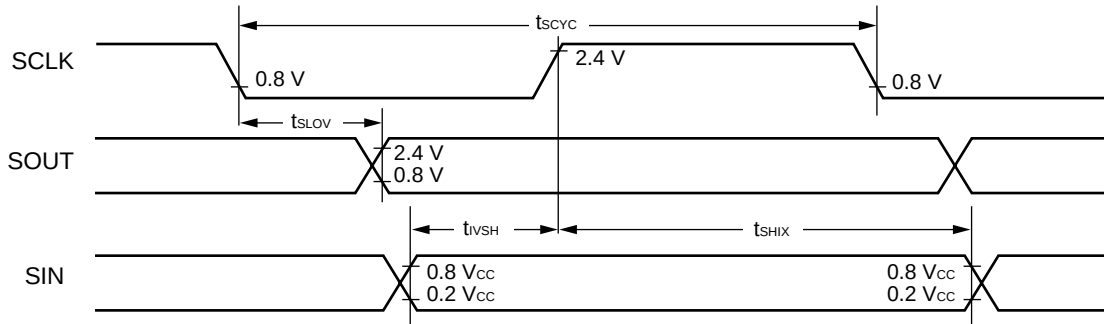
($V_{CC} = 3.15V$ to $3.6V$, $V_{SS} = AV_{SS} = 0.0V$, $T_A = 0^{\circ}C$ to $+70^{\circ}C$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	—	Internal shift clock mode	$8 \times t_{CYCP}^*$	—	ns	
SCLK $\downarrow \rightarrow$ SOUT delay time	t_{SLOV}	—		-80	80	ns	
Valid SIN $\rightarrow$ SCLK $\uparrow$	t_{IVSH}	—		100	—	ns	
SCLK $\uparrow \rightarrow$ valid SIN hold time	t_{SHIX}	—		60	—	ns	
Serial clock "H" pulse width	t_{SHSL}	—	External shift clock mode	$4 \times t_{CYCP}^*$	—	ns	
Serial clock "L" pulse width	t_{SLSH}	—		$4 \times t_{CYCP}^*$	—	ns	
SCLK $\downarrow \rightarrow$ SOUT delay time	t_{SLOV}	—		—	150	ns	
Valid SIN $\rightarrow$ SCLK $\uparrow$	t_{IVSH}	—		60	—	ns	
SCLK $\uparrow \rightarrow$ valid SIN hold time	t_{SHIX}	—		60	—	ns	

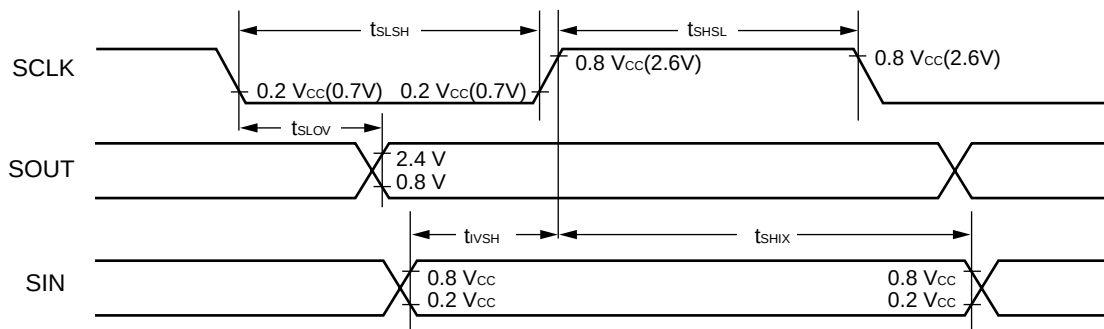
*: For information on t_{CYCP} (a cycle time of peripheral system clock), see "(2) Clock Timing Rating."

Notes: This rating is for AC characteristics in CLK synchronous mode.

• Internal shift clock mode



• External shift clock mode

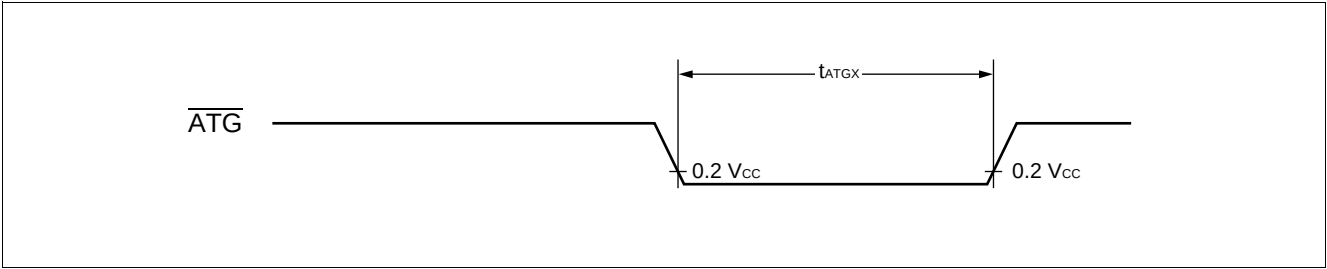


(16) Trigger System Input Timing

(V_{CC} = 3.15 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = 0°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
A/D start trigger input time	t _{ATGX}	$\overline{\text{ATG}}$	—	5 × t _{CYCP} *	—	ns	

*: For information on t_{CYCP} (a cycle time of peripheral system clock), see “(2) Clock Timing Rating.”

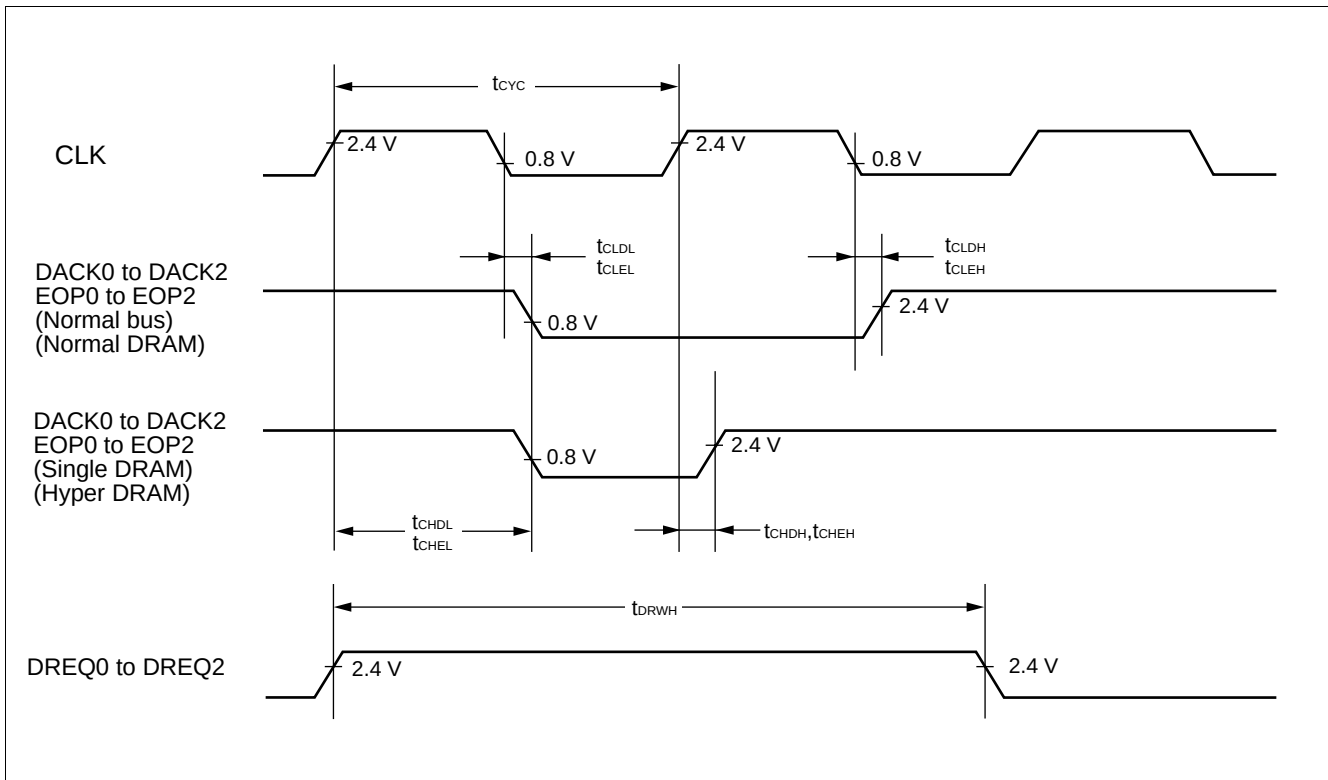


(17) DMA Controller Timing

($V_{CC} = 3.15 \text{ V to } 3.6 \text{ V}$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
DREQ input pulse width	t_{DRWH}	DREQ0 to DREQ2	—	$2 \times t_{CYC}^*$	—	ns	
DACK delay time (Normal bus) (Normal DRAM)	t_{CLDL}	CLK, DACK0 to DACK2		—	6	ns	
	t_{CLDH}	CLK, DACK0 to DACK2		—	6	ns	
EOP delay time (Normal bus) (Normal DRAM)	t_{CLEL}	CLK, EOP0 to EOP2		—	6	ns	
	t_{CLEH}	CLK, EOP0 to EOP2		—	6	ns	
DACK delay time (Single DRAM) (Hyper DRAM)	t_{CHDL}	CLK, DACK0 to DACK2		—	$n/2 \times t_{CYC}^*$	ns	
	t_{CHDH}	CLK, DACK0 to DACK2		—	6	ns	
EOP delay time (Single DRAM) (Hyper DRAM)	t_{CHEL}	CLK, EOP0 to EOP2		—	$n/2 \times t_{CYC}^*$	ns	
	t_{CHEH}	CLK, EOP0 to EOP2		—	6	ns	

*: For information on t_{CYC} (a cycle time of peripheral system clock), see “(3) Clock Output Timing.”



6. A/D Converter Block Electrical Characteristics

($V_{CC} = AV_{CC} = 3.15 \text{ V to } 3.6 \text{ V}$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $AVRH = 3.15 \text{ V to } 3.6 \text{ V}$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$)

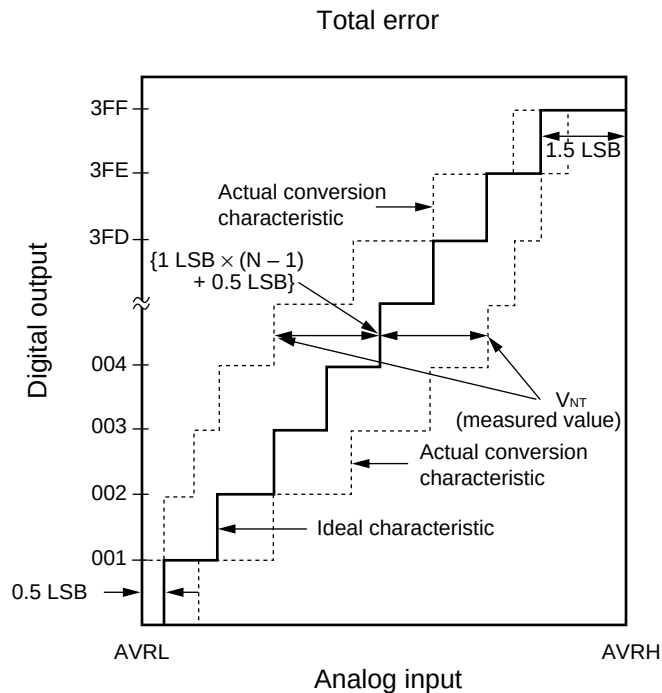
Parameter	Symbol	Pin name	Value			Unit
			Min	Typ	Max	
Resolution	—	—	—	10	10	bit
Total error	—	—	—	—	± 3.0	LSB
Linearity error	—	—	—	—	± 2.5	LSB
Differentiation linearity error	—	—	—	—	± 1.9	LSB
Zero transition voltage	V_{OT}	AN0 to AN3	-1.5LSB	$+0.5\text{LSB}$	$+2.5\text{LSB}$	mV
Full-scale transition voltage	V_{FST}	AN0 to AN3	$AVRH - 4.5\text{LSB}$	$AVRH - 1.5\text{LSB}$	$AVRH + 0.5\text{LSB}$	mV
Conversion time	—	—	5.19^{*1}	—	—	μs
Analog port input current	I_{AIN}	AN0 to AN3	—	0.1	10	μA
Analog input voltage	V_{AIN}	AN0 to AN3	AV_{SS}	—	$AVRH$	V
Reference voltage	—	$AVRH$	AV_{SS}	—	AV_{CC}	V
Power supply current	I_A	AV_{CC}	—	4	—	mA
	I_{AH}	AV_{CC}	—	—	5^{*2}	μA
Reference voltage supply current	I_R	$AVRH$	—	110	—	μA
	I_{RH}	$AVRH$	—	—	5^{*2}	μA
Conversion variance between channels	—	AN0 to AN3	—	—	4	LSB

*1 : $V_{CC} = AV_{CC} = 3.15 \text{ V to } 3.6 \text{ V}$, machine clock 25 MHz

*2 : Current value for A/D converters not in operation, CPU stop mode ($V_{CC} = AV_{CC} = AVRH = 3.6 \text{ V}$)

7. A/D Converter Glossary

- Resolution
The smallest change in analog voltage detected by A/D converter.
- Linearity error
A deviation of actual conversion characteristic from a line connecting the zero-traction point (between “00 0000 0000” ↔ “00 0000 0001”) to the full-scale transition point (between “11 1111 1110” ↔ “11 1111 1111”).
- Differential linearity error
A deviation of a step voltage for changing the LSB of output code from ideal input voltage.
- Total error
A difference between actual value and theoretical value. The overall error includes zero-transition error, full-scale transition error and linearity error.



$$\text{Total error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} [\text{LSB}]$$

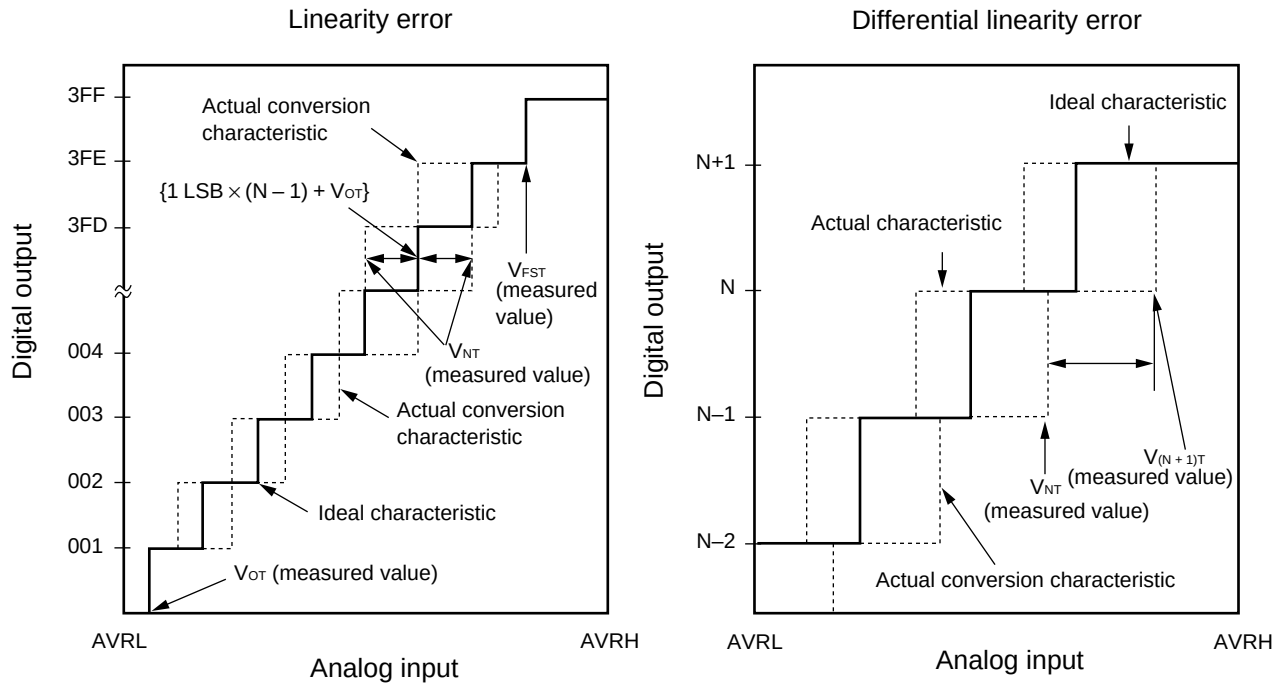
$$V_{OT} \text{ (ideal value)} = AVRL + 0.5 \text{ LSB [V]}$$

$$V_{FST} \text{ (ideal value)} = AVRH - 1.5 \text{ LSB [V]}$$

V_{NT} : A voltage for causing transition of digital output from $(N - 1)$ to N

(Continued)

(Continued)



$$\text{Linearity error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + V_{OT}\}}{1 \text{ LSB}} [\text{LSB}]$$

$$\text{Differential linearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1 [\text{LSB}]$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} [\text{V}]$$

$$1 \text{ LSB (ideal value)} = \frac{AVRH - AVRL}{1022} [\text{V}]$$

V_{OT} : A voltage for causing transition of digital output from $(000)_H$ to $(001)_H$

V_{FST} : A voltage for causing transition of digital output from $(3FE)_H$ to $(3FF)_H$

V_{NT} : A voltage for causing transition of digital output from $(N - 1)_H$ to N

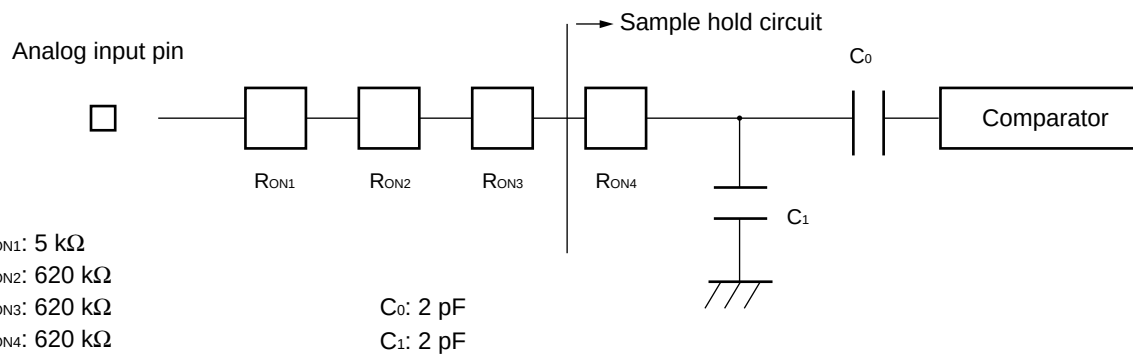
8. Notes on Using A/D Converter

Output impedance of external circuit of analog input under following conditions;

Output impedance of external circuit < 7 k Ω .

If output impedance of external circuit is too high, analog voltage sampling time may be too short for accurate sampling (sampling time is 5.6 μ s for a machine clock of 25 MHz).

• Analog input Equivalent Circuit

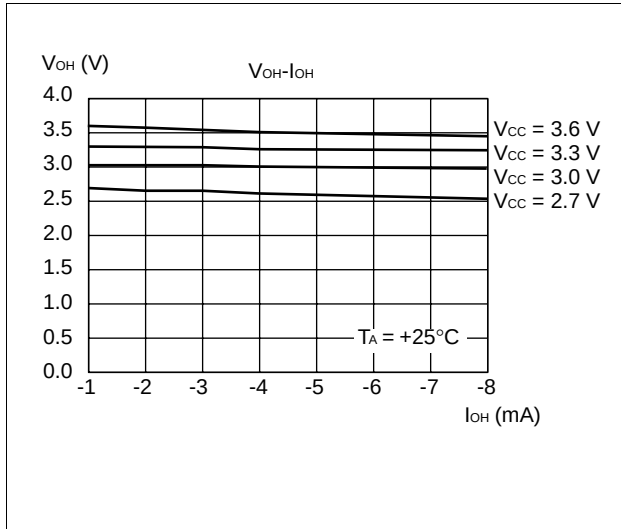


• Error

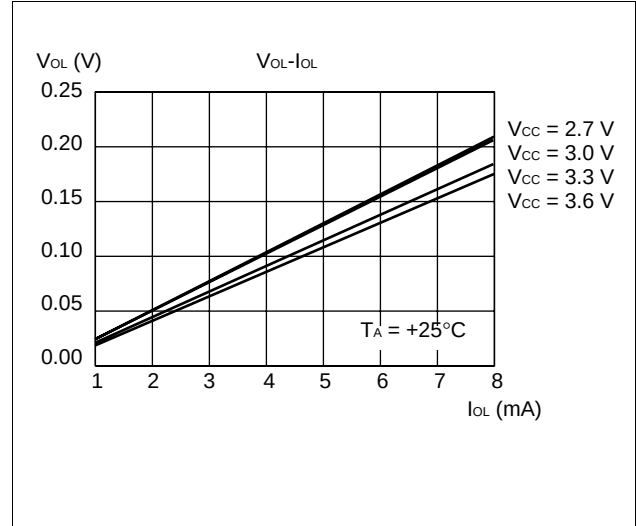
As the absolute value of $|AVRH - AVR_L|$ decreases, relative error increases.

EXAMPLE CHARACTERISTICS

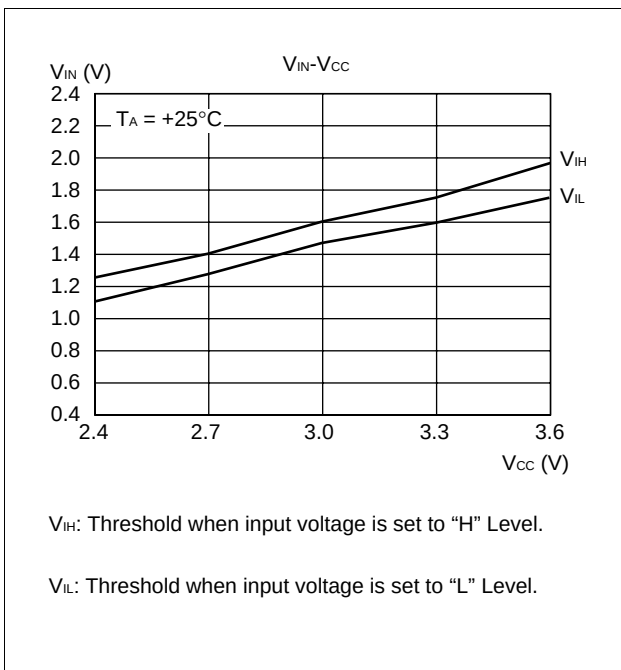
(1) "H" Level Output Voltage



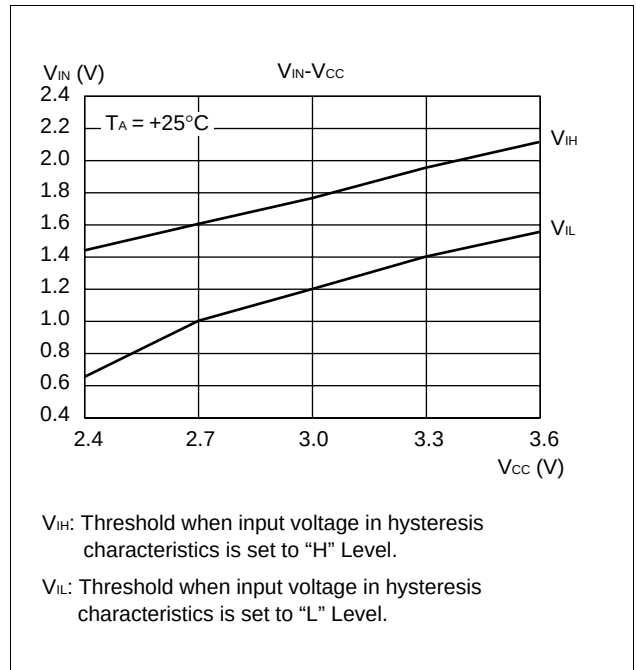
(2) "L" Level Output Voltage



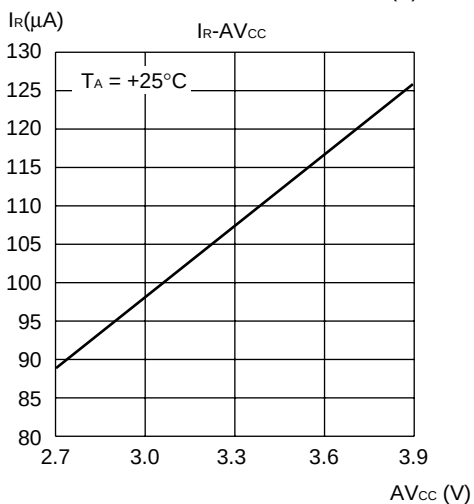
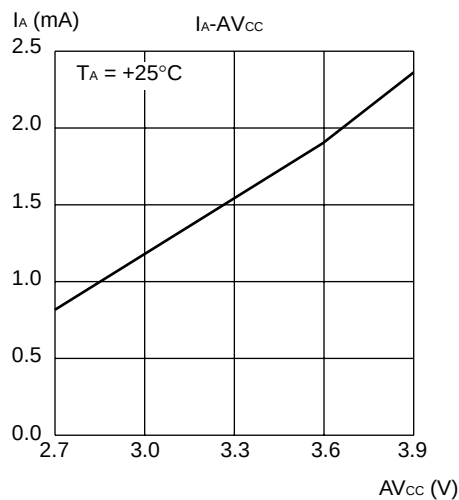
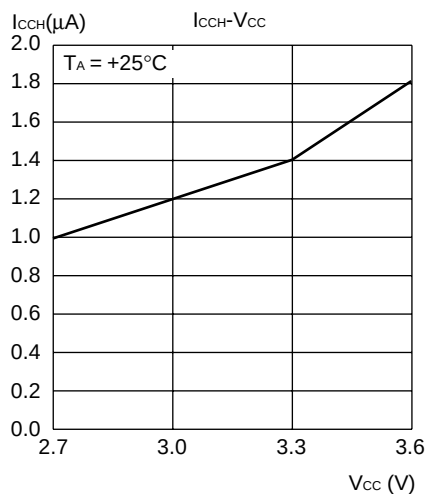
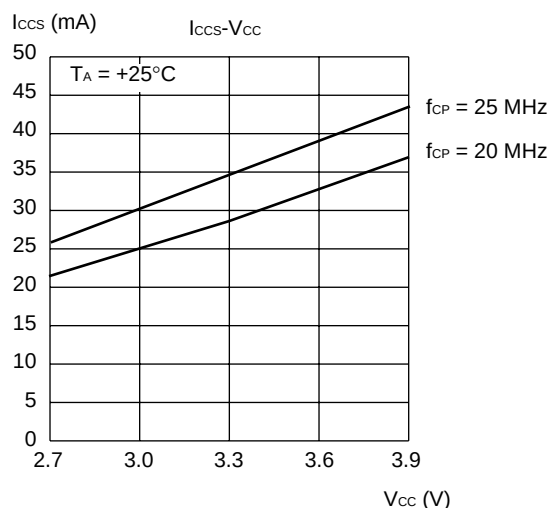
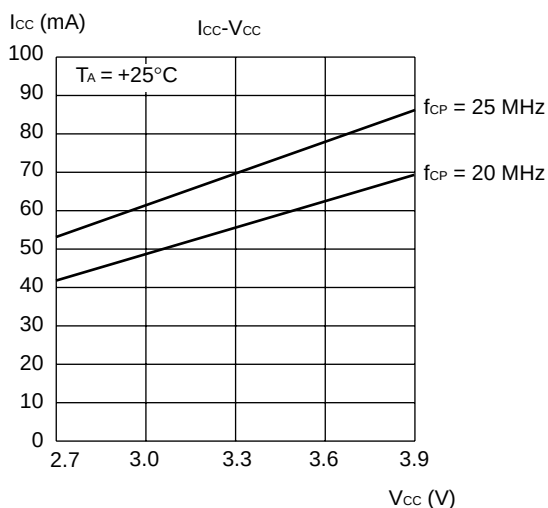
(3) "H" Level Input Voltage/"L" Level Input Voltage (CMOS Input)



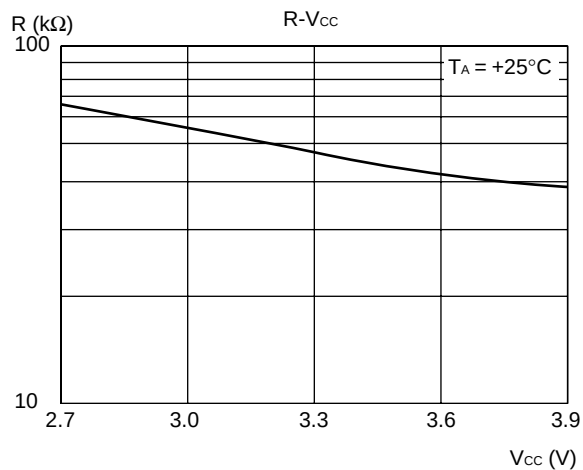
(4) "H" Level Input Voltage/"L" Level Input Voltage (Hysteresis Input)



(5) Power Supply Current (f_{CP} = Internal clock frequency)



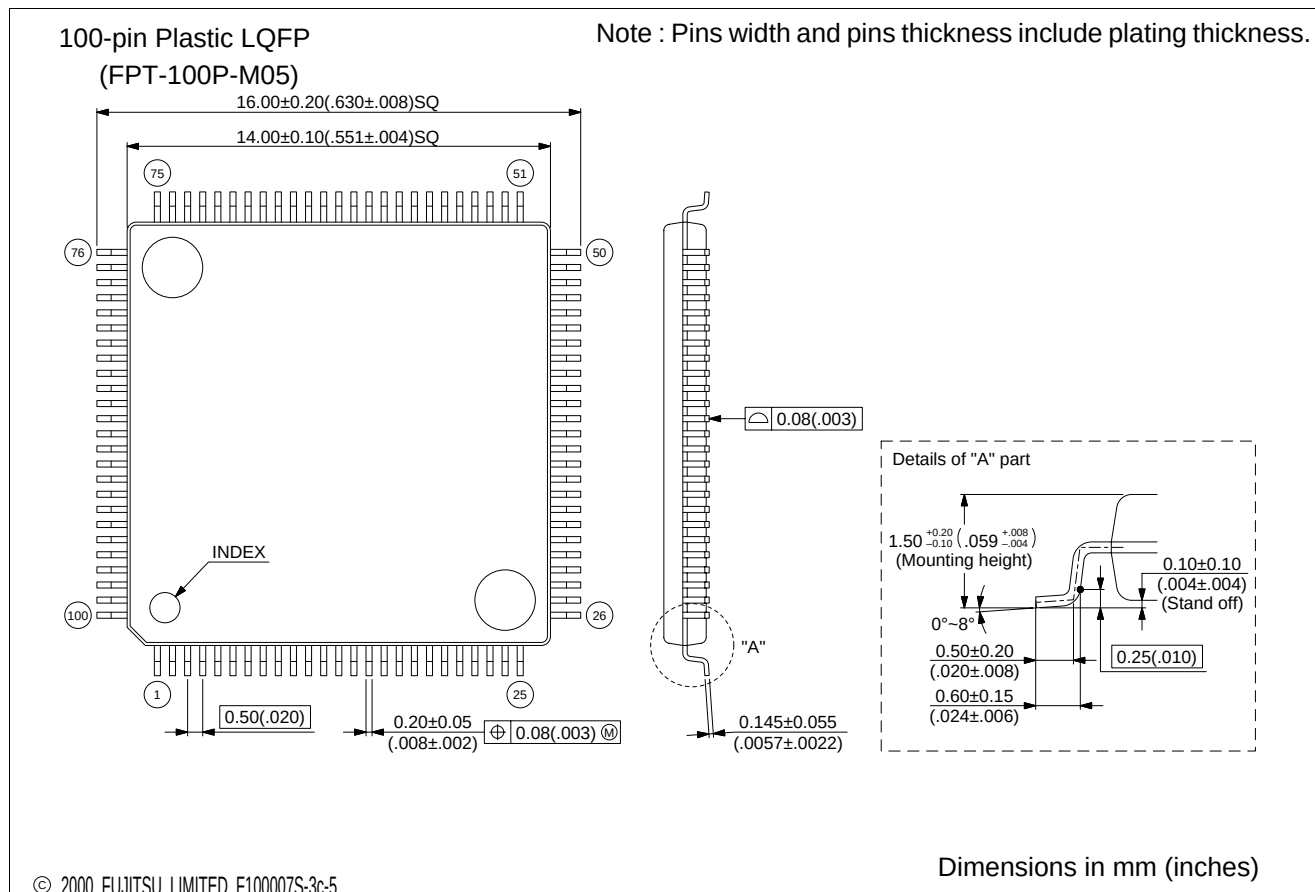
(6) Pull-up Resistance



■ ORDERING INFORMATION

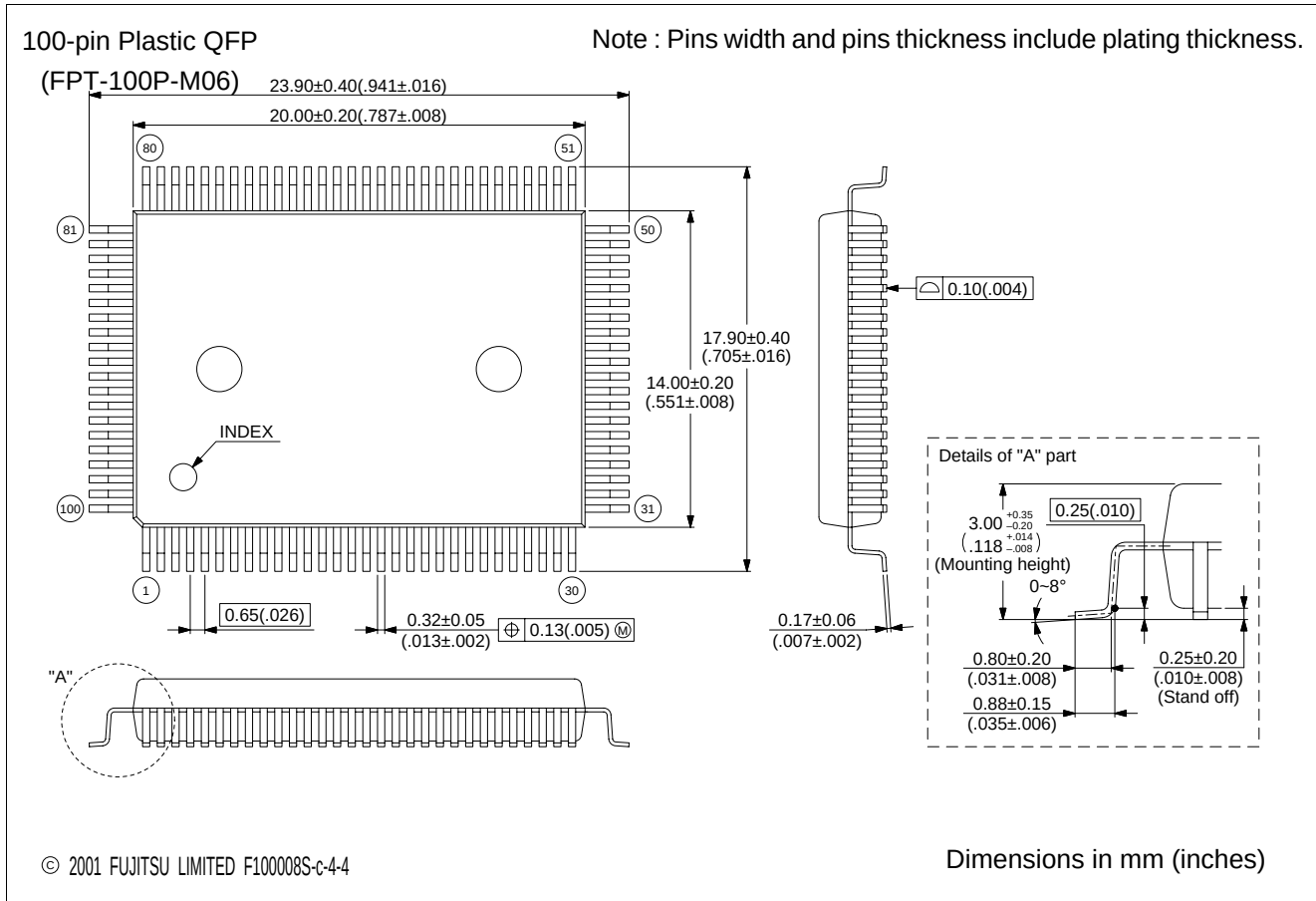
Part number	Package	Remarks
MB91F109PFV-XXX	100-pin Plastic LQFP (FPT-100P-M05)	
MB91F109PF-XXX	100-pin Plastic QFP (FPT-100P-M06)	

■ PACKAGE DIMENSIONS



(Continued)

(Continued)



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