FUJITSU SEMICONDUCTOR
DATA SHEET

DS06-20112-1E

Semicustom

CMOS

Embedded array

CE77 Series

■ DESCRIPTION

The CE77 series 0.25 µm CMOS embedded array is a line of highly integrated CMOS ASICs featuring high speed and low power consumption at the same time.

CE77 series is available in 15 frames with the enhanced lineup of 470 K to 6980 K gates.

■ FEATURES

- Technology : 0.25 µm silicon-gate CMOS, 3- to 4-layer wiring
- Supply voltage : +2.5 V ± 0.2 V (normal) to +1.5 V ± 0.1 V
- Junction temperature range : –40 °C to +125 °C
- Gate delay time : t_{pd} = 33 ps (2.5 V, inverter cell High Speed type, F/O = 1, No load)
- Gate power consumption : 0.02 µW/MHz (1.5 V, F/O = 1, No load)
- High-load driving capability : I_{OL} = 2 mA/4 mA/8 mA/12 mA mixable
- Output buffer cells with noise reduction circuits
- Inputs with on-chip input pull-up/pull-down resistors (25 kΩ typical) and bidirectional buffer cells
- Buffer cells dedicated to crystal oscillator
- Special interfaces (P-CML, LVDS, T-LVTTL, SSTL, PCI, USB, GTL+, and others including those under development)
- IP macros (CPU, PCI, USB, IrDA, PLL, DAC, ADC, and others including those under development)
- Capable of incorporating compiled cells (RAM/ROM/FIFO/Delay line, and others.)
- Configurable internal bus circuits
- Advanced hardware/software co-design environment
- Support for static timing sign-off
  Dramatically reducing the time for generating test vectors for timing verification and the simulation time
- Hierarchical design environment for supporting large-scale circuits
- Simulation (before layout) considering the input slew rate and detailed RC delay calculation (after layout) , supporting development with minimized timing trouble after trial manufacture

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- Support for memory (RAM/ROM) SCAN
- Support for memory (RAM) BIST
- Support for boundary SCAN
- Support for path delay test
- A variety of package options
  (QFP, TQFP, LQFP, HQFP, BGA, T-BGA, FCBGA under development)

■ MACRO LIBRARY (Including macros being prepared)

1. Logic cells (about 700 types)

- Adder
- AND-OR Inverter
- Clock Buffer
- Latch
- NAND
- AND
- NOR
- SCAN Flip Flop
- BUS Driver
- EOR
- Others
- AND-OR
- Decoder
- Non-SCAN Flip Flop
- Inverter
- Buffer
- OR-AND Inverter
- OR
- Selector
- ENOR
- Boundary Scan Register

2. IP macros

CPU	SPARClite, ARM7
Interface macro	USB, IrDA, etc.
Multimedia processing macros	JPEG, etc.
Mixed signal macros	ADC, DAC, Analog switch, etc.
Compiled macros	RAM, ROM, FIFO, Delay Line,
PLL	Analog PLL

3. Special I/O interface macros

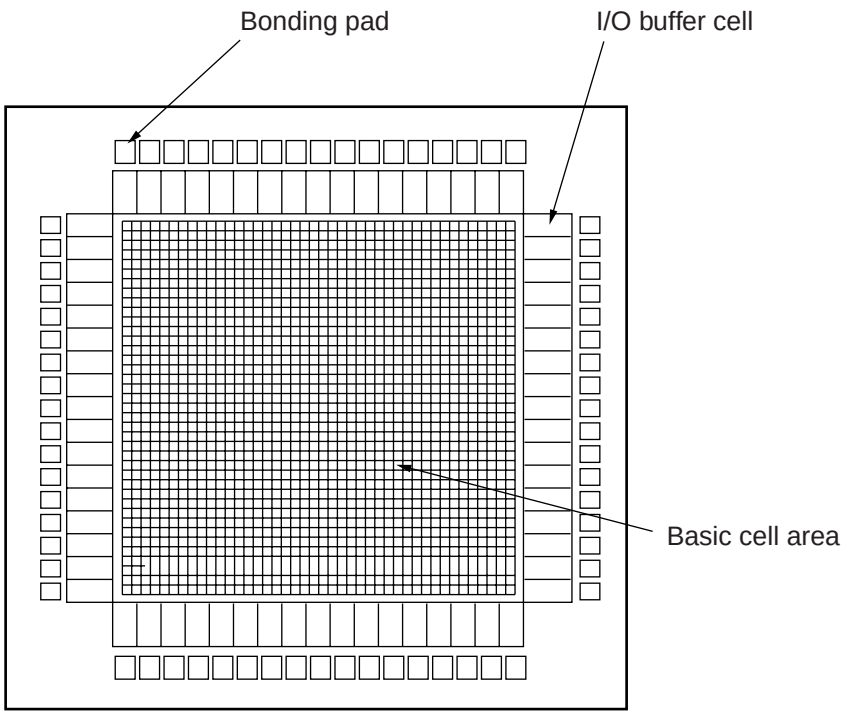
- P-CML
- USB

■ CHIP STRUCTURE

The chip layout of the CE77 series consists of two major areas : chip peripheral area and basic cell area.

The chip peripheral area contains the input/output buffer cells for interfacing with external devices and the associated bonding pads. The basic cell area contains some of input/output buffer cells, the unit cells and the compiled cells.

- Chip configuration



■ COMPILED CELLS

Compiled cells are macro cells which are automatically generated with the bit/word configuration specified. The CE77 series has the following types of compiled cells. (Note that each macro is different in word/bit range depending on the column type.)

1. Clock synchronous single-port RAM (1 address, 1 RW)

(High density type) / (Partial write type)

Column type	Memory capacity	Word range	Bit range	Unit
4	16 to 72 K	16 to 1 K	1 to 72	bit
16	64 to 72 K	64 to 4 K	1 to 18	bit

(Ultra high density type)

Column type	Memory capacity	Word range	Bit range	Unit
4	64 to 72 K	32 to 1 K	2 to 72	bit
4	2064 to 512 K	1032 to 4 K	2 to 128	bit
16	4160 to 512 K	2080 to 16 K	2 to 32	bit

(Low power consumption type)

Column type	Memory capacity	Word range	Bit range	Unit
4	128 to 72 K	32 to 1 K	4 to 72	bit
8	256 to 72 K	64 to 2 K	4 to 36	bit

(High speed type)

Column type	Memory capacity	Word range	Bit range	Unit
8	128 to 144 K	32 to 2 K	4 to 72	bit

2. Clock synchronous dual-port RAM (2 addresses, 1 RW/1 R)

Column type	Memory capacity	Word range	Bit range	Unit
4	16 to 72 K	16 to 1 K	1 to 72	bit
16	64 to 72 K	64 to 4 K	1 to 18	bit

3. Clock synchronous register file (3 address, 1W/2R)

Column type	Memory capacity	Word range	Bit range	Unit
1	4608	4 to 64	1 to 72	bit

4. Clock synchronous register file (4 address, 2W/2R)

Column type	Memory capacity	Word range	Bit range	Unit
1	4608	4 to 64	1 to 72	bit

5. Clock synchronous ROM (1 address, 1R)

Column type	Memory capacity	Word range	Bit range	Unit
8	128 to 512 K	32 to 4 K	4 to 128	bit
16	128 to 512 K	64 to 8 K	2 to 64	bit

6. Clock synchronous delay line memory (2 address, 1W/1R)

Column type	Memory capacity	Word range	Bit range	Unit
8	512 to 32 K	32 to 1 K	16 to 32	bit
16	512 to 32 K	64 to 2 K	8 to 16	bit
32	512 to 32 K	128 to 4 K	4 to 8	bit

7. Clock synchronous FIFO memory (2 address, 1W/1R)

Column type	Memory capacity	Word range	Bit range	Unit
8	512 to 32 K	32 to 1 K	16 to 32	bit
16	512 to 32 K	64 to 2 K	8 to 16	bit
32	512 to 32 K	128 to 4 K	4 to 8	bit

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0 V)

Parameter		Symbol	Application	Rating		Unit
				Min	Max	
Power supply voltage		V_{DD}	V_{DD} = 1.4 V to 2.7 V	− 0.5	+3.0*3	V
			V_{DD} = 2.7 V to 3.6 V		+4.0*4	
Input voltage		V_I	—	− 0.5	V_{DD} + 0.5 (≤ 3.0 V) *3	V
					V_{DD} + 0.5 (≤ 4.0 V) *4	
Output voltage		V_O	—	− 0.5	V_{DD} + 0.5 (≤ 3.0 V) *3	V
					V_{DD} + 0.5 (≤ 4.0 V) *4	
Storage temperature		TST	—	–55	+125	°C
Junction temperature		Tj	—	–40	+125	°C
Output current*1	L type	IO	Powerless type (I_{OL} = 2 mA)	—	±13	mA
	M type		Nomal type (I_{OL} = 4 mA)	—	±13	
	H type		Power type (I_{OL} = 8 mA)	—	±13	
	V type		High power type (I_{OL} = 12 mA)	—	±26	
Power-supply pin current *2		ID	Per V_{DD}, GND pin	—	60	mA

*1 : Maximum output current which can be supplied constantly.

*2 : Maximum supply current which can be supplied constantly.

*3 : Internal gate part in case of single power supply or dual power supply.

*4 : I/O part in case 3.3 V I/F or 2.5 V I/F is used by dual power supply.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

1. Single power supply

• Conditions: V_{DD} = 2.5 V±0.2 V, V_{SS} = 0 V

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Power supply voltage		V_{DD}	2.3	2.5	2.7	V
"H" level input voltage	CMOS normal	V_{IH}	1.7	—	V_{DD} + 0.3	V
	CMOS schmitt		V_{DD} × 0.8			
"L" level input voltage	CMOS normal	V_{IL}	–0.3	—	+0.7	V
	CMOS schmitt				V_{DD} × 0.2	
Junction temperature		T_j	–40	—	+125	°C

• Conditions: V_{DD} = 1.8 V±0.15 V, V_{SS} = 0 V

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Power supply voltage		V_{DDI}	1.65	1.8	1.95	V
"H" level input voltage	CMOS normal	V_{IH}	V_{DD} × 0.65	—	V_{DD} + 0.3	V
	CMOS schmitt		V_{DD} × 0.8			
"L" level input voltage	CMOS normal	V_{IL}	–0.3	—	V_{DD} × 0.35	V
	CMOS schmitt				V_{DD} × 0.2	
Junction temperature		T_j	–40	—	+125	°C

• Conditions: V_{DD} = 1.5 V±0.1 V, V_{SS} = 0 V

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Power supply voltage		V_{DDI}	1.4	1.5	1.6	V
"H" level input voltage	CMOS normal	V_{IH}	V_{DD} × 0.7	—	V_{DD} + 0.3	V
	CMOS schmitt		V_{DD} × 0.8			
"L" level input voltage	CMOS normal	V_{IL}	–0.3	—	V_{DD} × 0.3	V
	CMOS schmitt				V_{DD} × 0.2	
Junction temperature		T_j	–40	—	+125	°C

2. Dual power supply

• Conditions: V_{DDE} = 3.3 V±0.3 V/V_{DDI} = 2.5 V±0.2 V, V_{DDI} = 1.8 V±0.15 V, V_{DDI} = 1.5 V±0.1 V, V_{SS} = 0 V

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Power supply voltage		V_{DDE}	3.0	3.3	3.6	V
		V_{DDI}	1.4	—	2.7	
“H” level input voltage	1.5 V CMOS normal	V_{IH}	$V_{DDI} \times 0.7$	—	$V_{DDI} + 0.3$	V
	1.8 V CMOS normal		$V_{DDI} \times 0.65$			
	2.5 V CMOS normal		1.7			
	3.3 V CMOS normal		2.0		$V_{DDE} + 0.3$	
	1.5 V CMOS schmitt		$V_{DDI} \times 0.8$		$V_{DDI} + 0.3$	
	1.8 V CMOS schmitt					
	2.5 V CMOS schmitt					
	3.3 V CMOS schmitt		$V_{DDE} \times 0.8$		$V_{DDE} + 0.3$	
	5 V Tolerant		2.0		5.5	
“L” level input voltage	1.5 V CMOS normal	V_{IL}	–0.3	—	$V_{DDI} \times 0.3$	V
	1.8 V CMOS normal				$V_{DDI} \times 0.35$	
	2.5 V CMOS normal				0.7	
	3.3 V CMOS normal				0.8	
	1.5 V CMOS schmitt				$V_{DDI} \times 0.2$	
	1.8 V CMOS schmitt					
	2.5 V CMOS schmitt					
	3.3 V CMOS schmitt				$V_{DDE} \times 0.2$	
	5 V Tolerant				0.8	
Junction temperature		T_j	–40	—	+125	°C

• **Conditions:** V_{DDE} = 2.5 V±0.2 V/V_{DDI} = 1.8 V±0.15 V, V_{DDI} = 1.5 V±0.1 V, V_{SS} = 0 V

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Power supply voltage		V_{DDE}	2.3	2.5	2.7	V
		V_{DDI}	1.4	—	1.95	
"H" level input voltage	1.5 V CMOS normal	V_{IH}	$V_{DDI} \times 0.7$	—	$V_{DDI} + 0.3$	V
	1.8 V CMOS normal		$V_{DDI} \times 0.65$			
	2.5 V CMOS normal		1.7		$V_{DDE} + 0.3$	
	1.5 V CMOS schmitt		$V_{DDI} \times 0.8$		$V_{DDI} + 0.3$	
	1.8 V CMOS schmitt					
	2.5 V CMOS schmitt		$V_{DDE} \times 0.8$		$V_{DDE} + 0.3$	
"L" level input voltage	1.5 V CMOS normal	V_{IL}	–0.3	—	$V_{DDI} \times 0.3$	V
	1.8 V CMOS normal				$V_{DDI} \times 0.35$	
	2.5 V CMOS normal				0.7	
	1.5 V CMOS schmitt				$V_{DDI} \times 0.2$	
	1.8 V CMOS schmitt					
	2.5 V CMOS schmitt				$V_{DDE} \times 0.2$	
Junction temperature		T_j	–40	—	+125	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ DC CHARACTERISTICS

- **Single power supply** : V_{DD} = **2.5 V (Standard)**

(V_{DD} = 2.5 V ± 0.2 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Power supply current*1	I_{DDS}	T2	—	—	0.1	mA
		T3, T4	—	—	0.2	
		T5 to T7	—	—	0.3	
		T8, T9	—	—	0.4	
		TA	—	—	0.5	
		TB, TC	—	—	0.6	
		TD	—	—	0.8	
		TE	—	—	1.0	
		TF	—	—	1.1	
		TG	—	—	1.3	
“H” level output voltage	V_{OH}	I_{OH} = –100 µA	V_{DD} – 0.2	—	V_{DD}	V
“L” level output voltage	V_{OL}	I_{OL} = 100 µA	0	—	0.2	V
“H” level output voltage V-I characteristics	—	2.5 V V_{DD} = 2.5 V±0.2 V	*2	—	—	—
“L” level output current V-I characteristics	—	2.5 V V_{DD} = 2.5 V±0.2 V	*2	—	—	—
Input leakage current	I_L	—	—	—	±5	µA
Pull-up/pull-down resistance	R_P	Pull-up V_{IL} = 0 V Pull-down V_{IH} = V_{DD}	10	25	120	kΩ

*1 : When the memory is in a standby mode and analog macro is in a power-down mode. At both cases, conditions are V_{IH} = V_{DD}, V_{IL} = V_{SS}, and T_j = +25 °C. The above values may not be guaranteed when the input buffer with a pull-up/pull-down resistor or a crystal oscillator buffer is used.

*2 : See “(2) 2.5 V” in ■ V-I CHARACTERISTICS.

- **Single power supply** : V_{DD} = **1.8 V**

(V_{DD} = 1.8 V ± 0.15 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Power supply current*1	I_{DDS}	T2	—	—	0.1	mA
		T3, T4	—	—	0.2	
		T5 to T7	—	—	0.3	
		T8, T9	—	—	0.4	
		TA	—	—	0.5	
		TB, TC	—	—	0.6	
		TD	—	—	0.8	
		TE	—	—	1.0	
		TF	—	—	1.1	
		TG	—	—	1.3	
"H" level output voltage	V_{OH}	I_{OH} = –100 µA	V_{DD} – 0.2	—	V_{DD}	V
"L" level output voltage	V_{OL}	I_{OL} = 100 µA	0	—	0.2	V
"H" level output voltage V-I characteristics	—	1.8 V V_{DD} = 1.8 V±0.15 V	*2	—	—	—
"L" level output current V-I characteristics	—	1.8 V V_{DD} = 1.8 V±0.15 V	*2	—	—	—
Input leakage current	I_L	—	—	—	±5	µA
Pull-up/pull-down resistance	R_P	Pull-up V_{IL} = 0 V Pull-down V_{IH} = V_{DD}	10	40	120	kΩ

*1 : When the memory is in a standby mode and analog macro is in a power-down mode. At both cases, conditions are V_{IH} = V_{DD}, V_{IL} = V_{SS}, and T_j = +25 °C. The above values may not be guaranteed when the input buffer with a pull-up/pull-down resistor or a crystal oscillator buffer is used.

*2 : See "(3) 1.8 V" in ■ V-I CHARACTERISTICS.

- **Single power supply** : V_{DD} = **1.5 V**

(V_{DD} = 1.5 V ± 0.1 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Power supply current*1	I_{DDS}	T2	—	—	0.1	mA
		T3, T4	—	—	0.2	
		T5 to T7	—	—	0.3	
		T8, T9	—	—	0.4	
		TA	—	—	0.5	
		TB, TC	—	—	0.6	
		TD	—	—	0.8	
		TE	—	—	1.0	
		TF	—	—	1.1	
		TG	—	—	1.3	
"H" level output voltage	V_{OH}	I_{OH} = –100 µA	V_{DD} – 0.2	—	V_{DD}	V
"L" level output voltage	V_{OL}	I_{OL} = 100 µA	0	—	0.2	V
"H" level output voltage V-I characteristics	—	1.5 V V_{DD} = 1.5 V±0.1 V	*2	—	—	—
"L" level output current V-I characteristics	—	1.5 V V_{DD} = 1.5 V±0.1 V	*2	—	—	—
Input leakage current	I_L	—	—	—	±5	µA
Pull-up/pull-down resistance	R_P	Pull-up V_{IL} = 0 V Pull-down V_{IH} = V_{DD}	10	55	120	kΩ

*1 : When the memory is in a standby mode and analog macro is in a power-down mode. At both cases, conditions are V_{IH} = V_{DD}, V_{IL} = V_{SS}, and T_j = +25 °C. The above values may not be guaranteed when the input buffer with a pull-up/pull-down resistor or a crystal oscillator buffer is used.

*2 : See "(4) 1.5 V" in ■ V-I CHARACTERISTICS.

- **Dual power supply** : V_{DDE} = **3.3 V/**V_{DDI} = **2.5 V**, **1.8 V**, **1.5 V**

(V_{DDE} = 3.3 V ± 0.3 V/V_{DDI} = 2.5 V±0.2 V, 1.8 V ± 0.15 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C)

Parameter	Symbol	Conditions		Value			Unit
				Min	Typ	Max	
Power supply current*1	I_{DDS}	T2		—	—	0.1	mA
		T3, T4		—	—	0.2	
		T5 to T7		—	—	0.3	
		T8, T9		—	—	0.4	
		TA		—	—	0.5	
		TB, TC		—	—	0.6	
		TD		—	—	0.8	
		TE		—	—	1.0	
		TF		—	—	1.1	
		TG		—	—	1.3	
"H" level output voltage	V_{OH4}	3.3 V output I_{OH} = –100 µA		V_{DDE} – 0.2	—	V_{DDE}	V
	V_{OH3}	2.5 V output I_{OH} = –100 µA		V_{DDI} – 0.2	—	V_{DDI}	
	V_{OH2}	1.8 V output I_{OH} = –100 µA		V_{DDI} – 0.2	—	V_{DDI}	
	V_{OH1}	1.5 V output I_{OH} = –100 µA		V_{DDI} – 0.2	—	V_{DDI}	
"L" level output voltage	V_{OL4}	3.3 V output I_{OL} = 100 µA		0	—	0.2	V
	V_{OL3}	2.5 V output I_{OL} = 100 µA		0	—	0.2	
	V_{OL2}	1.8 V output I_{OL} = 100 µA		0	—	0.2	
	V_{OL1}	1.5 V output I_{OL} = 100 µA		0	—	0.2	
"H" level output V-I characteristics	—	3.3 V V_{DDE} = 3.3 V±0.3 V		*2	—	—	—
	—	2.5 V V_{DDI} = 2.5 V±0.2 V		*3	—	—	
	—	1.8 V V_{DDE} = 1.8 V±0.15 V		*4	—	—	
	—	1.5 V V_{DDI} = 1.5 V±0.1 V		*5	—	—	
"L" level output V-I characteristics	—	3.3 V V_{DDE} = 3.3 V±0.3 V		*2	—	—	—
	—	2.5 V V_{DDI} = 2.5 V±0.2 V		*3	—	—	
	—	1.8 V V_{DDE} = 1.8 V±0.15 V		*4	—	—	
	—	1.5 V V_{DDI} = 1.5 V±0.1 V		*5	—	—	
Input leakage current	I_L	—		—	—	±5	µA
Pull-up/pull-down resistance	R_P	3.3 V	Pull-up V_{IL} = 0 Pull-down V_{IH} = V_{DDE}	10	25	70	kΩ
		2.5 V	Pull-up V_{IL} = 0 Pull-down V_{IH} = V_{DDI}	10	25	120	
		1.8 V	Pull-up V_{IL} = 0 Pull-down V_{IH} = V_{DDI}	10	40	120	
		1.5 V	Pull-up V_{IL} = 0 Pull-down V_{IH} = V_{DDI}	10	55	120	

*1: When the memory is in a standby mode and analog macro is in a power-down mode. At both cases, conditions are V_{IH} = V_{DD}, V_{IL} = V_{SS}, and T_j = +25 °C. The above values may not be guaranteed when the input buffer with a pull-up/pull-down resistor or a crystal oscillator buffer is used.

*2: See "(1) 3.3 V" in ■ V-I CHARACTERISTICS.

*3: See "(2) 2.5 V" in ■ V-I CHARACTERISTICS.

*4: See "(3) 1.8 V" in ■ V-I CHARACTERISTICS".

*5: See "(4) 1.5 V" in ■ V-I CHARACTERISTICS.

- **Dual power supply** : V_{DDE} = **2.5 V/**V_{DDI} = **2.5 V**, **1.8 V**, **1.5 V**

(V_{DDE} = 2.5 V ± 0.2 V/V_{DDI} = 1.8 V±0.15 V, 1.5 V ± 0.1 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C)

Parameter	Symbol	Conditions		Value			Unit
				Min	Typ	Max	
Power supply current*1	I_{DDS}	T2		—	—	0.1	mA
		T3, T4		—	—	0.2	
		T5 to T7		—	—	0.3	
		T8, T9		—	—	0.4	
		TA		—	—	0.5	
		TB, TC		—	—	0.6	
		TD		—	—	0.8	
		TE		—	—	1.0	
		TF		—	—	1.1	
		TG		—	—	1.3	
"H" level output voltage	V_{OH3}	2.5 V output I_{OH} = –100 µA		V_{DDE} – 0.2	—	V_{DDE}	V
	V_{OH2}	1.8 V output I_{OH} = –100 µA		V_{DDI} – 0.2	—	V_{DDI}	
	V_{OH1}	1.5 V output I_{OH} = –100 µA		V_{DDI} – 0.2	—	V_{DDI}	
"L" level output voltage	V_{OL3}	2.5 V output I_{OL} = 100 µA		0	—	0.2	V
	V_{OL2}	1.8 V output I_{OL} = 100 µA		0	—	0.2	
	V_{OL1}	1.5 V output I_{OL} = 100 µA		0	—	0.2	
"H" level output V-I characteristics	—	2.5 V V_{DDE} = 2.5 V±0.2 V		*2	—	—	—
	—	1.8 V V_{DDI} = 1.8 V±0.15 V		*3	—	—	
	—	1.5 V V_{DDI} = 1.5 V±0.1 V		*4	—	—	
"L" level output V-I characteristics	—	2.5 V V_{DDE} = 2.5 V±0.2 V		*2	—	—	—
	—	1.8 V V_{DDI} = 1.8 V±0.15 V		*3	—	—	
	—	1.5 V V_{DDI} = 1.5 V±0.1 V		*4	—	—	
Input leakage current	I_L	—		—	—	±5	µA
Pull-up/pull-down resistance	R_P	2.5 V	Pull-up V_{IL} = 0 Pull-down V_{IH} = V_{DDE}	10	25	120	kΩ
		1.8 V	Pull-up V_{IL} = 0 Pull-down V_{IH} = V_{DDI}	10	40	120	
		1.5 V	Pull-up V_{IL} = 0 Pull-down V_{IH} = V_{DDI}	10	55	120	

*1: When the memory is in a standby mode and analog macro is in a power-down mode. At both cases, conditions are V_{IH} = V_{DD}, V_{IL} = V_{SS}, and T_j = +25 °C. The above values may not be guaranteed when the input buffer with a pull-up/pull-down resistor or a crystal oscillator buffer is used.

*2: See "(2) 2.5 V" in ■ V-I CHARACTERISTICS.

*3: See "(3) 1.8 V" in ■ V-I CHARACTERISTICS".

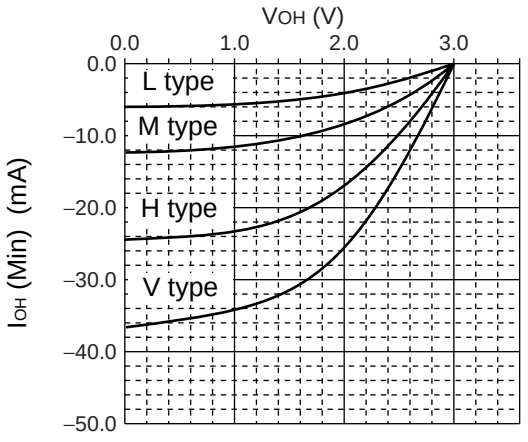
*4: See "(4) 1.5 V" in ■ V-I CHARACTERISTICS.

■ V-I CHARACTERISTICS

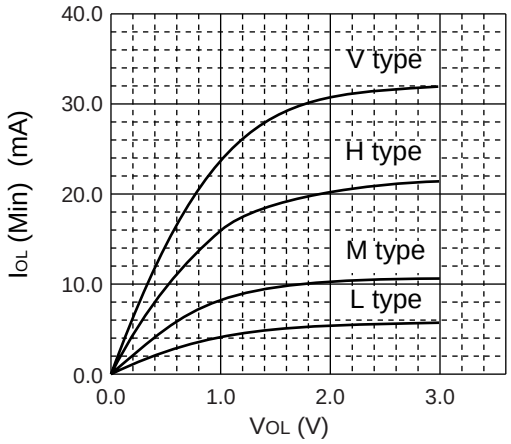
(1) 3.3 V

- 3.3 V normal I/O V-I characteristics [Condition : V_{DD} = 3.0 V]

"H" level output V-I characteristics (V_{DD} = 3.0 V)
3.0 V normal I/O V_{OH}-I_{OH} (Min) <V_{DD} = 3.0 V>

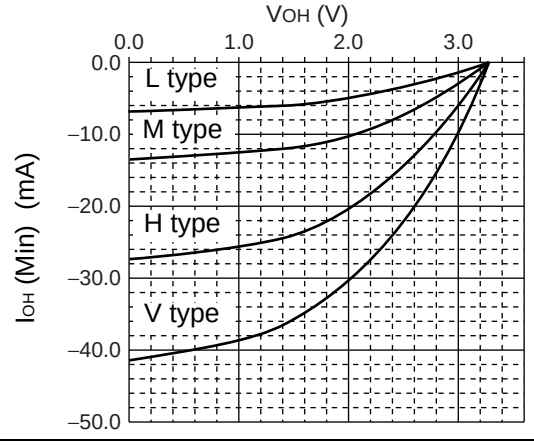


"L" level output V-I characteristics (V_{DD} = 3.0 V)
3.0 V normal I/O V_{OL}-I_{OL} (Min) <V_{DD} = 3.0 V>

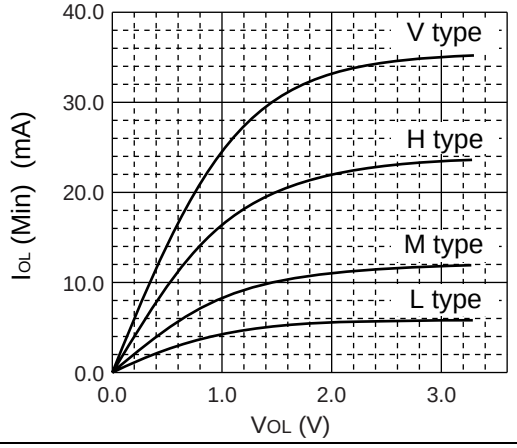


- 3.3 V normal I/O V-I characteristics [Condition : V_{DD} = 3.3 V]

"H" level output V-I characteristics (V_{DD} = 3.3 V)
3.3 V normal I/O V_{OH}-I_{OH} (Min) <V_{DD} = 3.3 V>

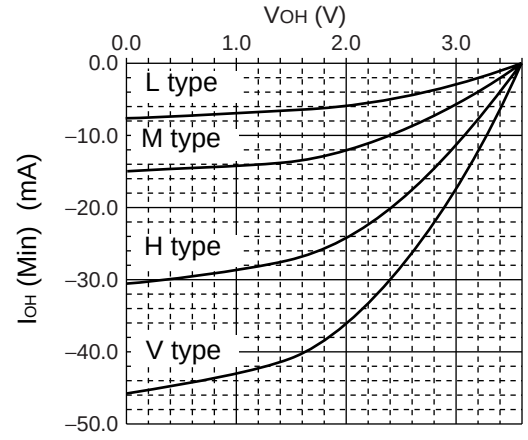


"L" level output V-I characteristics (V_{DD} = 3.3 V)
3.3 V normal I/O V_{OL}-I_{OL} (Min) <V_{DD} = 3.3 V>

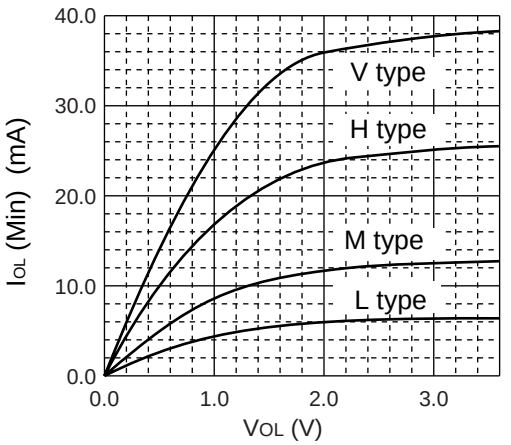


- 3.3 V normal I/O V-I characteristics [Condition : V_{DD} = 3.6 V]

"H" level output V-I characteristics (V_{DD} = 3.6 V)
3.3 V normal I/O V_{OH}-I_{OH} (Min) <V_{DD} = 3.6 V>



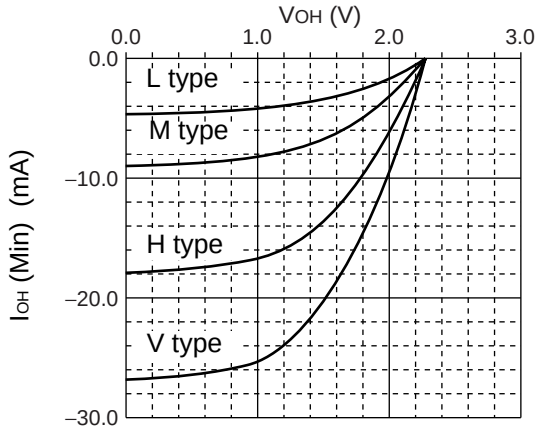
"L" level output V-I characteristics (V_{DD} = 3.6 V)
3.3 V normal I/O V_{OL}-I_{OL} (Min) <V_{DD} = 3.6 V>



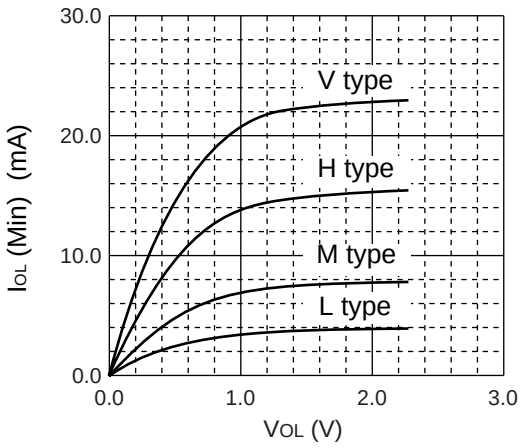
(2) 2.5 V

- 2.5 V normal I/O V-I characteristics [Condition : V_{DD} = 2.3 V]

"H" level output V-I characteristics (V_{DD} = 2.3 V)
2.5 V normal I/O V_{OH}-I_{OH} (Min) <V_{DD} = 2.3 V>

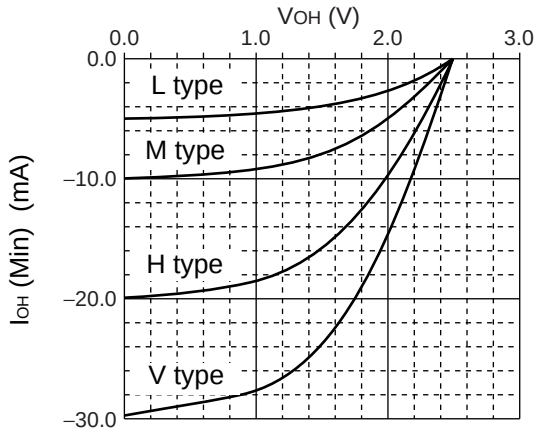


"L" level output V-I characteristics (V_{DD} = 2.3 V)
2.5 V normal I/O V_{OL}-I_{OL} (Min) <V_{DD} = 2.3 V>

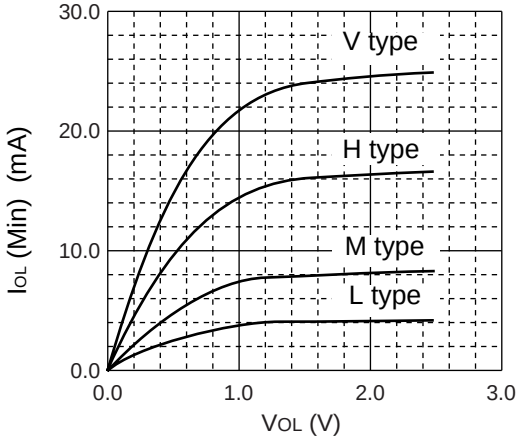


- 2.5 V normal I/O V-I characteristics [Condition : V_{DD} = 2.5 V]

"H" level output V-I characteristics (V_{DD} = 2.5 V)
2.5 V normal I/O V_{OH}-I_{OH} (Min) <V_{DD} = 2.5 V>

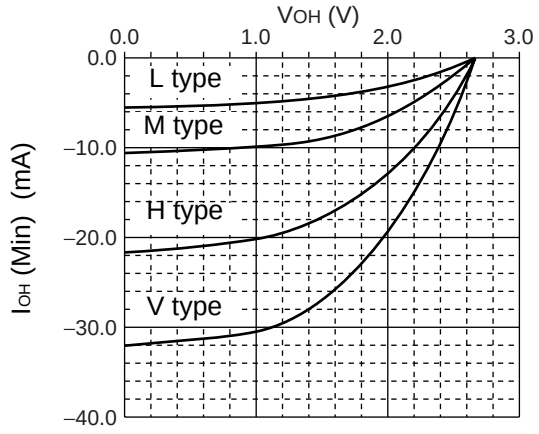


"L" level output V-I characteristics (V_{DD} = 2.5 V)
2.5 V normal I/O V_{OL}-I_{OL} (Min) <V_{DD} = 2.5 V>

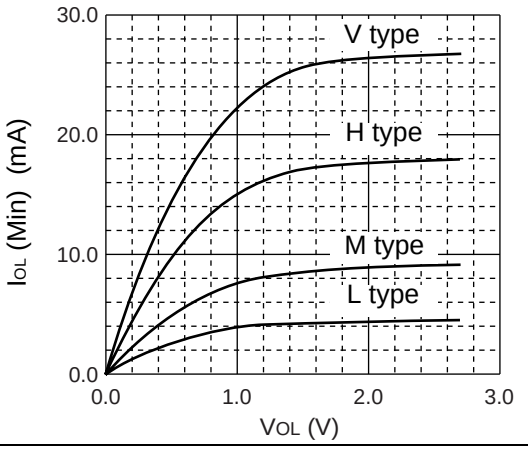


- 2.5 V normal I/O V-I characteristics [Condition : V_{DD} = 2.7 V]

"H" level output V-I characteristics (V_{DD} = 2.7 V)
2.5 V normal I/O V_{OH}-I_{OH} (Min) <V_{DD} = 2.7 V>



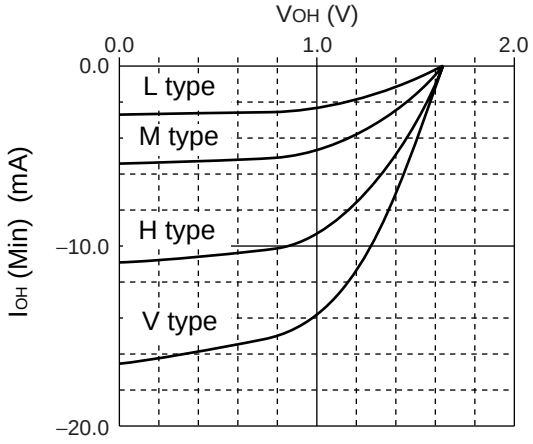
"L" level output V-I characteristics (V_{DD} = 2.7 V)
2.5 V normal I/O V_{OL}-I_{OL} (Min) <V_{DD} = 2.7 V>



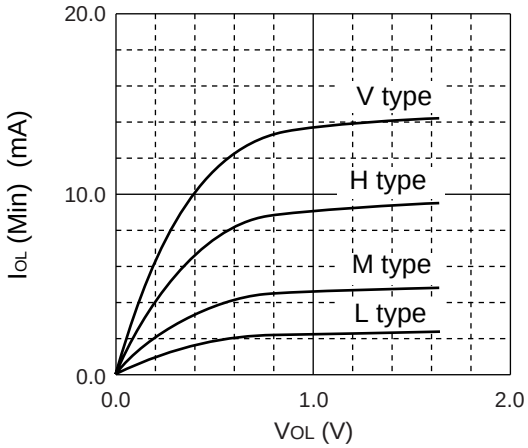
(3) 1.8 V

- 1.8 V normal I/O V-I characteristics [Condition : V_{DD} = 1.65 V]

"H" level output V-I characteristics (V_{DD} = 1.65 V)
1.8 V normal I/O V_{OH}-I_{OH} (Min) <V_{DD} = 1.65 V>

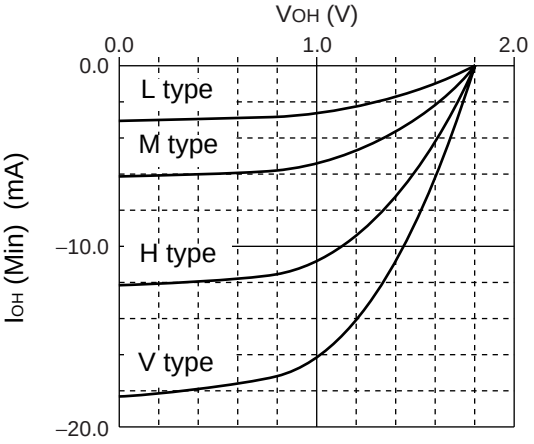


"L" level output V-I characteristics (V_{DD} = 1.65 V)
1.8 V normal I/O V_{OL}-I_{OL} (Min) <V_{DD} = 1.65 V>

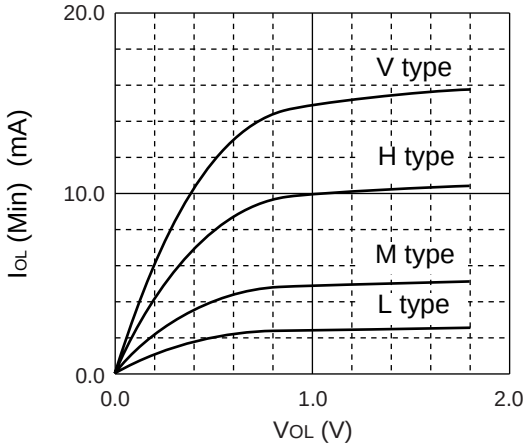


- 1.8 V normal I/O V-I characteristics [Condition : V_{DD} = 1.8 V]

"H" level output V-I characteristics (V_{DD} = 1.8 V)
1.8 V normal I/O V_{OH}-I_{OH} (Min) <V_{DD} = 1.8 V>

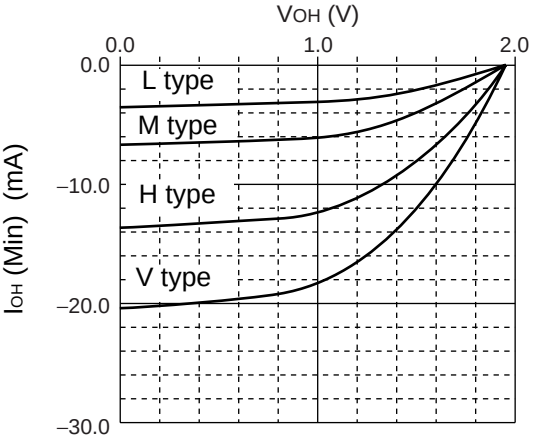


"L" level output V-I characteristics (V_{DD} = 1.8 V)
1.8 V normal I/O V_{OL}-I_{OL} (Min) <V_{DD} = 1.8 V>

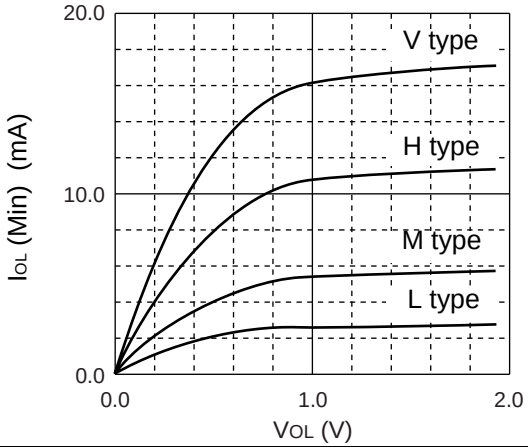


- 1.8 V normal I/O V-I characteristics [Condition : V_{DD} = 1.95 V]

"H" level output V-I characteristics (V_{DD} = 1.95 V)
1.8 V normal I/O V_{OH}-I_{OH} (Min) <V_{DD} = 1.95 V>



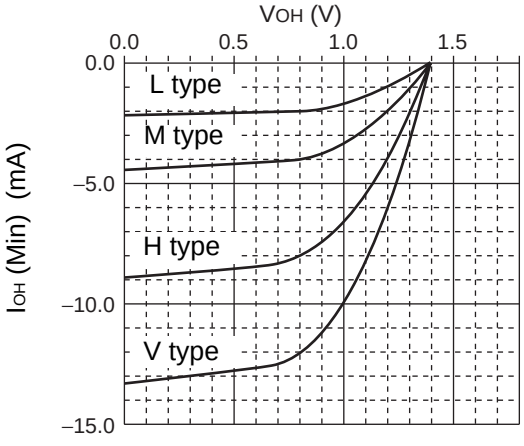
"L" level output V-I characteristics (V_{DD} = 1.95 V)
1.8 V normal I/O V_{OL}-I_{OL} (Min) <V_{DD} = 1.95 V>



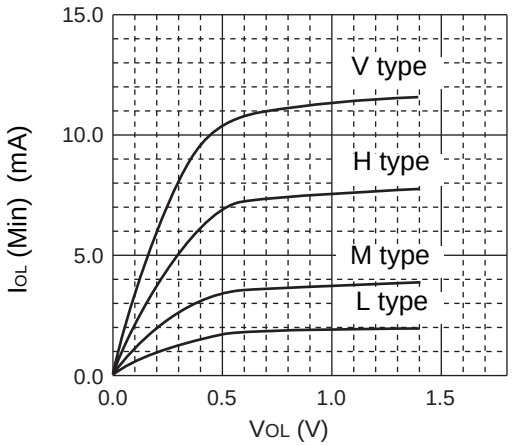
(4) 1.5 V

- 1.5 V normal I/O V-I characteristics [Condition : V_{DD} = 1.4 V]

"H" level output V-I characteristics (V_{DD} = 1.4 V)
1.5 V normal I/O V_{OH}-I_{OH} (Min) <V_{DD} = 1.4 V>

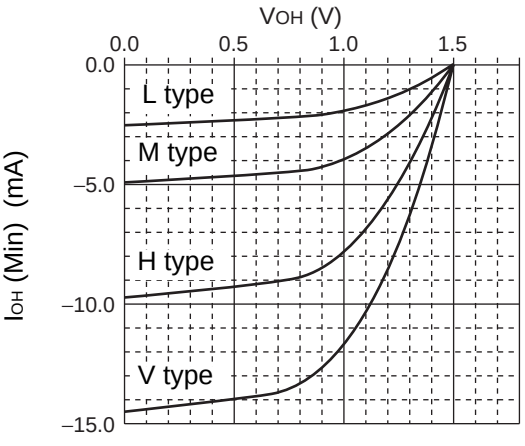


"L" level output V-I characteristics (V_{DD} = 1.4 V)
1.5 V normal I/O V_{OL}-I_{OL} (Min) <V_{DD} = 1.4 V>

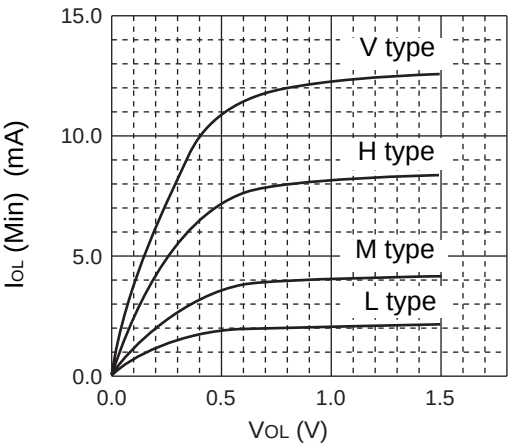


- 1.5 V normal I/O V-I characteristics [Condition : V_{DD} = 1.5 V]

"H" level output V-I characteristics (V_{DD} = 1.5 V)
1.5 V normal I/O V_{OH}-I_{OH} (Min) <V_{DD} = 1.5 V>

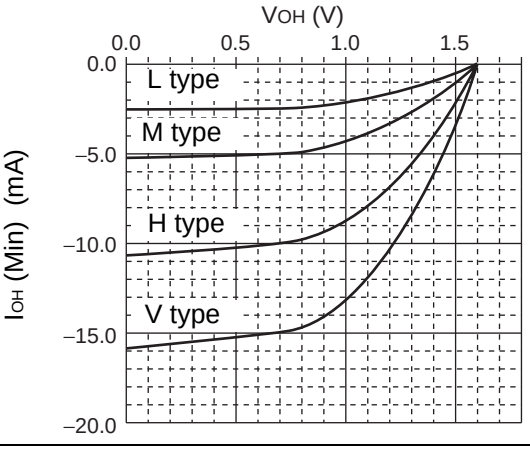


"L" level output V-I characteristics (V_{DD} = 1.5 V)
1.5 V normal I/O V_{OL}-I_{OL} (Min) <V_{DD} = 1.5 V>

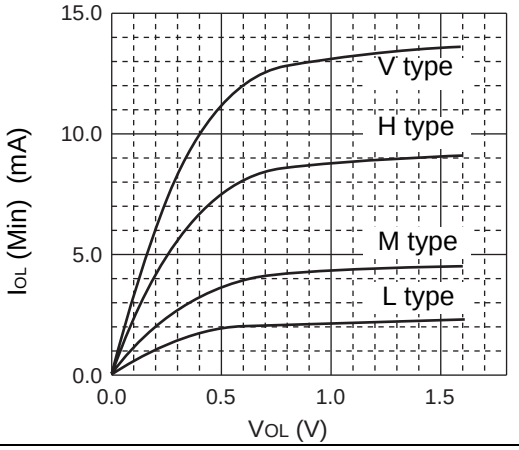


- 1.5 V normal I/O V-I characteristics [Condition : V_{DD} = 1.6 V]

"H" level output V-I characteristics (V_{DD} = 1.6 V)
1.5 V normal I/O V_{OH}-I_{OH} (Min) <V_{DD} = 1.6 V>



"L" level output V-I characteristics (V_{DD} = 1.6 V)
1.5 V normal I/O V_{OL}-I_{OL} (Min) <V_{DD} = 1.6 V>



■ AC CHARACTERISTICS

(V_{DD} = 1.8 V ± 0.15 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Delay time	t_{pd}*1	typ*2 × tmin*3	typ*2 × ttyp*3	typ*2 × tmax*3	ns

*1 : Delay time = propagation delay time, enable time, disable time

*2 : “typ” is calculated from the cell specification.

*3 : Measurement condition

Measurement condition	tmin	ttyp	tmax
V_{DD} = 2.5 ± 0.2 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C	0.60	1.00	1.64
V_{DD} = 1.8 ± 0.15 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C	0.84	1.57	2.84
V_{DD} = 1.5 ± 0.1 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C	1.14	2.22	4.09

Note : tpd Max is calculated according to the maximum junction temperature (T_j) .

■ INPUT/OUTPUT CAPACITANCE

(f = 1 MHz, V_{DD} = V_I = 0 V, Tj = +25 °C)

Parameter	Symbol	Value	Unit
Input pin	C_{IN}	Max 16	pF
Output pin	C_{OUT}	Max 16	pF
Input/output capacitance	$C_{I/O}$	Max 16	pF

■ DESIGN METHOD

Linking a floor plan tool and a logic synthesis tool enables automatic circuit optimization using floor plan information. In addition, CDDM (Clock Driven Design Method) clock tree synthesis tools using floor plan information is also available. Using floor plan information at a pre-layout stage prevents major problems with setup and hold timings which can occur after layout. Using a hierarchical layout method to support larger-scale circuit design considerably shortens the overall design cycle time.

■ SUPPORT TOOLS

- Simulation
  Synopsys, Inc. : VCS
  Cadence Design Systems, Inc. : Verilog-XL, NC-Verilog, NC-VHDL
  Model Technology, Inc./Mewtor Graphics, Inc : Model-Sim
  FUJITSU LIMITED : LCADFE
- Logic synthesis
  Synopsys, Inc. : DesignCompiler (Including Design Power/Power Compiler)
- Floor plan
  FUJITSU LIMITED : GLOSCAD
- Clock tree
  FUJITSU LIMITED : GLOSCAD
- Timing analysis
  Synopsys, Inc. : PrimeTime
  FUJITSU LIMITED : GISTA
- Power calculation
  Sequence, Inc. : Watt Watcher
  FUJITSU LIMITED : PScope
- Layout
  Cadence Design Systems, Inc. : Gate Ensemble DSM
  FUJITSU LIMITED : GLOSCAD
- Test tools
  FUJITSU LIMITED : ATREX, FANTCAD, RAPARA, TERBAN, FANSCAD
- Format verification
  Verplex, Inc : Tuxed-LEC
  Synopsys, Inc : Formality
  Chrysalis Symbolic Design, Inc. : Design VERIFYer
  FUJITSU LIMITED : ASSURE
- Verification tool
  Cadence Design Systems, Inc. : Dracula/Assura

■ THE NUMBER OF GATES USED AND PACKAGES

1. Counting the number of the gates used

Evaluation of the basic cell count used has revealed some problems including the circuit complexities, difference of the utilization depending on the circuit design scheme (whether it is designed with the logic synthesis) or being unable to achieve the minimum layout with the logically synthesized circuit.

To cope with those problems, Fujitsu developed the AREA as a criteria where the circuit size and the layout feasibility is determined. The AREA is a basic cell conceived from the viewpoint of congestion of the wiring; it has been calculated from the actual basic cell count and pin count in units of BC.

Estimate method for the frame include the conventional one by the basic cell count and the one by the AREA for more detailed estimate.

Hard macro basic cell count and AREA count for unit cell, I/O buffer cell or compiled cell are listed in the respective cell characteristic table.

2. Packages

The table below lists the package types available and the reference number of gates used.

Consult Fujitsu for the combination of each package and the availability.

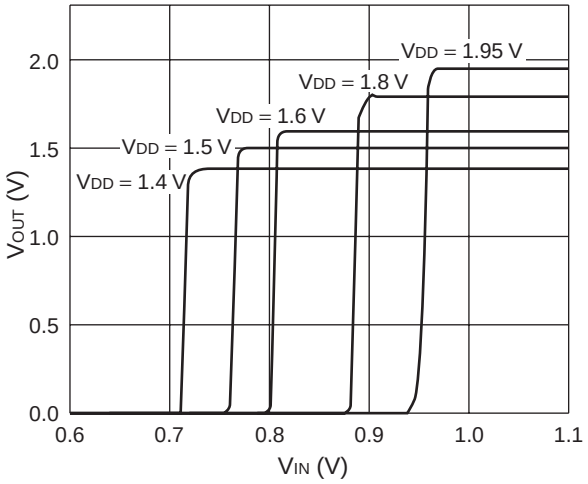
CE77

Package and Pin count		0 500 k 1000 k 1500 k 2000 k 2500 k 3000 k 3500 k 4000 k 4500 k 5000 k 5500 k	material
LQFP	144	976 k	●
	176	744 k	●
	208	1375 k	●
	256	1841 k	●
HQFP	208	1375 k	●
	240	1609 k	●
	256	2109 k	●
	304	4538 k	●
FBGA	144	461 k	●
	176	646 k	●
	224	1375 k	●
	228	2109 k	●
PBGA	256	1841 k	●
	352	2678 k	●
	420	3789 k	●

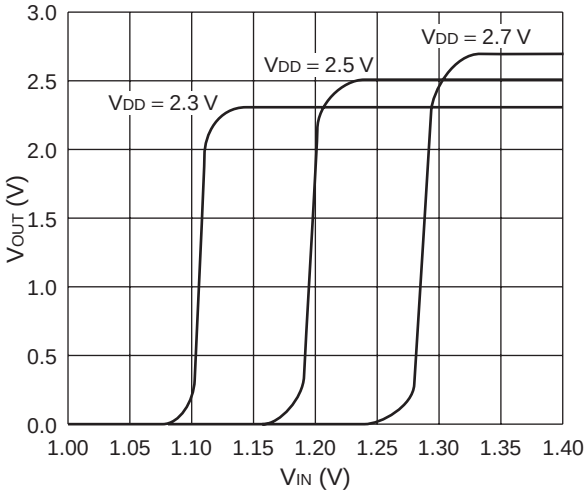
Note : This list contains packages under planning. ● : Plastic

■ BASIC CHARACTERISTICS

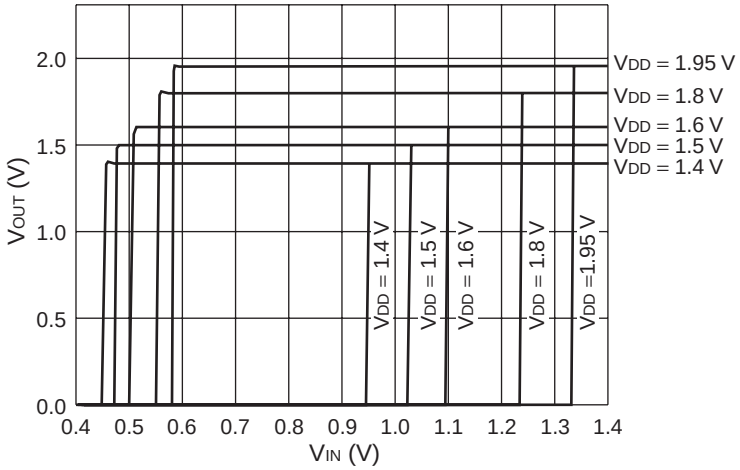
Transfer characteristics
(Typical CMOS input buffer) 1



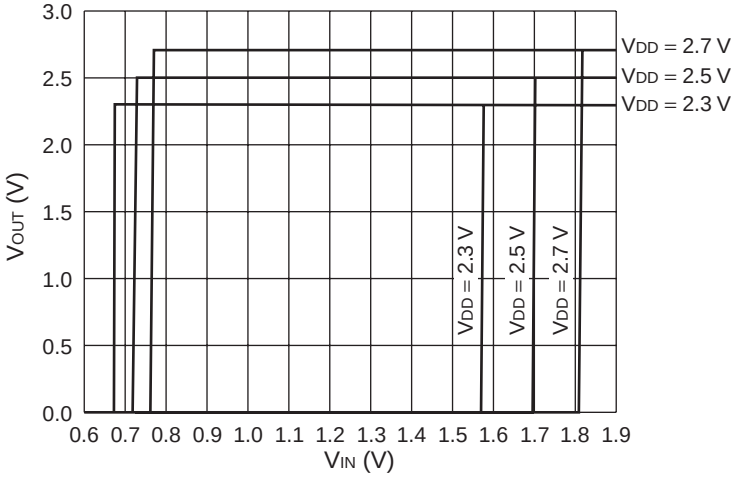
Transfer characteristics
(Typical CMOS input buffer) 2



Transfer characteristics (Typical schmitt input buffer) 1



Transfer characteristics (Typical schmitt input buffer) 2



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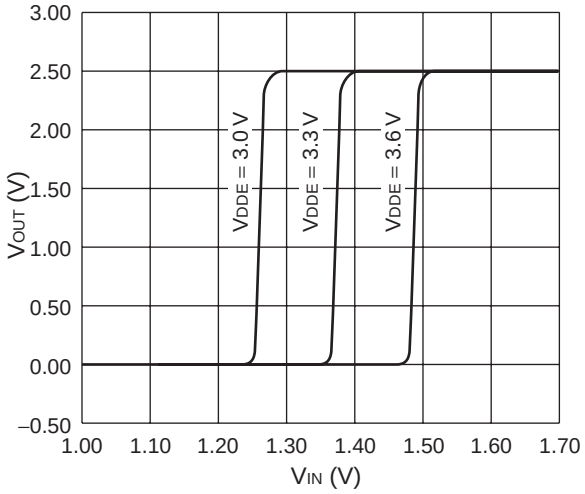
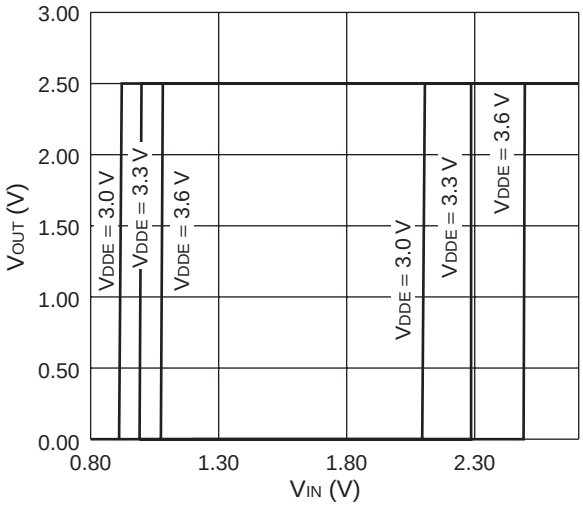
Transfer characteristics (3.3 V normal CMOS input buffer V_{DDI} = 2.5 V)



Transfer characteristics (3.3 V normal schmitt input buffer V_{DDI} = 2.5 V)



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