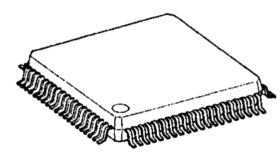
CMOS 8-Bit Microcontroller

TMP86FP24F

The TMP86FP24 is a Flash type MCU which includes 48 K bytes Flash memory. It is a pin compatible with a mask ROM product of the TMP86CP24. Writing the program to built-in Flash memory, the TMP86FP24 operates as the same way as the TMP86CP24. The TMP86FP24 has a 2 K bytes BOOT ROM (masked ROM) for programming to Flash memory.

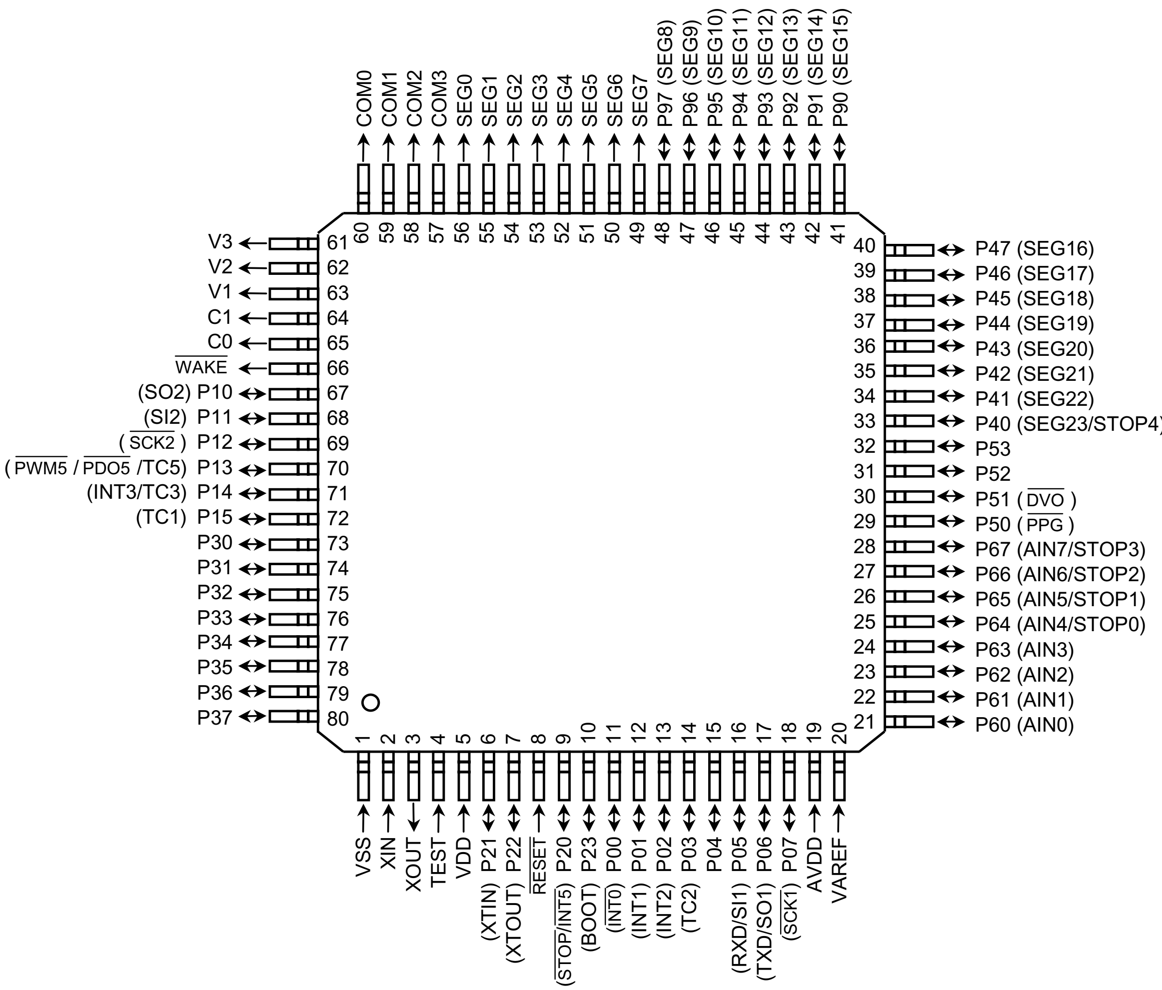
Product No.	Flash Memory	BOOT ROM	RAM	Package
TMP86FP24F	48 K × 8 bits	2 K × 8 bits	2 K × 8 bits	P-LQFP80-1212-0.50A



TMP86FP24F

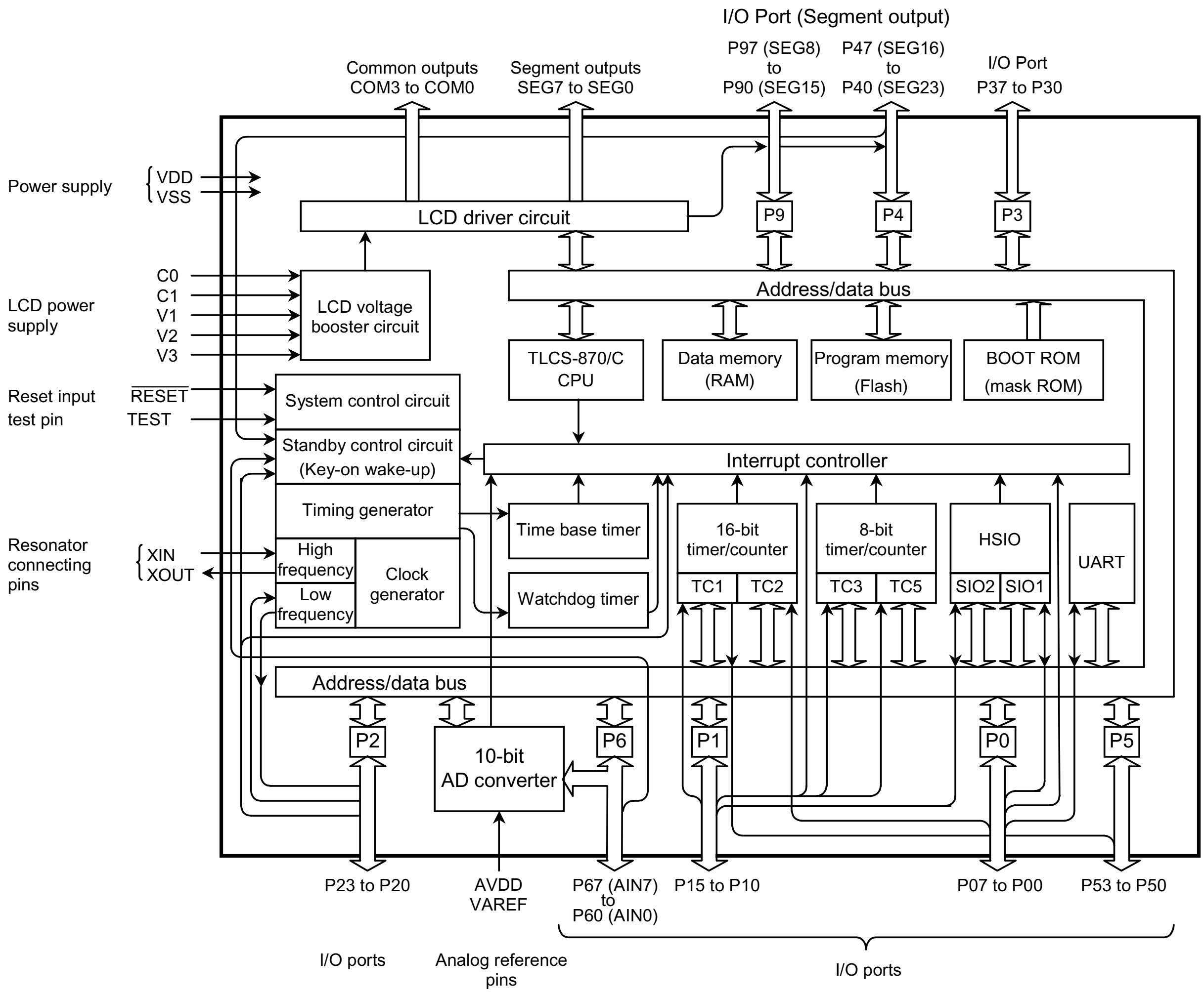
Pin Assignments (Top View)

P-LQFP80-1212-0.50A



Note: The mask ROM product (TMP86CP24) doesn't have a BOOT function in P23 pin.

Block Diagram



Pin Funtions

The TMP86FP24 has MCU mode and serial PROM mode.

(1)MCU mode

In the MCU mode, the TMP86FP24 is a pin compatible with the TMP86CP24 (Make sure to fix the TEST pin to low level).

(2)Serial PROM mode

In the Serial PROM mode, programming to Flash memory is available by executing BOOT ROM. For details, refer to “2.1 Serial PROM mode”.

1.1 FLASH Memory

1.1.1 Outline

The TMP86FP24 incorporates 49152 bytes of FLASH memory (address 4000H to FFFFH). The writing to FLASH is controlled by FLASH control register (EEPCR), FLASH status register (EEPSR) and FLASH write emulate time control register (EEPEVA).

To write data to the FLASH , execute the Serial PROM mode. For details about the Serial PROM mode, refer to "2.1 Serial PROM mode".

The FLASH memory of the TMP86FP24 features:

- The FLASH memory is constructed of 384 pages FLASH and one page size is 128 bytes (384 pages × 128 bytes = 49512 bytes).
- The TMP86FP24 incorporates a 128-byte temporary data buffer. The data written to FLASH is temporarily stored in this data buffer. After 128 bytes data have been written to the temporary data buffer, the writing to FLASH automatically starts by page writing (The 128 bytes data are written to specified page of FLASH simultaneously). At the same time, page-by-page erasing occurs automatically. So, it is unnecessary to erase individual pages in advance.
- The FLASH control circuit incorporates an oscillator dedicated to the FLASH. So FLASH writing time is independent of the system clock frequency (fc). In addition, because an FLASH control circuit controls writing time for each FLASH cell, the writing time varies in each page (Typically 4 ms per page).
- Controlling the power for the FLASH control circuit (regulator and voltage step-up circuit) achieves low power consumption if the FLASH is not in use (Example. When the program is executed in RAM area).

1.1.2 Conditions for Accessing the FLASH Areas

The conditions for accessing the FLASH areas vary depending on each operation mode. The following tables shows FLASH are access conditions.

Table 1.1.1 FLASH Area Access Conditions

	Area	Operation Mode	
		MCU mode (Note 1)	Serial PROM mode (Note 2)
FLASH Memory	4000H to FFFFH	Read/Fetch only	Write/Read/Fetch supported

Note1: "MCU mode" shows NORMAL1/2 and SLOW1/2 modes.

Note2: "Serial PROM mode" shows the FLASH controlling mode. For details, refer to "2.1 Serial PROM mode".

Note3: "Fetch" means reading operation of FLASH data as an instruction by CPU.

2.1 Serial PROM Mode

2.1.1 Outline

The TMP86FP24 has a 2 Kbytes BOOT-ROM for programming to FLASH memory. This BOOT-ROM is a mask ROM that contains a program to write the FLASH memory on-board. The BOOT-ROM is available in a serial PROM mode and it is controlled by BOOT pin (P23) and $\overline{\text{RESET}}$ pin, and is communicated via TXD (P06) and RXD (P05) pins. There are four operation modes in a serial PROM mode: FLASH writing mode, RAM loader mode, FLASH memory SUM output mode and Product discrimination code output mode. Operating area of serial PROM mode differs from that of MCU mode. The operating area of serial PROM mode shows in Table 2.1.1.

Table 2.1.1 Operating Area of Serial PROM Mode

Parameter	Min	Max	Unit
Operating voltage	2.7	3.6	V
High frequency (Note)	2	16	MHz
Temperature	25 ± 5		℃

Note: Even though included in above operating area, part of frequency can not be supported in serial PROM mode. For details, refer to Table 2.1.4.

2.1.2 Memory Mapping

The BOOT-ROM is mapped in address 3800H to 3FFFH. The Figure 2.1.1 shows a memory mapping.

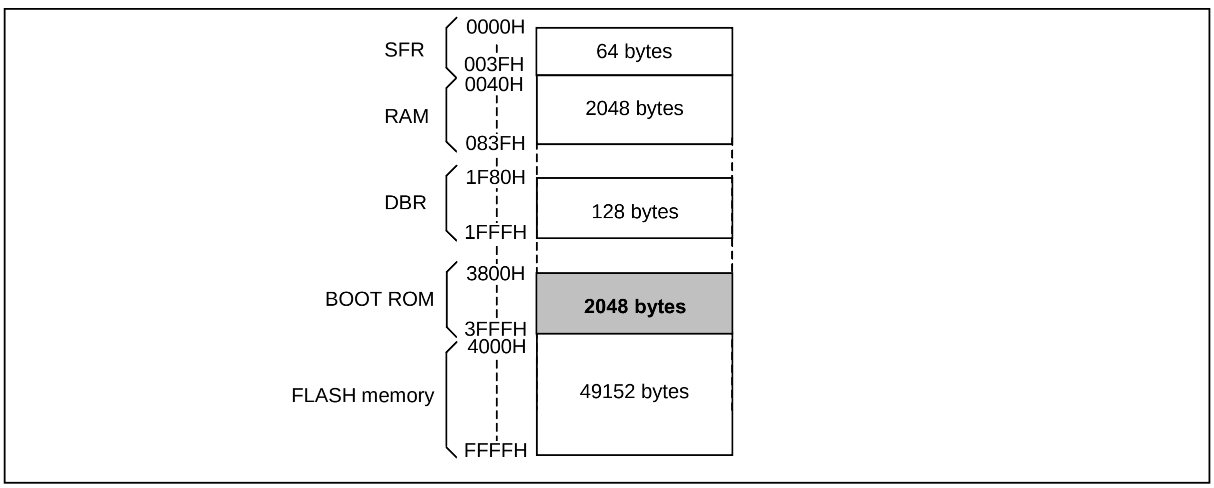


Figure 2.1.1 Memory Address Maps

2.1.3 Serial PROM Mode Setting

2.1.3.1 Serial PROM Mode Control Pins

To execute on-board programming, start the TMP86FP24 in serial PROM mode. Setting of a serial PROM mode is shown in Table 2.1.2.

Table 2.1.2 Serial PROM Mode Setting

Pin	Setting
TEST pin	High
BOOT pin (P23)	High
$\overline{\text{RESET}}$ pin	

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Pins	Rating	Unit
Supply voltage	V_{DD}		–0.3 to 4.0	V
Input voltage	V_{IN}		–0.3 to V_{DD} + 0.3	
Output voltage	V_{OUT1}	Except V3 pin	–0.3 to V_{DD} + 0.3	
	V_{OUT2}	V3 pin	-0.3 to 4.0	
Output current (Per 1 pin)	I_{OUT1}	P0, P1, P20, P23, P3, P5, P6 Ports	–2	mA
	I_{OUT2}	P0, P1, P2, P4, P6, P9, $\overline{\text{WAKE}}$ Ports	2	
	I_{OUT3}	P3, P5 Ports	10	
Output current (Total)	ΣI_{OUT1}	P0, P1, P20, P23, P3, P5, P6 Ports	–80	
	ΣI_{OUT2}	P0, P1, P2, P4, P6, P9, $\overline{\text{WAKE}}$ Ports	80	
	ΣI_{OUT3}	P3, P5 Ports	30	
Power dissipation [Topr = 85°C]	PD		350	mW
Soldering temperature (time)	Tsld		260 (10 s)	°C
Storage temperature	Tstg		–55 to 125	
Operating temperature	Topr		–40 to 85	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Condition-1 (V_{SS} = 0 V, Topr = –40 to 85°C)

Parameter	Symbol	Pins	Condition		Min	Max	Unit
Supply voltage	V_{DD}		fc = 16 MHz	NORMAL1, 2 mode	2.7	3.6	V
				IDLE0, 1, 2 mode			
			fc = 8 MHz	NORMAL1, 2 mode	1.8		
				IDLE0, 1, 2 mode			
			fs = 32.768 kHz	SLOW1, 2 mode	1.8		
				SLEEP0, 1, 2 mode			
				STOP mode			
Input high level	V_{IH1}	Except hysteresis input	V_{DD} ≥ 2.7 V		V_{DD} × 0.70	V_{DD}	
	V_{IH2}	Hysteresis input			V_{DD} × 0.75		
	V_{IH3}		V_{DD} < 2.7 V		V_{DD} × 0.80		
Input low level	V_{IL1}	Except hysteresis input	V_{DD} ≥ 2.7 V		0	V_{DD} × 0.30	
	V_{IL2}	Hysteresis input				V_{DD} × 0.25	
	V_{IL3}		V_{DD} < 2.7 V			V_{DD} × 0.20	
Clock frequency	fc	XIN, XOUT	V_{DD} = 1.8 to 3.6 V		1.0	8.0	MHz
			V_{DD} = 2.7 to 3.6 V			16.0	
	fs	XTIN, XTOUT	V_{DD} = 1.8 to 3.6 V		30.0	34.0	kHz
LCD reference voltage	V1		Booster circuit is enable ($V3 \geq V_{DD}$)		0.8	1.2	V
	V2				1.6	2.4	
Capacity for LCD booster circuit	C_{LCD}		LCD booster circuit is enable ($V3 \geq V_{DD}$)		0.1	0.47	μF

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Recommended Operating Condition-2 (Serial PROM mode) (V_{SS} = 0 V, Topr = 25°C ± 5°C)

Parameter	Symbol	Pins	Condition	Min	Max	Unit
Supply voltage	VDD		2 MHz ≤ fc ≤ 16MHz	2.7	3.6	V
Clock frequency	fc	XIN, XOUT	VDD = 2.7 to 3.6 V	2.0	16.0	MHz

Note: The operating temperature area of serial PROM mode is 25°C ± 5°C and the operating area of high frequency of serial PROM mode is different from MCU mode.

DC Characteristics (V_{SS} = 0 V, Topr = –40 to 85°C)

Parameter	Symbol	Pins	Condition	Min	Typ.	Max	Unit
Hysteresis voltage	V_{HS}	Hysteresis input	V_{DD} = 3.3 V	–	0.4	–	V
Input current	I_{IN1}	TEST	V_{DD} = 3.6 V, V_{IN} = 0 V	–	–	–5	μA
	I_{IN2}	Sink-open drain, Tri-state	V_{DD} = 3.6 V, V_{IN} = 3.6 V/0 V	–	–	±5	
	I_{IN4}	$\overline{\text{RESET}}$	V_{DD} = 3.6 V, V_{IN} = 3.6 V	–	–	+5	
Input resistance	R_{IN1}	TEST pull-down	V_{DD} = 3.6 V, V_{IN} = 3.6 V	–	70	–	kΩ
	R_{IN2}	$\overline{\text{RESET}}$ pull-Up P21, P22 ports	V_{DD} = 3.6 V, V_{IN} = 0 V	100	220	450	
	R_{IN3}	Programmable pull-down (P4, P9 ports)		–	T.B.D.	–	
High frequency feedback resister	R_{FB}	XOUT	V_{DD} = 3.6 V	–	1.2	–	MΩ
Low frequency feedback resister	R_{FBT}	XTOUT	V_{DD} = 3.6 V	–	14	–	
Output leakage current	I_{LO}	Sink-open drain, Tri-state	V_{DD} = 3.6 V V_{OUT} = 3.4V / 0.2 V	–	–	±10	μA
Output high voltage	V_{OH}	C-MOS, Tri-state	V_{DD} = 3.6 V, I_{OH} = –0.6 mA	3.2	–	–	V
Output low voltage	V_{OL}	Except XOUT, P3 and P5 Ports	V_{DD} = 3.6 V, I_{OL} = 0.9 mA	–	–	0.4	
Output low current	I_{OL}	P3, P5 ports	V_{DD} = 3.6 V, V_{OL} = 1.0 V	–	6	–	mA
LCD output voltage (LCD booster is enable)	$V_{2\text{-}3OUT}$	V2 pin	V3 ≥ V_{DD} Reference supply pin: V1 SEG/COM pin: No-load	–	V1 × 2	–	V
		V3 pin		–	V1 × 3	–	
	$V_{1\text{-}3OUT}$	V1 pin	V3 ≥ V_{DD} Reference supply pin: V2 SEG/COM pin: No-load	–	V2 × 1/2	–	
		V3 pin		–	V2 × 3/2	–	
LCD output current capacity (LCD booster is enable)	I_{LCDV3}	V3 pin	V_{DD} = 3.6 V, fc = 16 MHz, C_{LCD} = 0.1 μF, Reference supply pin: V1 = 1V; <VFSEL> = 00	–	T.B.D.	–	mV/μA
			<VFSEL> = 01	–	T.B.D.	–	
			<VFSEL> = 10	–	T.B.D.	–	
			<VFSEL> = 11	–	T.B.D.	–	
			V_{DD} = 3.6 V, fc = 16 MHz, C_{LCD} = 0.1 μF, Reference supply pin: V2 = 2 V; <VFSEL> = 00	–	T.B.D.	–	
			<VFSEL> = 01	–	T.B.D.	–	
			<VFSEL> = 10	–	T.B.D.	–	
			<VFSEL> = 11	–	T.B.D.	–	
Supply current in NORMAL1, 2 mode	I_{DD}	Fetch area: Flash area	V_{DD} = 3.6 V, V_{IN} = 3.4 V/0.2 V, fc = 16 MHz, fs = 32.768 kHz; MNP = “1”	–	T.B.D.	T.B.D.	mA
		Fetch area: RAM area	MNP = “0”	–	T.B.D.	T.B.D.	
			MNP = “1”	–	T.B.D.	T.B.D.	
Supply current in IDLE0, 1, 2 mode			MNP·ATP = “1”	–	T.B.D.	T.B.D.	
			MNP·ATP = “0”	–	T.B.D.	T.B.D.	
Supply current in SLOW1 mode		Fetch area: Flash area	V_{DD} = 3.6 V, V_{IN} = 3.4 V/0.2 V, fs = 32.768 kHz; MNP = “1”	–	T.B.D.	T.B.D.	μA
		Fetch area: RAM area	MNP = “0”	–	T.B.D.	T.B.D.	
			MNP = “1”	–	T.B.D.	T.B.D.	
Supply current in SLEEP1 mode			MNP·ATP = “1”	–	T.B.D.	T.B.D.	
			MNP·ATP = “0”	–	T.B.D.	T.B.D.	
Supply current in SLEEP0 mode			MNP·ATP = “1”	–	T.B.D.	T.B.D.	
			MNP·ATP = “0”	–	T.B.D.	T.B.D.	
Supply current in STOP mode			V_{DD} = 3.6 V V_{IN} = 3.4 V/0.2 V	–	T.B.D.	T.B.D.	

Note 1: Typical values show those at Topr = 25°C, V_{DD} = 3.3 V.

Note 2: Input current (I_{IN1}, I_{IN2}): The current through pull-up or pull-down resistor is not included.

Note 3: I_{DD} does not include I_{REF} current.

Note 4: The supply currents of SLOW 2 and SLEEP 2 modes are equivalent to IDLE0, 1, 2.

Note 5: Current capacity indicates the drop in pin V3 output voltage per $1\mu A$. Select an appropriate booster frequency setting in LCDCR<VFSEL> according to LCD panel. To maintain stable operation, the current capacity for the reference pin must be more than ten times that of the output current capacity.

Note 6: MNP (MNPWDW) shows bit0 in EEPCR register and ATP (ATPWDW) shows bit1 in EEPCR register.

Note 7: “Fetch” means reading operation of FLASH data as an instruction by CPU.

AD Conversion Characteristics (V_{SS} = 0.0 V, 2.7 V ≤ V_{DD} ≤ 3.6 V, Topr = –40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog reference voltage	V_{AREF}		A_{VDD} – 1.0	–	A_{VDD}	V
Power supply voltage of analog control circuit	A_{VDD}		V_{DD}			V
Analog reference voltage range (Note 4)	ΔV_{AREF}		2.5	–	–	V
Analog input voltage	V_{AIN}		V_{SS}	–	V_{AREF}	V
Power supply current of analog reference voltage	I_{REF}	V_{DD} = A_{VDD} = V_{AREF} = 3.6 V V_{SS} = 0.0 V	–	T.B.D.	T.B.D.	mA
Non linearity error		V_{DD} = A_{VDD} = 2.7 V V_{SS} = 0.0 V V_{AREF} = 2.7 V	–	–	±2	LSB
Zero point error			–	–	±2	
Full scale error			–	–	±2	
Total error			–	–	±2	

(V_{SS} = 0.0 V, 2.0 V ≤ V_{DD} < 2.7 V, Topr = –40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog reference voltage	V_{AREF}		A_{VDD} – 0.6	–	A_{VDD}	V
Power supply voltage of analog control circuit	A_{VDD}		V_{DD}			V
Analog reference voltage range (Note 4)	ΔV_{AREF}		2.0	–	–	V
Analog input voltage	V_{AIN}		V_{SS}	–	V_{AREF}	V
Power supply current of analog reference voltage	I_{REF}	V_{DD} = A_{VDD} = V_{AREF} = 2.0V V_{SS} = 0.0 V	–	T.B.D.	T.B.D.	mA
Non linearity error		V_{DD} = A_{VDD} = 2.0 V V_{SS} = 0.0 V V_{AREF} = 2.0 V	–	–	±4	LSB
Zero point error			–	–	±4	
Full scale error			–	–	±4	
Total error			–	–	±4	

(V_{SS} = 0.0 V, 1.8 V ≤ V_{DD} < 2.0 V, Topr = –10 to 85°C) (Note 5)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog reference voltage	V_{AREF}		A_{VDD} – 0.1	–	A_{VDD}	V
Power supply voltage of analog control circuit	A_{VDD}		V_{DD}			V
Analog reference voltage range (Note 4)	ΔV_{AREF}		1.8	–	–	V
Analog input voltage	V_{AIN}		V_{SS}	–	V_{AREF}	V
Power supply current of analog reference voltage	I_{REF}	V_{DD} = A_{VDD} = V_{AREF} = 1.8V V_{SS} = 0.0 V	–	T.B.D.	T.B.D.	mA
Non linearity error		V_{DD} = A_{VDD} = 1.8 V V_{SS} = 0.0 V V_{AREF} = 1.8 V	–	–	±4	LSB
Zero point error			–	–	±4	
Full scale error			–	–	±4	
Total error			–	–	±4	

Note 1: The total error includes all errors except a quantization error, and is defined as a maximum deviation from the ideal conversion line.

Note 2: Conversion time is different in recommended value by power supply voltage.
About conversion time, please refer to "2.12.2 Register Configuration".

Note 3: Please use input voltage to AIN input Pin in limit of V_{AREF} – V_{SS}.
When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.

Note 4: Analog Reference Voltage Range: $\Delta V_{AREF} = V_{AREF} - V_{SS}$.

Note 5: When AD is used with V_{DD} < 2.0 V, the guaranteed temperature range varies with the operating voltage.

Note 6: When AD converter is not used, fix the A_{VDD} pin on the V_{DD} level.

AC Characteristics (V_{SS} = 0 V, V_{DD} = 2.7 to 3.6 V, Topr = –40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine cycle time	tcy	NORMAL1, 2 mode IDLE1, 2 mode	0.25	–	4	μs
		SLOW1, 2 mode SLEEP1, 2 mode	117.6	–	133.3	
High level clock pulse width	twcH	For external clock operation (XIN input) fc = 16 MHz	–	31.25	–	ns
Low level clock pulse width	twcL					
High level clock pulse width	twcH	For external clock operation (XTIN input) fs = 32.768 kHz	–	15.26	–	μs
Low level clock pulse width	twcL					

(V_{SS} = 0 V, V_{DD} = 1.8 to 3.6 V, Topr = –40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine cycle time	tcy	NORMAL1, 2 mode IDLE1, 2 mode	0.5	–	4	μs
		SLOW1, 2 mode SLEEP1, 2 mode	117.6	–	133.3	
High level clock pulse width	twcH	For external clock operation (XIN input) fc = 8 MHz	–	62.5	–	ns
Low level clock pulse width	twcL					
High level clock pulse width	twcH	For external clock operation (XTIN input) fs = 32.768 kHz	–	15.26	–	μs
Low level clock pulse width	twcL					

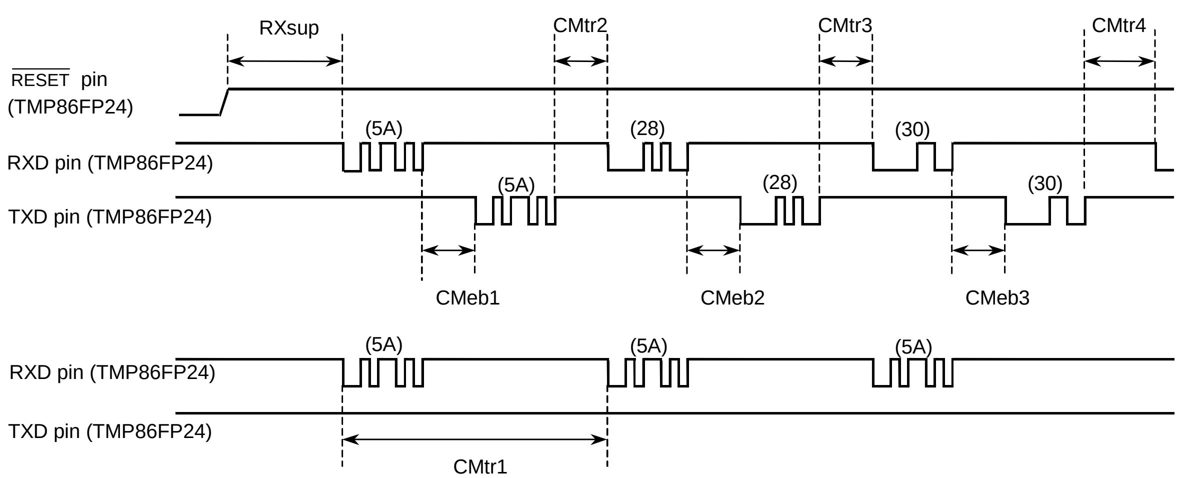
UART Timing in Serial PROM Mode

UART Timing-1 (VDD = 2.7 V to 3.6 V, fc = 2 MHz to 16 MHz,Ta = 25°C)

Parameter	Symbol	The Number of Clock (fc)	Required Minimum Time	
			at fc = 2 MHz	at fc = 16 MHz
Time from the reception of a matching data until the output of an echo back	CMeb1	Approx. 600	300 μs	37.5 μs
Time from the reception of a Baud Rate Modification Data until the output of an echo back	CMeb2	Approx. 700	350 μs	43.7 μs
Time from the reception of an operation command until the output of an echo back	CMeb3	Approx. 600	300 μs	37.5 μs
Calculation time of checksum	CKsm	Approx. 2360000	1180 ms	147.5 ms

UART Timing-2 (VDD = 2.7 V to 3.6 V, fc = 2 MHz to 16 MHz,Ta = 25°C)

Parameter	Symbol	The Number of Clock (fc)	Required Minimum Time	
			at fc = 2 MHz	at fc = 16 MHz
Time from reset release until acceptance of start bit of RXD pin	RXsup	110000	55 ms	6.9 ms
Time between a matching data and the next matching data	CMtr1	28500	14.3 ms	1.8 ms
Time from the echo back of matching data until the acceptance of baud rate modification data	CMtr2	600	300 μs	37.5 μs
Time from the output of echo back of baud rate modification data until the acceptance of an operation command	CMtr3	750	375 μs	46.9 μs
Time from the output of echo back of operation command until the acceptance of Password count storage addresses	CMtr4	950	475 μs	59.4 μs



Recommended Oscillating Conditions

Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.

Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following
http://www.murata.co.jp/search/index.html