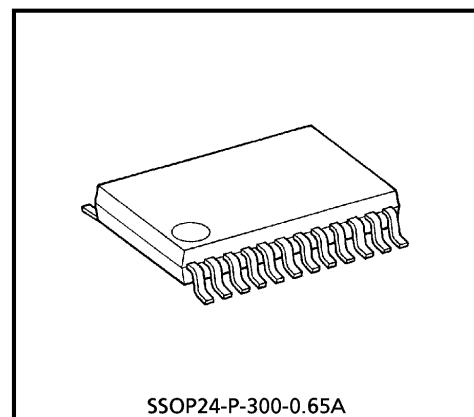


TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# TC74LCX652FS

## LOW VOLTAGE OCTAL BUS TRANSCEIVER / REGISTER WITH 5V TOLERANT INPUTS AND OUTPUTS

The TC74LCX652 is a high performance CMOS OCTAL BUS TRANSCEIVER / REGISTER. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. This device is designed for low-voltage (3.3V)  $V_{CC}$  applications, but it could be used to interface to 5V supply environment for both inputs and outputs. This device is bus transceiver with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers. All inputs are equipped with protection circuits against static discharge.



Weight : 0.14g (Typ.)

### FEATURES

- Low voltage operation :  $V_{CC} = 2.0 \sim 3.6V$
- High speed operation :  $t_{pd} = 7.0ns$  (Max.) ( $V_{CC} = 3.0 \sim 3.6V$ )
- Output current :  $|I_{OH}| / I_{OL} = 24mA$  (Min.) ( $V_{CC} = 3.0V$ )
- Latch-up performance :  $\pm 500mA$
- Available in SSOP.
- Bidirectional interface between 5V and 3.3V signals.
- Power down protection is provided on all inputs and outputs.
- Pin and function compatible with the 74 series (74AC / F / ALS / LS etc.) 652 type.

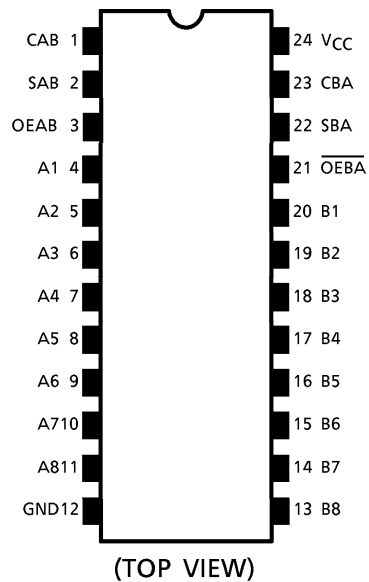
(Note) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.

All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

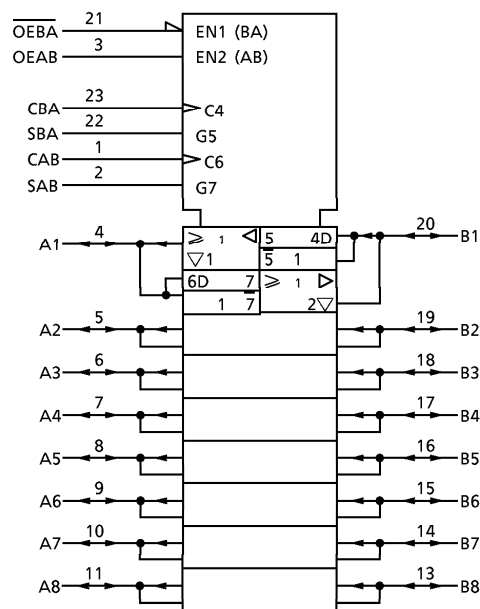
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**PIN ASSIGNMENT**



**IEC LOGIC SYMBOL**



TRUTH TABLE

| CONTROL INPUTS |      |                                                                                   |                                                                                     |     |     | BUS              |                 | FUNCTION                                                                                                                                         |
|----------------|------|-----------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-----|-----|------------------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| OEAB           | OEBA | CAB                                                                               | CBA                                                                                 | SAB | SBA | A                | B               |                                                                                                                                                  |
| L              | H    | X*                                                                                | X*                                                                                  | X   | X   | INPUT<br>Z       | INPUT<br>Z      | The output functions of A and B Busses are disabled.                                                                                             |
|                |      |  |    | X   | X   | X                | X               | Both A and B Busses are used as inputs to the internal flip-flops. Data on the Bus will be stored on the rising edge of the Clock.               |
|                |      | X*                                                                                | X*                                                                                  | L   | X   | INPUT<br>L<br>H  | INPUT<br>L<br>H | The data on the A bus are displayed on the B bus.                                                                                                |
| H              | H    |  | X*                                                                                  | L   | X   | L<br>H           | L<br>H          | The data on the A bus are displayed on the B Bus, and are stored into the A storage flip-flops on the rising edge of CAB.                        |
|                |      | X*                                                                                | X*                                                                                  | H   | X   | X                | Qn              | The data in the A storage flip-flops are displayed on the B Bus.                                                                                 |
|                |      |  | X*                                                                                  | H   | X   | L<br>H           | L<br>H          | The data on the A Bus are stored into the A storage flip-flops on the rising edge of CAB, and the stored data propagate directly onto the B Bus. |
|                |      | X*                                                                                | X*                                                                                  | X   | L   | OUTPUT<br>L<br>H | INPUT<br>L<br>H | The data on the B Bus are displayed on the A bus.                                                                                                |
|                |      | X*                                                                                |  | X   | L   | L<br>H           | L<br>H          | The data on the B Bus are displayed on the A Bus, and are stored into the B storage flip-flops on the rising edge of CBA.                        |
|                |      | X*                                                                                | X*                                                                                  | X   | H   | Qn               | X               | The data in the B storage flip-flops are displayed on the A Bus.                                                                                 |
| L              | L    | X*                                                                                |  | X   | H   | L<br>H           | L<br>H          | The data on the B Bus are stored into the B storage flip-flops on the rising edge of CBA, and the stored data propagate directly onto the A Bus. |
|                |      | X*                                                                                | X*                                                                                  | H   | H   | OUTPUT<br>Qn     | OUTPUT<br>Qn    | The data in the A storage flip-flops are displayed on the B Bus, and the data in the B storage flip-flops are displayed on the A.                |
|                |      | X*                                                                                | X*                                                                                  | H   | H   | Qn               | Qn              |                                                                                                                                                  |

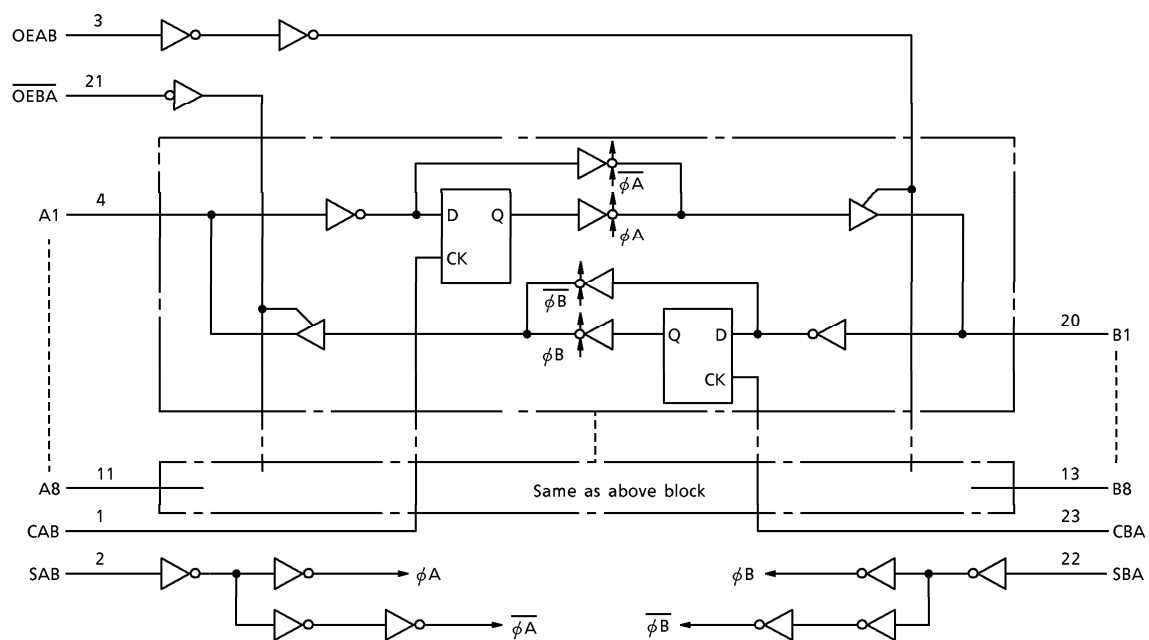
X : Don't care

Z : High Impedance

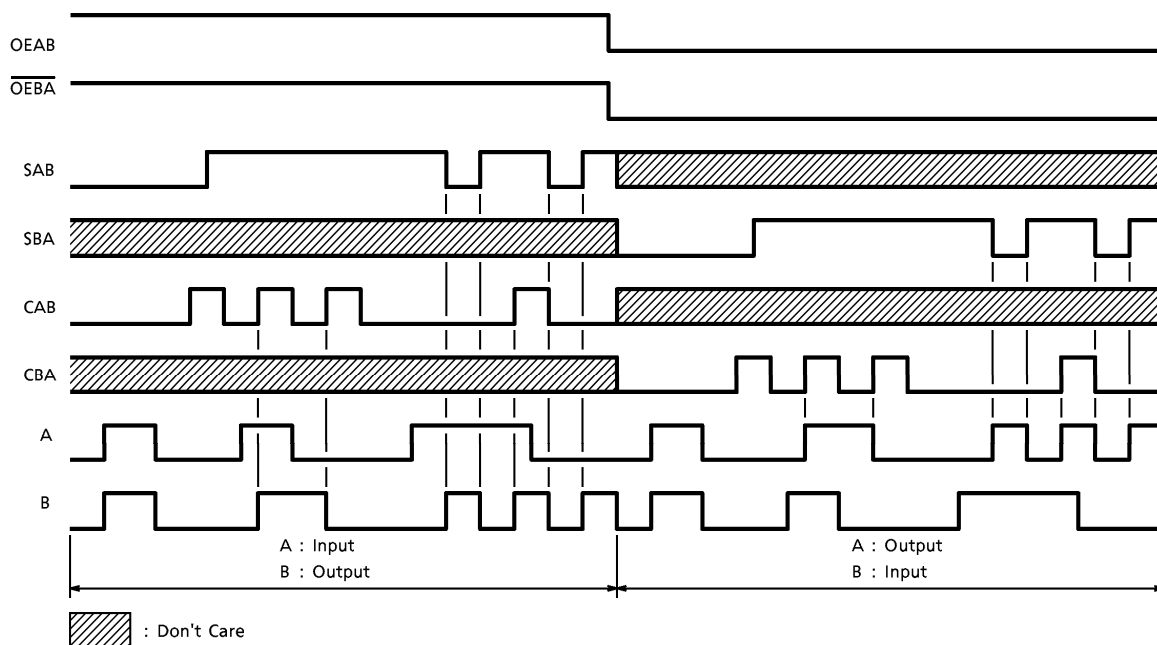
Qn : The data stored into the internal flip-flops by most recent low to high transition of the clock inputs.

\* The clocks are not internally gated with either OEAB or OEBA. Therefore, data on the A and/or B Busses may be clocked into the storage flip-flops at any time.

## SYSTEM DIAGRAM



## TIMING CHART



## MAXIMUM RATINGS

| PARAMETER                                               | SYMBOL           | RATING                         | UNIT |
|---------------------------------------------------------|------------------|--------------------------------|------|
| Supply Voltage Range                                    | $V_{CC}$         | - 0.5~7.0                      | V    |
| DC Input Voltage<br>(CAB, CBA, SAB, SBA, OEAB,<br>OEBA) | $V_{IN}$         | - 0.5~7.0                      | V    |
| DC Bus I/O Voltage                                      | $V_{I/O}$        | - 0.5~7.0 (Note 1)             | V    |
|                                                         |                  | - 0.5~ $V_{CC}$ + 0.5 (Note 2) |      |
| Input Diode Current                                     | $I_{IK}$         | - 50                           | mA   |
| Output Diode Current                                    | $I_{OK}$         | $\pm 50$ (Note 3)              | mA   |
| DC Output Current                                       | $I_{OUT}$        | $\pm 50$                       | mA   |
| Power Dissipation                                       | $P_D$            | 180                            | mW   |
| DC $V_{CC}$ /Ground Current                             | $I_{CC}/I_{GND}$ | $\pm 100$                      | mA   |
| Storage Temperature                                     | $T_{stg}$        | - 65~150                       | °C   |

(Note 1) Off-State

(Note 2) High or Low State.  $I_{OUT}$  absolute maximum rating must be observed.(Note 3)  $V_{OUT} < GND$ ,  $V_{OUT} > V_{CC}$ 

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER                                            | SYMBOL          | RATING               | UNIT |
|------------------------------------------------------|-----------------|----------------------|------|
| Supply Voltage                                       | $V_{CC}$        | 2.0~3.6              | V    |
|                                                      |                 | 1.5~3.6 (Note 4)     |      |
| Input Voltage<br>(CAB, CBA, SAB, SBA, OEAB,<br>OEBA) | $V_{IN}$        | 0~5.5                | V    |
| Bus I/O Voltage                                      | $V_{I/O}$       | 0~5.5 (Note 5)       | V    |
|                                                      |                 | 0~ $V_{CC}$ (Note 6) |      |
| Output Current                                       | $I_{OH}/I_{OL}$ | $\pm 24$ (Note 7)    | mA   |
|                                                      |                 | $\pm 12$ (Note 8)    |      |
| Operating Temperature                                | $T_{opr}$       | - 40~85              | °C   |
| Input Rise And Fall Time                             | $dt/dv$         | 0~10 (Note 9)        | ns/V |

(Note 4) Data Retention Only.

(Note 5) Off-State

(Note 6) High or Low State.

(Note 7)  $V_{CC} = 3.0 \sim 3.6V$ (Note 8)  $V_{CC} = 2.7 \sim 3.0V$ (Note 9)  $V_{IN} = 0.8 \sim 2.0V$ ,  $V_{CC} = 3.0V$

## ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = -40~85°C)

| PARAMETER                             |                 | SYMBOL                                        | TEST CONDITION                                                                    |                           | V <sub>CC</sub> (V) | MIN.                  | MAX. | UNIT |
|---------------------------------------|-----------------|-----------------------------------------------|-----------------------------------------------------------------------------------|---------------------------|---------------------|-----------------------|------|------|
| Input Voltage                         | "H" Level       | V <sub>IH</sub>                               |                                                                                   |                           | 2.7~3.6             | 2.0                   | —    | V    |
|                                       | "L" Level       | V <sub>IL</sub>                               |                                                                                   |                           | 2.7~3.6             | —                     | 0.8  |      |
| Output Voltage                        | "H" Level       | V <sub>OH</sub>                               | V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>                              | I <sub>OH</sub> = - 100μA | 2.7~3.6             | V <sub>CC</sub> - 0.2 | —    | V    |
|                                       |                 |                                               |                                                                                   | I <sub>OH</sub> = - 12mA  | 2.7                 | 2.2                   | —    |      |
|                                       |                 |                                               |                                                                                   | I <sub>OH</sub> = - 18mA  | 3.0                 | 2.4                   | —    |      |
|                                       |                 |                                               |                                                                                   | I <sub>OH</sub> = - 24mA  | 3.0                 | 2.2                   | —    |      |
|                                       | "L" Level       | V <sub>OL</sub>                               | V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>                              | I <sub>OL</sub> = 100μA   | 2.7~3.6             | —                     | 0.2  |      |
|                                       |                 |                                               |                                                                                   | I <sub>OL</sub> = 12mA    | 2.7                 | —                     | 0.4  |      |
|                                       |                 |                                               |                                                                                   | I <sub>OL</sub> = 16mA    | 3.0                 | —                     | 0.4  |      |
|                                       |                 |                                               |                                                                                   | I <sub>OL</sub> = 24mA    | 3.0                 | —                     | 0.55 |      |
| Input Leakage Current                 |                 | I <sub>IN</sub>                               | V <sub>IN</sub> = 0~5.5V                                                          | 2.7~3.6                   | —                   | ± 5.0                 | μA   |      |
| 3-State Output Off-State Current      |                 | I <sub>OZ</sub>                               | V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>V <sub>OUT</sub> = 0~5.5V | 2.7~3.6                   | —                   | ± 5.0                 | μA   |      |
| Power Off Leakage Current             |                 | I <sub>OFF</sub>                              | V <sub>IN</sub> / V <sub>OUT</sub> = 5.5V                                         | 0                         | —                   | 10.0                  | μA   |      |
| Quiescent Supply Current              | I <sub>CC</sub> | V <sub>IN</sub> = V <sub>CC</sub> or GND      |                                                                                   | 2.7~3.6                   | —                   | 10.0                  | μA   |      |
|                                       |                 | V <sub>IN</sub> / V <sub>OUT</sub> = 3.6~5.5V |                                                                                   | 2.7~3.6                   | —                   | ± 10.0                |      |      |
| Increase In I <sub>CC</sub> Per Input |                 | ΔI <sub>CC</sub>                              | V <sub>IH</sub> = V <sub>CC</sub> - 0.6V                                          |                           | 2.7~3.6             | —                     |      | 500  |

AC characteristic (Ta = -40~85°C)

| PARAMETER                                | SYMBOL                                   | TEST CONDITION | V <sub>CC</sub> (V) | MIN. | MAX. | UNIT |
|------------------------------------------|------------------------------------------|----------------|---------------------|------|------|------|
|                                          |                                          |                |                     |      |      |      |
| Maximum Clock Frequency                  | f <sub>MAX</sub>                         | (Fig.1, 2)     | 2.7                 | —    | —    | MHz  |
|                                          |                                          |                | 3.3 ± 0.3           | 150  | —    |      |
| Propagation Delay Time (An, Bn-Bn, An)   | t <sub>pLH</sub><br>t <sub>pHL</sub>     | (Fig.1, 2)     | 2.7                 | —    | 8.0  | ns   |
|                                          |                                          |                | 3.3 ± 0.3           | 1.5  | 7.0  |      |
| Propagation Delay Time (CAB, CBA-Bn, An) | t <sub>pLH</sub><br>t <sub>pHL</sub>     | (Fig.1, 5)     | 2.7                 | —    | 9.5  | ns   |
|                                          |                                          |                | 3.3 ± 0.3           | 1.5  | 8.5  |      |
| Propagation Delay Time (SAB, SBA-Bn, An) | t <sub>pLH</sub><br>t <sub>pHL</sub>     | (Fig.1, 2)     | 2.7                 | —    | 9.5  | ns   |
|                                          |                                          |                | 3.3 ± 0.3           | 1.5  | 8.5  |      |
| Output Enable Time (OEAB, OEBA-An, Bn)   | t <sub>pZL</sub><br>t <sub>pZH</sub>     | (Fig.1, 3, 4)  | 2.7                 | —    | 9.5  | ns   |
|                                          |                                          |                | 3.3 ± 0.3           | 1.5  | 8.5  |      |
| Output Disable Time (OEAB, OEBA-An, Bn)  | t <sub>pLZ</sub><br>t <sub>pHZ</sub>     | (Fig.1, 3, 4)  | 2.7                 | —    | 9.5  | ns   |
|                                          |                                          |                | 3.3 ± 0.3           | 1.5  | 8.5  |      |
| Minimum Pulse Width                      | t <sub>w</sub> (H)<br>t <sub>w</sub> (L) | (Fig.1, 5)     | 2.7                 | 3.3  | —    | ns   |
|                                          |                                          |                | 3.3 ± 0.3           | 3.3  | —    |      |
| Minimum Set-up Time                      | t <sub>s</sub>                           | (Fig.1, 5)     | 2.7                 | 2.5  | —    | ns   |
|                                          |                                          |                | 3.3 ± 0.3           | 2.5  | —    |      |
| Minimum Hold Time                        | t <sub>h</sub>                           | (Fig.1, 5)     | 2.7                 | 1.5  | —    | ns   |
|                                          |                                          |                | 3.3 ± 0.3           | 1.5  | —    |      |
| Output To Output Skew                    | t <sub>osLH</sub><br>t <sub>osHL</sub>   | (Note 10)      | 2.7                 | —    | —    | ns   |
|                                          |                                          |                | 3.3 ± 0.3           | —    | 1.0  |      |

(Note 10) Parameter guaranteed by design.

(t<sub>osLH</sub> = |t<sub>pLHm</sub> - t<sub>pLHn</sub>|, t<sub>osHL</sub> = |t<sub>pHLm</sub> - t<sub>pHLn</sub>|)DYNAMIC SWITCHING CHARACTERISTICS (Ta = 25°C, Input t<sub>r</sub> = t<sub>f</sub> = 2.5ns, C<sub>L</sub> = 50pF, R<sub>L</sub> = 500Ω)

| PARAMETER                                    | SYMBOL           | TEST CONDITION                                         | V <sub>CC</sub> (V) | TYP. | UNIT |
|----------------------------------------------|------------------|--------------------------------------------------------|---------------------|------|------|
|                                              |                  |                                                        |                     |      |      |
| Quiet Output Maximum Dynamic V <sub>OL</sub> | V <sub>OLP</sub> | V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V (Note 11) | 3.3                 | 0.8  | V    |
| Quiet Output Minimum Dynamic V <sub>OL</sub> | V <sub>OLV</sub> | V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V (Note 11) | 3.3                 | 0.8  | V    |

(Note 11) Characterized with 7 outputs switching from High-to-Low or Low-to-High. The remaining output is measured in the Low state.

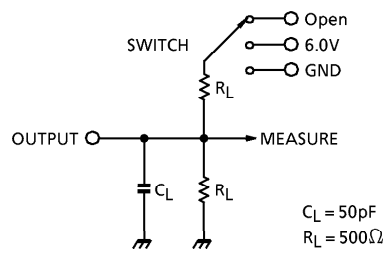
CAPACITIVE CHARACTERISTICS (Ta = 25°C)

| PARAMETER                     | SYMBOL           | TEST CONDITION                    | V <sub>CC</sub> (V) | TYP. | UNIT |
|-------------------------------|------------------|-----------------------------------|---------------------|------|------|
|                               |                  |                                   |                     |      |      |
| Input Capacitance             | C <sub>IN</sub>  | OEAB, OEBA, CAB, CBA, SAB, SBA    | 3.3 ± 0.3           | 7    | pF   |
| Bus Input Capacitance         | C <sub>I/O</sub> | An, Bn                            | 3.3 ± 0.3           | 8    | pF   |
| Power Dissipation Capacitance | C <sub>PD</sub>  | f <sub>IN</sub> = 10MHz (Note 12) | 3.3 ± 0.3           | 25   | pF   |

(Note 12) C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.  
Average operating current can be obtained by the equation :  
 $I_{CC (opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8$  (per bit)

TEST CIRCUIT

Fig.1



| PARAMETER                                                           | SWITCH |
|---------------------------------------------------------------------|--------|
| t <sub>pLH</sub> , t <sub>pHL</sub>                                 | Open   |
| t <sub>pLZ</sub> , t <sub>pZL</sub>                                 | 6.0V   |
| t <sub>pHZ</sub> , t <sub>pZH</sub>                                 | GND    |
| t <sub>w</sub> , t <sub>s</sub> , t <sub>h</sub> , f <sub>MAX</sub> | Open   |



## AC WAVEFORM

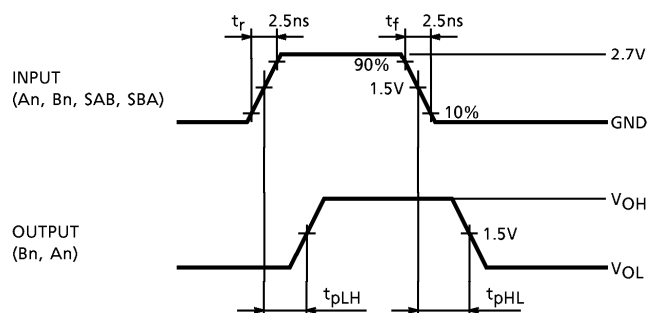
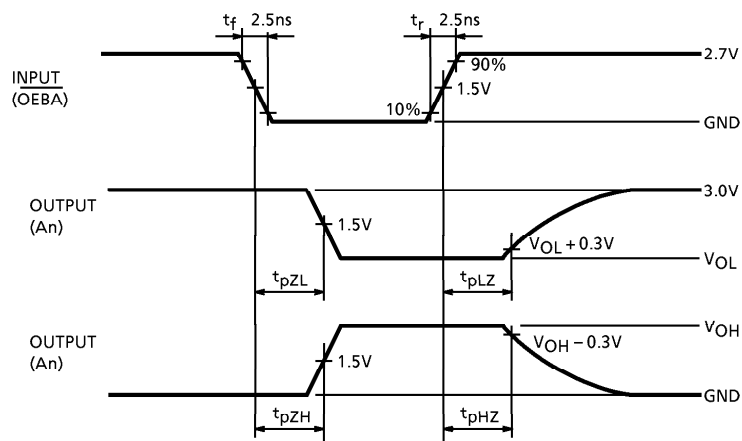
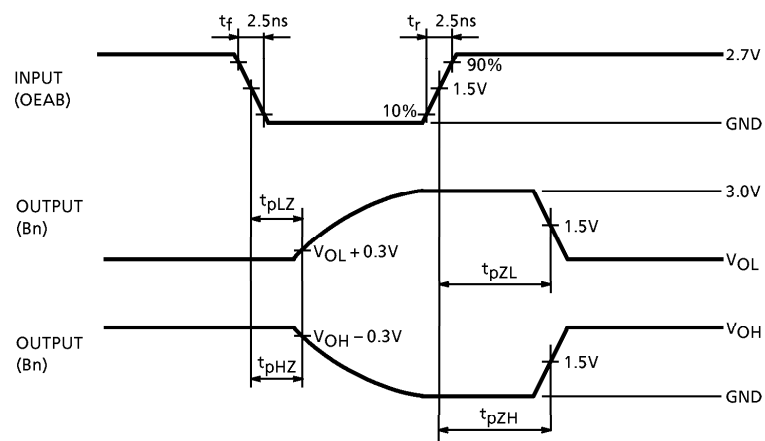
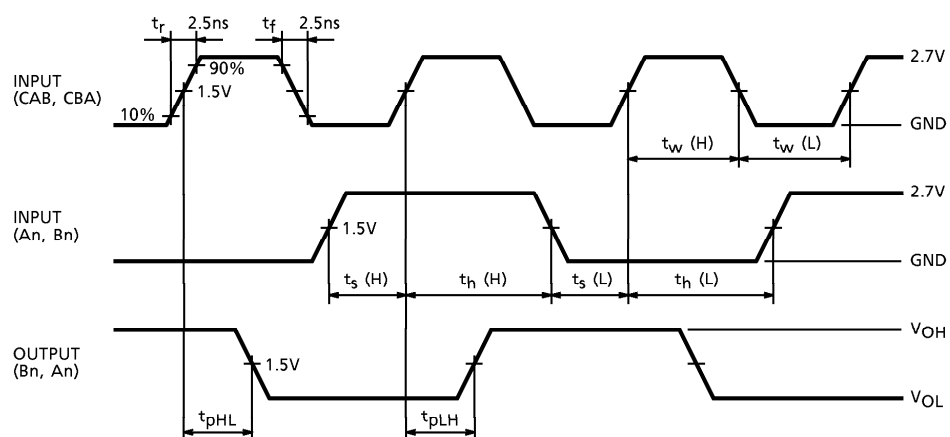
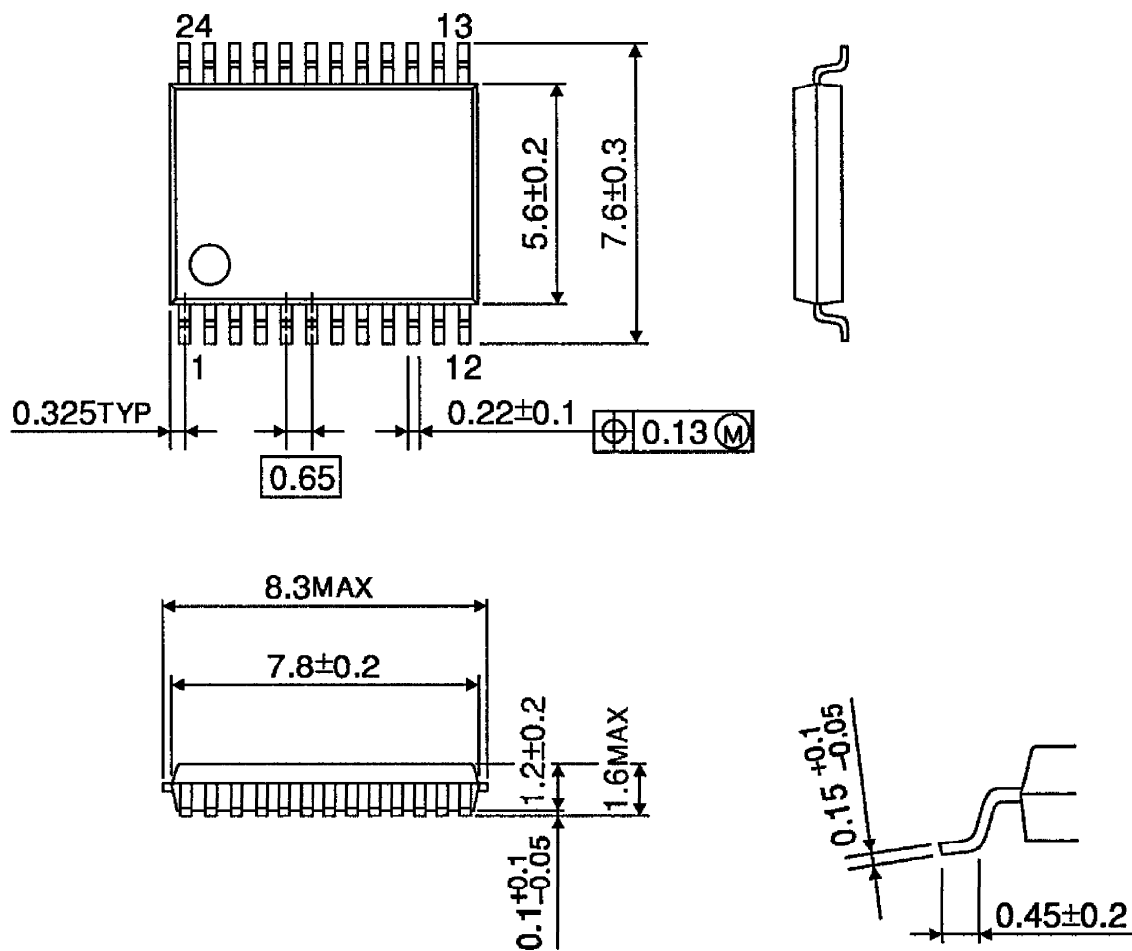
Fig.2  $t_{pLH}$ ,  $t_{pHL}$ Fig.3  $t_{pLZ}$ ,  $t_{pHZ}$ ,  $t_{pZL}$ ,  $t_{pZH}$ 

Fig.4  $t_{pLZ}$ ,  $t_{pHZ}$ ,  $t_{pZL}$ ,  $t_{pZH}$ Fig.5  $t_{pLH}$ ,  $t_{pHL}$ ,  $t_w$ ,  $t_s$ ,  $t_h$ 

## OUTLINE DRAWING

SSOP24-P-300-0.65A

Unit : mm



Weight : 0.14g (Typ.)